



# IMPLEMENTATION AND SIMULATION OF DIRECT TORQUE CONTROL SCHEME WITH THE USE OF FPGA CIRCUIT

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## ABSTRACT

This paper presents a simple approach to design and implementation of Direct Torque Control (DTC) of three phase squirrel cage induction motor using Matlab/Simulink and FPGA software. The direct torque control of induction machine is a simple control. To maintain this simple control structure while at the same time improving the performance of the DTC drives two simple new techniques i.e. constant switching frequency and stator flux estimation are proposed. To maintain a constant switching a simple torque control is introduced to replace the three level hysteresis comparators. The magnitude and phase error associated with stator flux estimation based on voltage model is compensated by using simple compensator which is based on steady state operation.

**Keywords:** FPGA, VHDL, induction motor, methodology, DoPC.

## 1. INTRODUCTION

Induction motors have many advantages when compared to direct current (DC) motors. The well known advantages are simple construction, reliability, ruggedness, and low cost. Nevertheless, DC drives have dominated the field of adjustable speed drives, due to the high dynamic performances [14]. Induction machine control was only possible after the development of powerful switching component and efficient control techniques. For instance, the first control theory was presented in 1971 [15] and implemented ten years later with the advent of microprocessors. Induction motor control methods can be divided into scalar and vector control. In scalar control, which is based on relationships valid in steady state, only magnitude and frequency of voltage, current, and flux linkage space vector are controlled. In vector control, which is based on relations valid for dynamic state, not only magnitude and frequency but also instantaneous position of voltage, current, and flux space vector are controlled. Vector control is general control philosophy that can be implemented in many different ways; the most popular method is field oriented control (FOC). In the mid 1980s, the innovative studies of Depenbrock [19], [20] and of Takahashi and Noguchi [21] which depart from the idea of coordinate transformation and the analogy with dc motor control. These innovators proposed to replace the decoupling control, which meets very well with on-off operation of the inverter semiconductor power devices. This control strategy is commonly referred to as direct torque control (DTC). Allowing for a performance even superior to DC machine drives. The DTC scheme is very simple, in its basic configuration it consists of DTC controller, torque and flux calculator and voltage source inverter. The configuration is much simpler than the Field Oriented Control (FOC) system due to the following features:

- Absence of frame transformer.

- No current control loop, hence, the current is not regulated directly.
- It does not need pulse width modulator and position encoder, which introduce delays and requires mechanical transducers respectively.
- Stator flux vector and torque estimation is required.

The DTC method was introduced two decades ago, a number of technical papers appear in the literature mainly to improve the performance of DTC of induction machines. The two problems usually associated with DTC drives which are based on hysteresis comparators are: (i) variable switching frequency due to the hysteresis comparators used for the torque and flux comparators and (ii) inaccurate stator flux estimations which can degrade the drive performance. Generally, the stator flux is estimated based on the variation of the two types of estimators, namely the voltage and current models [17]. To take advantage of both type of estimators, some researchers have combined both types of estimators, namely the voltage and current models. However, the use of current model will require a speed sensor or speed estimators which in both cases are undesirable. To maintain a speed sensorless operation, only voltage model has to be used. In voltage model technique, low pass (LP) estimator is normally used in place of a pure integrator to avoid integration drift problem [18]. The LP filter however introduces magnitude and phase errors in the estimated flux.

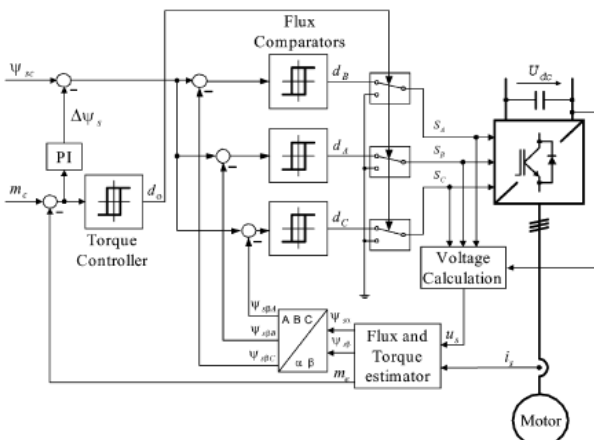
This paper proposed a simple yet effective methods to overcome these two problems. To maintain a constant switching frequency, a simple torque controller is introduced to replace the conventional 3-level hysteresis comparator. The magnitude and phase error associated with stator flux estimation based on voltage model is compensated by using simple compensator which is based on steady state operations. The rest of the paper is organised as follows. Section-II presents the



proposed torque controller and Section-III presents the improved stator flux estimation methods. Section-IV presents the FPGA based design methodology for the complete control. Section-V presents the simulation and experimental results of the proposed methods. Finally, conclusions are given.

**2. DTC PRINCIPLES**

The block diagram of the Direct Self Control (DSC) scheme, proposed by Depenbrock [22], is shown in Figure-1. Based on stator flux components  $\psi_{s\beta A}$ ,  $\psi_{s\beta B}$  and  $\psi_{s\beta C}$ , the flux comparators generate the digitized variables  $d_A$ ,  $d_B$ , and  $d_C$  which correspond to active voltage vectors for six-step operation.



**Figure-1.** Direct Self Control (DSC) scheme.

The hysteresis torque controller, on the other hand, generates the digitized signal that determines the zero states duration. In the field-weakening region, where the inverter is in six-step operation under rated output voltage, the torque is not determined by the hysteresis torque controller but by a momentary change of the stator flux amplitude. In a simple case, it can be obtained by means of the PI-flux controller of Figure-1. However, for precise control, more complex calculation is required.

A DTC drive based on fixed torque hysteresis band, suffer from a varying rate of change of torque which is simply referred to as torque slope and hence torque controller switching frequency, as a function of motor speed, stator and rotor fluxes, and stator voltage. This in turn results in a varying device switching frequency. Variable switching frequency is undesirable since the switching capability of the inverter is not fully utilized. For fixed torque band, the choice of the band's width is normally based on the worst condition which is limited by the thermal condition of the switching devices, thus operation for other conditions are not optimized. The torque slope is given in equation (1)

$$\frac{T_{e(n+1)} - T_{e(n)}}{\Delta t} = -T_{e(n)} \left( \frac{1}{\sigma\tau_s} + \frac{1}{\sigma\tau_r} \right) + \frac{3p}{2} \frac{L_m}{\sigma L_s L_r} \left[ \left( \bar{V}_{s,n} - j\omega_r \bar{\psi}_{s(n)}^g \right) \cdot j\bar{\psi}_{r,n}^g \right] \tag{1}$$

The negative slope can be obtained by setting the active voltage  $\bar{V}_{s,n}$  to zero, thus

$$\text{slope}^- = \frac{T_{e(n+1)} - T_{e(n)}}{\Delta t} = -\frac{T_{e(n)}}{\sigma\tau_{s,r}} + \frac{3p}{4} \frac{L_m}{\sigma L_s L_r} \left[ \left( -j\omega_r \bar{\psi}_s \right) \cdot j\bar{\psi}_r \right] \tag{2}$$

On the other hand, positive slope is given by the non-zero voltage vectors, thus

$$\text{slope}^+ = \frac{T_{e(n+1)} - T_{e(n)}}{\Delta t} = -\frac{T_{e(n)}}{\sigma\tau_{s,r}} + \frac{3p}{4} \frac{L_m}{\sigma L_s L_r} \left[ \left( \bar{V}_s - j\omega_r \bar{\psi}_s \right) \cdot j\bar{\psi}_r \right] \tag{3}$$

**2.1. Proposed torque control**

The proposed torque controller consists of two triangular waveform generators, two comparators and a PI controller. The two triangular waveforms are 180° out of phase with each other. The triangular waveforms are referred as upper and lower carriers. The offset values of the DC offsets of upper and lower carriers are set to half of its peak to peak value. The upper dc offset is positive while the lower is negative. The output of the proposed torque controller is similar to that of the three level hysteresis comparator [16], which can be either of three states: -1, 0 or 1.

The value of the instantaneous output of the torque controller designated by  $q(t)$  is given by:

$$q(t) = \begin{cases} 1 & \text{for } T_{pi} \geq C_{upper} \\ 0 & \text{for } C_{lower} < T_{pi} < C_{upper} \\ -1 & \text{for } T_{pi} \leq C_{lower} \end{cases} \tag{4}$$

The average torque error status  $q(t)$  is defined as continuous duty ratio and is denoted by  $d(t)$ . The average is taken over an interval  $T_{tri}$ , which is the period of the triangular carrier waveform. It is defined by:

$$d(t) = \frac{1}{T_{tri}} \int_t^{t+T_{tri}} q(t) dt \tag{5}$$

The values of the PI controller parameters are chosen based on the linear analysis of the controller. The linear model is obtained by averaging and linearising the torque equations (2) and (3). It can be shown that the positive and negative torque slope equations are given by (6) and (7) respectively,

$$dT_e^+ = -AT_e + Bv_s^{u/s} + K_1 \left( \frac{\omega_e}{d} - \omega_e \right) \tag{6}$$

$$\frac{dT_e^-}{dt} = -AT_e - K_1 \omega_r \tag{7}$$

Where,



$$A = \frac{1}{\sigma \tau_{s,r}}$$

$$B = \frac{3p}{4} \frac{L_m}{\sigma L_s L_r} \psi_s$$

$$K_1 = \frac{3p}{4} \frac{L_m}{\sigma L_s L_r} (\psi_s \psi_r^{\psi_s})$$

Averaging and linearising equations (6) and (7), and with further simplifications, it can be shown that

$$\frac{dT_e}{dt} = -AT_e + Bv_s^{\psi_s} d + K_1(\omega_{slip}) \quad (8)$$

Based on equation (8), the transfer function between  $d$  and  $T_e$  can be obtained by setting the slip frequency to zero. It can also be shown that the transfer function between the output of the PI controller,  $T_{pi}$  and the averaged duty ratio  $\bar{d}$  is given by a reciprocal of the peak-peak triangular carrier,  $C_{pp}$ . The values of the PI controller's parameters are chosen based on the following constraints: (i) the absolute slope of equation (5) and (6) cannot exceed the triangular carrier slope. (ii) The crossover frequency of the loop gain (bandwidth) cannot exceed half of the carrier triangular frequency.

**2.2. Stator flux estimation**

Stator flux estimation based on voltage model is carried out by using following equation (9)

$$\bar{\psi}_s = \int (\bar{V} - \bar{i}_s R_s) dt \quad (9)$$

To avoid integration drift problem due to the dc off-set or measurement noise, a low-pass filter is normally used in place of the pure integrator in stator flux estimation. With a low-pass filter, sinusoidal steady state form, it can be shown that:

$$\bar{\psi}_s = \frac{\bar{V}_s - \bar{I}_s R_s}{j\omega_e + \omega_c} \quad (10)$$

where  $\omega_c$  is the cut-off frequency of the low-pass filter in rad/s and  $\bar{\psi}_s'$  is the estimated stator based on LP filter.

If  $\bar{\psi}_s' = \psi_s' \angle \theta'$  and  $\bar{\psi}_s = \psi_s \angle \theta$ , then it can be shown that the relation between the estimated stator flux based on LP filter and pure integrator is given by (11):

$$\frac{\psi_s'}{\psi_s} \angle \theta' - \theta = \frac{\omega_e}{\sqrt{\omega_e^2 + \omega_c^2}} \angle \phi \quad (11)$$

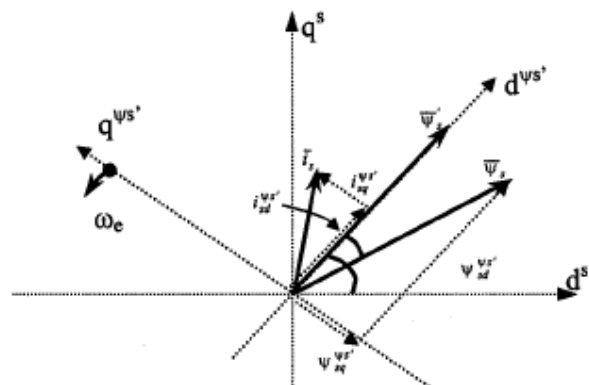
$$\phi = (\pi / 2) - \tan^{-1} \left( \frac{\omega_e}{\omega_c} \right)$$

The core of the proposed improvement is to provide a magnitude and phase compensations for the estimated flux, under steady state condition, only at the

operating frequency thus improving the steady state performance of the DTC drive. In other words, the LP filter action is effective at all frequencies except at the operating frequency, that is,

$$\psi_s' = \begin{cases} \frac{v - iR}{j\omega} & \text{for } \omega = \omega_e \\ \frac{v - iR}{j\omega + \omega_c} & \text{for } \omega \neq \omega_e \end{cases} \quad (12)$$

The LP filter action is therefore valid or effective for the DC offsets and low frequency components present in the sensed currents or voltages. This avoids the integration drift problem while maintaining good system stability. This is due to the fact that the phase and magnitude errors are compensated at the operating frequency. The stator flux is compensated at the operating frequency for the d and q components by determining the expressions for the actual stator flux in terms of estimated stator flux in the stationary reference frame. Figure-2 shows the relationship of the estimated and actual stator flux with their d and q components in the stationary reference frame, denoted by the direct and quadrature axis,  $d^s$  and  $q^s$ .



**Figure-2.** Space vectors of stator current, actual stator flux, and estimated stator flux with rotating and stationary reference frame.

The compensated flux is given in (13) and (14) and can be incorporated in the flux estimator block. The compensator can be initiated by the flag manually or based on steady state speed error.

$$\psi_{sq} = \left( \psi_q' - \psi_d' \frac{\omega_c}{\omega_e} \right) \quad (13)$$

$$\psi_{sd} = \left( \psi_d' - \psi_q' \frac{\omega_c}{\omega_e} \right) \quad (14)$$

The synchronous speed is  $\omega_e$  is obtained from the measured terminal variables using (15).



$$\omega_e = -\frac{(\overline{V}_s - \overline{I}_s R_s)}{\psi_s^2} \cdot j\psi_s \quad (15)$$

**3. FPGA DESIGN METHODOLOGY**

The steps in the design procedure for the drive system using the proposed controller are illustrated in the flow diagram in Figure-3. The complete DTC model, including the power circuit and the controller is simulated in Matlab / Simulink. When the controller performs as expected in simulation, a VHDL representation of controller can be generated using a special block of the Xilinx System Generator (SG). SG blocks are like standard Simulink blocks except that they can operate only in discrete-time and fixed point format. The two control blocks are simulated in Matlab / Simulink and then built using SG block. The design methodology uses FPGAs as the target device and parameter driven VHDL style coding to describe the digital circuit. All the modules were designed and tested in the Xilinx Foundation Express. The design flow of the overall coding is compiled and synthesized using the popular synthesis tool Synplify. Before synthesis the target device has to be selected. During synthesis a gate level net list is developed in an Electronic Data Interchange Format (EDIF). A file bearing EDIF net list information is created with various extension names depending on the target type.

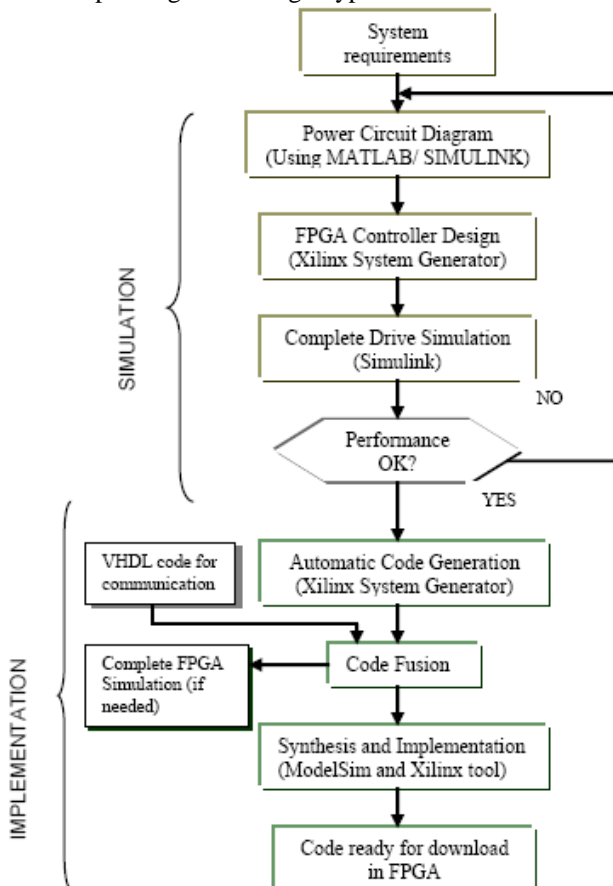


Figure-3. Methodology design flow.

The target XC2S100 FPGA of Xilinx family is used here in the design and the relevant EDIF net list file created carries .vqm (Verilog Quartus Map) extension. During synthesis and RTL (Register Transfer Level) corresponding to the design code is developed, which represents an optimized design. The Quartus-II tool compiler creates the .vho (VHDL output file) that contains post routing and post partitioning net list information for timing simulation carried out by ModelSim. The .sof (SRAM Object file) file generated during Placement and Routing is downloaded finally to the FPGA target via JTAG (Joint Test Action Group) port. The XC2S100 FPGA is used as the target. Thus the entire design is strictly based on the FPGA design flow concepts and rendered expected results. The development of each module in terms of architecture is based on standardization principles. These principles are regularity, understandability, and reusability of already designed components. The architecture of stator flux, rotor flux and torque estimator are shown in Figure-4. The resulting RTL model of the estimator architecture presenting the VHDL entity is shown in Fig-5.

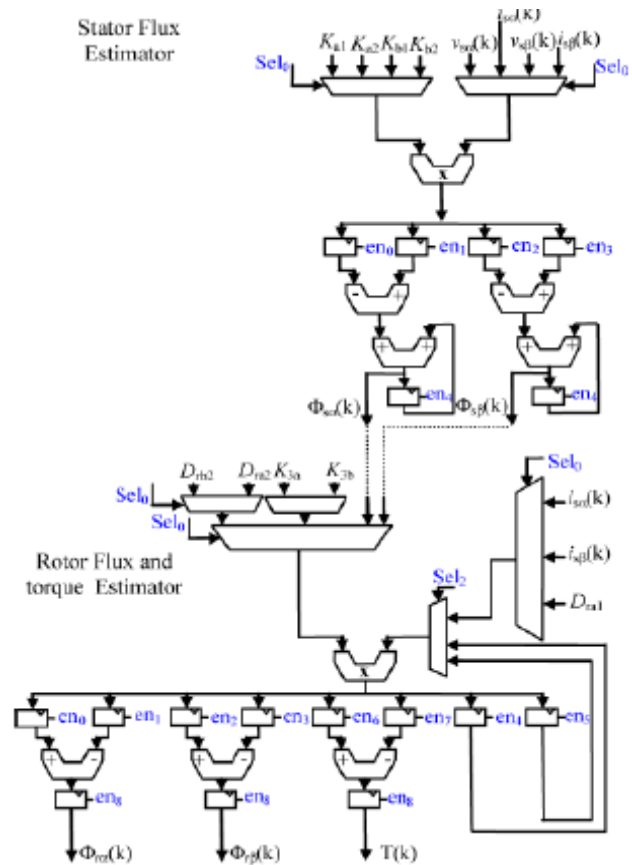


Figure-4. Architecture of Stator Flux, Rotor Flux, and Torque Estimators.

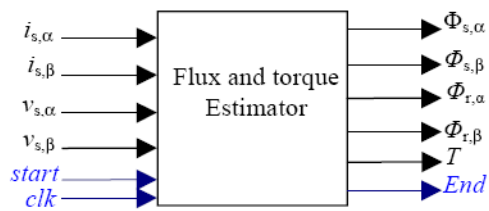


Figure-5. RTL model of the estimator architecture.

#### 4. RESULTS

Experimentation was carried out with ¼ kW, 2 poles induction motor. The experimental setup consists of Xilinx FPGA device (XC2S100), IGBT based VSI, Induction motor and peripheral devices such as ADC, VSI interface board, DAC and a host PC connected with the FPGA via serial interface. The analog to digital conversion time is equal to 2.4µs. The block diagram of the experimental set-up is shown in Figure-6.

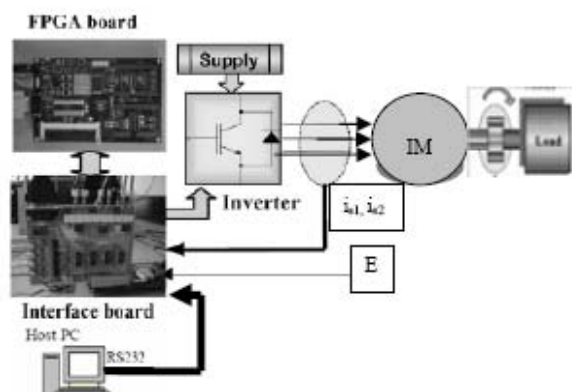
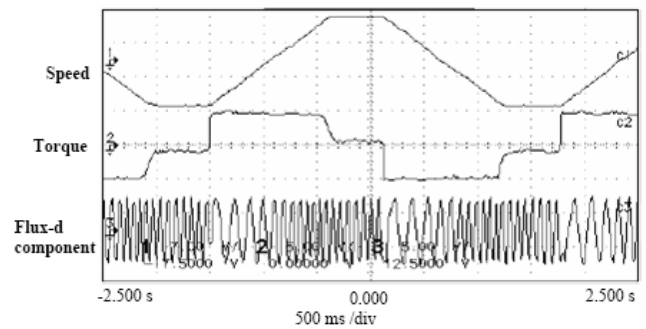
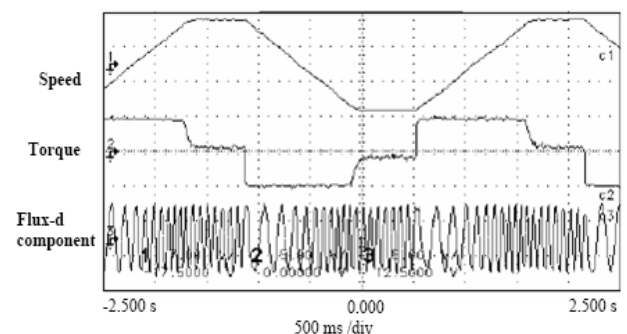


Figure-6. Experimental set-up.

To look at the dynamic response of the proposed controller, a square wave speed command is applied and the waveforms of the rotor speed, torque and d-axis stator flux is as shown in Figure-7(a). For comparison, the same command is applied to the hysteresis-based torque controller with the results shown in Figure-7(b). From the Figure it can be seen that with the proposed controller, the dynamic torque controller is the same as with the hysteresis based controller, with an added advantage of a reduced torque ripple [23]. The compensation and estimations were done within the software with sampling frequency of 55µs. The frequency spectrum of the phase currents at rotor speed of 10 rad/sec for the proposed torque controller is shown in Figure-8. The steady state stator flux vector locus for the proposed torque controller is shown in Figure-8(a) and (b) present torque response to a step control from 0 N.m to 4 N.m. It shows that torque response do not present large ripples with the proposed torque controller by comparison to hysteresis based controller.



(a)



(b)

Figure-7. Response for a square wave speed reference for (a) proposed torque controller and (b) a hysteresis-based controller.

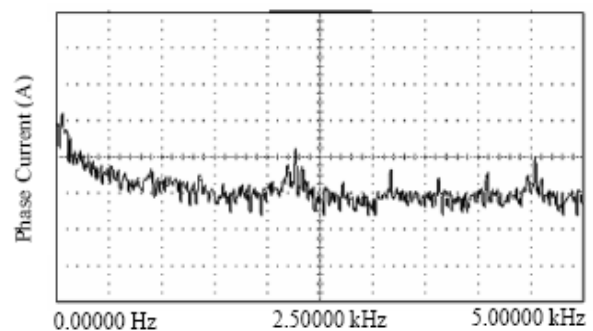
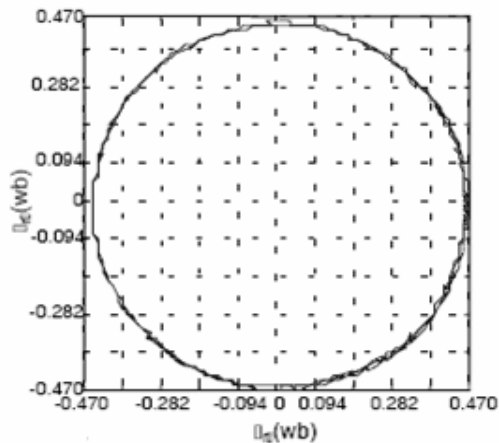
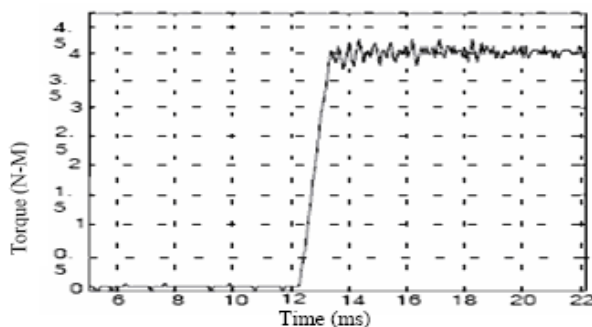


Figure-8. Experimental result of phase current frequency spectrum for proposed torque controller.



(a)



(b)

**Figure-9.** Experimental results obtained with the proposed torque controller: (a) Steady state rotor flux vector locus, (b) torque response to a step control.

## 5. CONCLUSIONS

The new torque controller for constant switching frequency and a compensation scheme to eliminate the phase and magnitude errors for the stator flux estimation under steady state condition is proposed. The obtained results have demonstrated that FPGAs are well suited for implementation of complex motor control and estimation algorithms due to their very high execution speed. The architecture contains a set of building blocks. Each block is geared towards a specific algorithm function. To increase module reutilization, standard and modular design principle is proposed. The modules can be readily suit new requirements such as modification of communication system, addition of measured variable, and modification of control configuration. In the proposed approach, the design time could be reduced because of the accuracy of the simulation attainable with Simulink and Xilinx System Generator at every operation details of FPGA. Most of the time only one step of debugging is required because the design in Simulink represents an exact model of the actual device. This simple scheme has significantly improved the performance of the DTC drive system while at the same time maintaining the simple control structure of the DTC drive.

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