



EVALUATION OF SUBSTRATE AND WELL DOPING LEVELS AND CHIP DIMENSIONS TO PREVENT LATCH-UP IN CMOS INVERTER CIRCUITS IN SILICON USING P-WELL TECHNOLOGY WITH LINE GEOMETRY OF 0.5 μm

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ABSTRACT

CMOS inverter circuits in silicon employing p-well technology have a low current consumption in both the on and off states. However, the inherent and undesirable parasitic bipolar transistors give rise to latch-up which results in a large current flow through the chip. Based on the equivalent circuit of the parasitic transistors, it can be shown that latch-up can be prevented using a suitable substrate and well dopings. In this paper an analytical study has been made and optimum substrate and well dopings have been evaluated with (W/L) ratio ranging from 2 to 0.05 for both p-n-p and n-p-n transistors. It is expected that both substrate and well dopings of $10^{15}/\text{cc}$ will help to solve the latch up problem for (W/L) ratio of 1.

Keywords: CMOS inverter circuit, doping levels, chip dimensions.

INTRODUCTION

CMOS inverter circuits have been in use for quite sometime now and serve as the basic element of CMOS logic operations. These circuits have the major advantage of using a small chip area as compared to BJT based similar circuits and have significantly low power consumption in both the on and off states [1]. Normally on chip fabrication of the CMOS circuits require the use of well technology using either (1) p-well, (2) n-well or (3) twin-tub structures. However, these structures form undesirable and in-built bipolar p-n-p and n-p-n parasitic transistors which give rise to latch up causing a large current to flow from the drain supply voltage V_{DD} to ground. The problem of latch-up technology has been solved by using the Refilled Trench Technology, whereas the p and n, twin tubes are separated by the trench [2] and the parasitic transistors become isolated from each other. These technologies require additional processing steps and are expensive. Another way to reduce the latch is to use a heavily doped substrate with devices fabricated on a highly doped epitaxial layer [3-8]. Other techniques involve the use of retrograde wells and can reduce the current gain of vertical transistors, thereby preventing latch up to occur [9-12].

In this paper an attempt has been made to reduce the current gain of the vertical and lateral parasitic transistors and solve the problem of latch-up. This has been done by estimating the current gain of the two transistors by changing the substrate and well doping such that they do not fill the condition necessary for latch-up using the equivalent circuit of the parasitic regions which involve the p-n-p and n-p-n transistor and the substrate and well resistances, R_s and R_w respectively. It is estimated that latch-up can be avoided by using a substrate and well doping of the order of 10^{15} atoms per cc.

CIRCUIT EVALUATION

The circuit diagram of a CMOS inverter circuit is shown in Figure-1. The notations S_1 , G_1 , and D_1 have been used to denote the source, gate and drain of the p channel MOSFET. The subscript 2 is used for the n-channel MOSFET. The gates of the two transistors are shorted and provide the input terminal. The drains are shorted and act as the output terminal. The sources and substrate of the p-MOSFET are shorted and connected to the drain bias, V_{DD} . Likewise the source and substrate of the n-MOSFET are shorted and connected to the source supply ($-V_{SS}$).

Figure-2 shows the layered structure of a fully fabricated CMOS inverter circuit of Figure-1 using the p well structure in a silicon wafer. The symbols and notations are the same as in Figure-1. The parasitic transistors are: (1) the lateral p-n-p transistor is formed by the p^+ - source as emitter, n-substrate as base and p-well as the collector; (2) The vertical n-p-n transistor is formed by the n^+ -source (S_2) as emitter, p-well as the base and n substrate as the collector. The two transistors are interconnected as shown in Figure-2. The other two parasitic elements are the substrate resistance R_s and the well resistance R_w . The equivalent circuit of the system is shown in Figure-3. Here I_s and I_w are the currents flowing through the substrate and the well as shown in Figure-2. The current gains of the two transistors are denoted by α_{pnp} and α_{npn} . The other currents in Figure-3 are I_1 and I_2 . The drain supply voltage is ($+V_{DD}$) and source supply voltage is ($-V_{SS}$).

Using basic circuit theory it can be shown from Figure-3, that the current I flowing into the emitter of the p-n-p transistor can be given by:



$$I = \left[\frac{\left(\frac{\alpha_{npn}}{2} - 1 \right) I_{rs} + I_{CBO1} + I_{CBO2}}{1 - \alpha_{pnp} - \left(\frac{\alpha_{npn}}{2} \right)} \right]$$

Hence when $\left[\alpha_{pnp} + \left(\frac{\alpha_{npn}}{2} \right) \right]$ approaches unity, $I \rightarrow \infty$.

This is the condition for latch-up of the system.

MATHEMATICAL ANALYSIS

The mathematical analysis was performed to evaluate the magnitudes of the current gain α_{pnp} and α_{npn} for this the emitter and collector currents of the transistors were evaluated with the drain supply voltage (+V_{DD}) and (-V_{SS}) = 0V. The expressions for the emitter and collector currents for the p-n-p transistor can be given by:

$$I_E = Aq \frac{D_B P_B}{L_B} \coth\left(\frac{W}{L_B}\right) \left[\frac{(e^{qV_{EB}/kT} - 1) - 1}{\cosh\left(\frac{W}{L_B}\right)} (e^{qV_{CB}/kT} - 1) \right] + Aq \frac{D_E n_E}{L_E} (e^{qV_{EB}/kT} - 1)$$

And

$$I_E = Aq \frac{D_B P_B}{L_B} \frac{1}{\sinh\left(\frac{W}{L_B}\right)} \left[\frac{(e^{qV_{EB}/kT} - 1) - 1}{\cosh\left(\frac{W}{L_B}\right)} (e^{qV_{CB}/kT} - 1) \right] + Aq \frac{D_C n_C}{L_C} (e^{qV_{CB}/kT} - 1)$$

Where

L_B is the diffusion length of holes in the base;
L_E and L_C are the diffusion lengths in emitter and collector, respectively;

D_E, D_B and D_C are the diffusion coefficients of corresponding carriers in the emitter, base and collector, respectively;

W is the active base width;

A is the cross sectional area of the transistor;

V_{EB} is the base to emitter voltage;

V_{CB} is the collector to base voltage;

q is the electronic charge; and

P_B, n_E and n_C are the respective minority carrier concentrations in the base, emitter and collector regions, respectively.

The following sequences of calculations were used for this analysis:

- (1) The p-n-p transistor had the n region as the base which was the substrate and which was also the n region of the collector of the n-p-n transistor. Similarly the 2nd p region of the p-n-p transistor was its collector which was the p-well and was the p-base of the n-p-n transistor. If we denote substrate by (s) and well by (w) and emitter by (E), the two transistors may be denoted by the notation:

P (E)-n(s)-p (w) and n (E)-p (w)-n(s)

- (2) Calculations for IE and IC for the p-n-p transistor were performed by setting the emitter doping at 1017/CC, fixing the well doping at 1016/cc and varying the substrate doping from 1015 to 1012 by an order of 10 each time.
- (3) The drain supply voltage VDD was fixed at +5V, the source supply voltage -Vss was set equal to 0V, i.e. the source was grounded.
- (4) For not too large emitter currents, we may regard node B in Figure-3 may be regarded to be at zero volts and node A at +5V, which would give VCB of both transistors to be approximately equal to (Vbi+5)V, where Vbi is the built in potential of the collector base diode.
- (5) Depending upon the emitter-base doping levels and collector base doping levels, the built in potential Vbi was determined in each case from standard graphs [4].
- (6) The mobility values for carriers were also determined from plots of mobility versus doping concentrations.
- (7) The D values were obtained from Einstein relation

$$D = \mu \left(\frac{kT}{q} \right)$$
- (8) The value of VEB was set equal to Vbi and that for VCB = (Vbi + 5) volts.
- (9) The depletion region width at each junction was calculated and the diffusion lengths 'L' set equal to half of the depletion widths.
- (10) These values were put in equations (2) and (3) above and values of upnp and were obtained for eight doping profiles of the p-n-p transistor as quoted in item 2 above for (W/L) = 2, where W is the active base width.
- (11) This was repeated for calculating simultaneous values of anpn for the n-p-n transistor for (W/L) = 2.
- (12) The values of apnp and anpn were calculated in eight sets each for (W/L) = 2, 1.5, 1, 0.5 and 0.05.
- (13) The magnitude of $[\alpha_{pnp} + (\alpha_{npn}/2)]$ was then obtained for all values of substrate and well dopings and for five values of (W/L), i.e. from 2 to 0.05 as in (12) above.
- (14) The process was repeated for the n-p-n transistor by setting the emitter doping at 1017 per cc, fixing the substrate-doping at 1015 per cc and varying the well doping from 1016 to 1013 per cc by an order of 10 successively.
- (15) The following set of graphs was then plotted:



- I. Current gain (α_{npn} vs. Substrate-doping) for different (W/L) ratio-Figure- 4.
- II. Current gain (α_{npn} vs. Substrate-doping) for different (W/L) ratio-Figure-5.
- III. Current gain (α_{npn} vs. Well-doping) for different (W/L) ratio-Figure-6.
- IV. Current gain (α_{npn} vs. Well-doping) for different (W/L) ratio-Figure-7.
- V. $[\alpha_{pnp} + (\alpha_{npn}/2)]$ vs. Substrate-doping-Figure-8.
- VI. $[\alpha_{pnp} + (\alpha_{npn}/2)]$ vs. Well-doping-Figure-9.
- VII. (W/L) ratio vs. $[\alpha_{pnp} + (\alpha_{npn}/2)]$ for different Substrate-doping-Figure-10(a) to 10(d).
- VIII. (W/L) ratio vs. $[\alpha_{pnp} + (\alpha_{npn}/2)]$ for different Well-doping-Figure-11(a) to 11(d).

RESULTS and DISCUSSIONS

It is seen from Figures 4 and 5 that the current gains α_{pnp} and α_{npn} of the two parasitic transistors, remains fixed irrespective of the substrate-doping levels. However, these two current gains increase in magnitude as the parameter (W/L) decreases, a result that is easily understandable. However, the effect of well-doping on these current gains does show a certain level of variation (Figures 6 and 7). At low values of well doping, i.e. from 10^{13} to 10^{14} per cc the current gain remains unchanged. However, they increase with a decrease in the parameter (W/L). However, α_{pnp} increases at well doping levels in excess of 10^{15} per cc for all values of (W/L). The current gain α_{npn} decreases in this range of well doping levels. The factor $[\alpha_{pnp} + (\alpha_{npn}/2)]$ remains an invariant under varying substrate-doping (Figure-8) but decreases beyond well doping levels of 10^{14} per cc to increase again at a well doping level of 10^{16} per cc (Figure-9).

A plot of the quantity $[\alpha_{pnp} + (\alpha_{npn}/2)]$ vs. (W/L) for different values of substrate doping are shown in Figure-10(a) to Figure-10(d) It is seen that all these graphs have identical slopes and exhibit almost the same nature of variation. When $[\alpha_{pnp} + (\alpha_{npn}/2)]$ is plotted against (W/L) for different well dopings, the nature of variation is again found to be the same. This is shown in Figure-11 (a) to Figure-11(d).

DISCUSSIONS

In order to avoid latch-up it is necessary that we set restrictions on the limits of the following parameters.

- The current gains α_{pnp} and α_{npn} should be much less than 1 so that the quantity $[\alpha_{pnp} + (\alpha_{npn}/2)]$ also may have a value less than unity. We see from Figures 4 and 5 that α_{pnp} and α_{npn} remains independent of the level of substrate doping. However the well doping does alter their magnitudes and looking at the plots given in Figures 6 and 7, it is seen that these current gains show a low value for (W/L) ≤ 1 especially for well dopings of 10^{15} atoms per cc or higher. Since the well acts as the base of n-p-n transistor and collector of the pnp transistor, it is desirable to have a moderate value of well doping of 10^{15} atoms per cc.

- It is then required to set the value of (W/L). In order to keep the magnitudes of α_{pnp} and α_{npn} low we need to reduce the magnitude of (W/L) for each transistor. If the magnitude of (W/L) is increased to 2 or 1.5 then the size of the CMOS inverter would increase which would be undesirable. Moreover, values of (W/L) less than unity shows higher values of current gains. Hence, optimum value for (W/L) would be to set it equal to 1. The condition for latch-up given by the factor $[\alpha_{pnp} + (\alpha_{npn}/2)]$ is significantly less than one for (W/L) equal to one and substrate and well-dopings of 10^{15} atoms per cc each. This can be verified from Figures-8 and 9.
- The quantity $[\alpha_{pnp} + (\alpha_{npn}/2)]$ plotted against (W/L) for different substrate and well doping levels shows that for substrate and well dopings of 10^{15} per cc each the quantity $[\alpha_{pnp} + (\alpha_{npn}/2)]$ has a magnitude much less than 1 at (W/L) = 1. This is shown in Figures 10 and 11.
- Lastly, the base width of the p-n-p and n-p-n transistors is evaluated using Figure-12. Here parasitic lateral p-n-p transistor has a depletion width of x_{nBE} and x_{nBC} at the emitter/base and collector/base junctions respectively. In order to reduce collector currents we set the diffusion length in base, $L_B = 1/2 x_{nBE}$. These correspond to very short carrier lifetimes of the order of 10-5 s or less and cause a significant reduction in the collector current. For substrate and well-dopings of 10^{15} per cc each, the p-n-p transistor has $x_{pBE} = 1.12\mu\text{m}$, $x_{pBC} = 2.06\mu\text{m}$, giving $L_B = 0.56\mu\text{m}$. The active base width W being set equal to L gives $W = 0.56\mu\text{m}$ since we have chosen (W/L) to be equal to 1. The physical base width $W_{B1} = x_{nBE} + x_{pBC} + W$ is then equal to $3.74\mu\text{m}$ for the base width of the parasitic p-n-p transistor shown in Figure-12.
- Similar analysis leads to a physical base width W_{B2} of the parasitic vertical n-p-n transistor of $3.74\mu\text{m}$, which points to a well depth W_w of about $4\mu\text{m}$.
- The CMOS inverter chip dimensions using these values of W_{B1} and W_{B2} can then be estimated. These are shown in Figure-12 with numbers in microns. The width has been estimated using $W_{B1} = 3.74\mu\text{m}$ as reference using a gate width of $0.5\mu\text{m}$. These points to a chip width of 11.98 or $12\mu\text{m}$.
- The chip thickness may be estimated as follows: p + and n + regions having a depth of $0.5\mu\text{m}$, W_{B2} being $3.74\mu\text{m}$ and an additional thickness of $2.5\mu\text{m}$ beneath W_{B2} (to accommodate collector / base depletion width of n-p-n transistor) gives a total thickness of $6.74\mu\text{m}$ for the chip.

CONCLUSIONS

In conclusion it may be said that to design Silicon based CMOS inverter with line geometry of $0.5\mu\text{m}$, the following fabrication guidelines should be used so that the problem of latch-up is prevented:



- Substrate and well dopings should have doping levels of 10^{15} per cc. The p⁺ and n⁺ regions should have a doping of 10^{17} /cc each.
- The base diffusion length must be set equal to half the depletion width at the emitter-base junction of the parasitic p-n-p and n-p-n transistors.
- The (W/L) ratio should be set equal to 1.
- The CMOS inverter chip (width x thickness) can be accommodated in a cross-sectional area of (11.98 x 6.74) μm^2 , which appears to be a respectable value for these dimensions.

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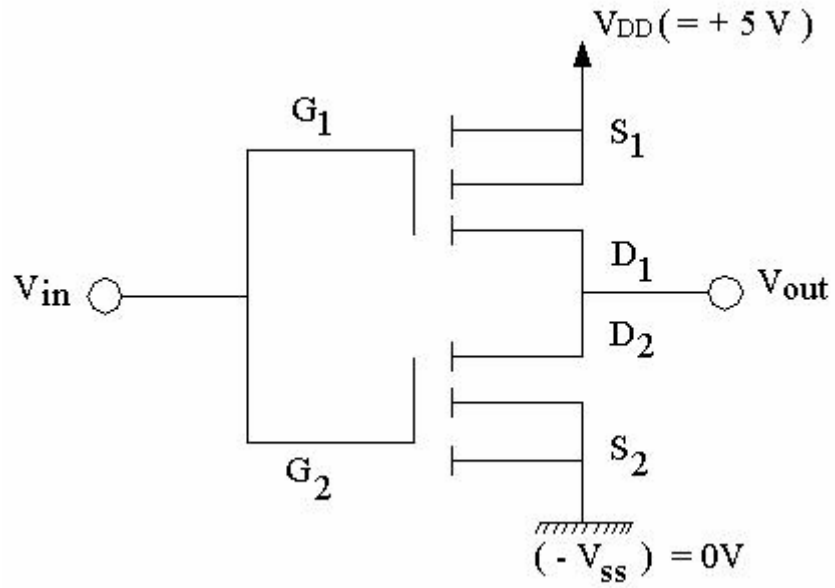


Figure-1.

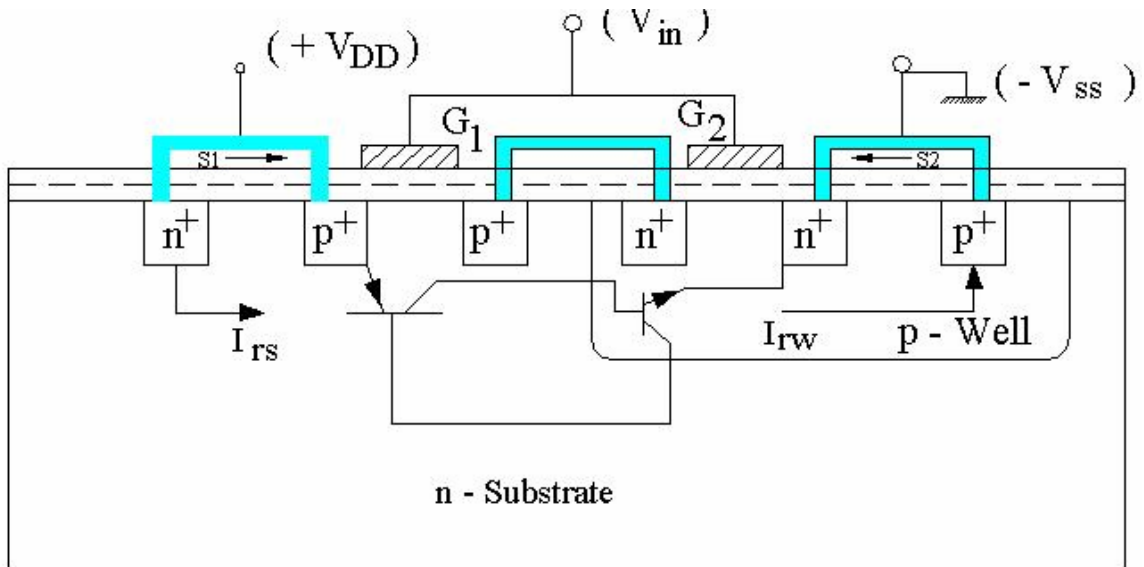


Figure-2.

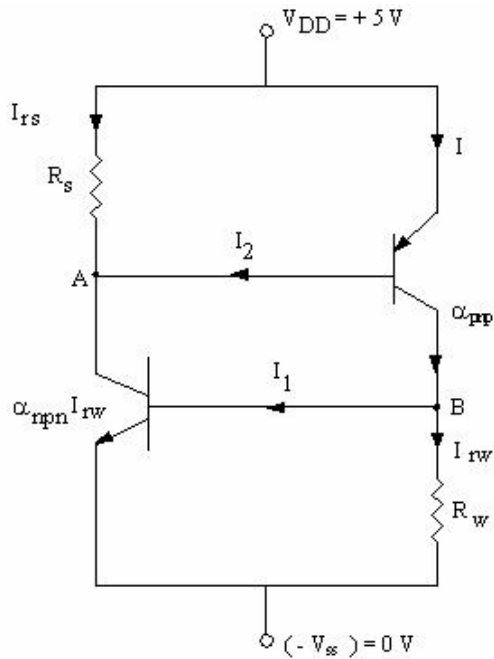


Figure-3.

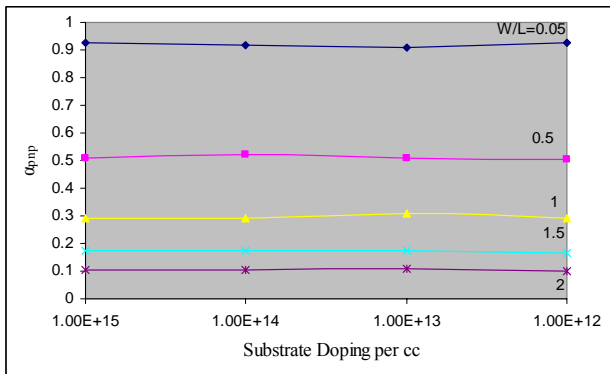


Figure-4. Current gain (α_{pnp}) vs substrate-doping for different W/L ratio.

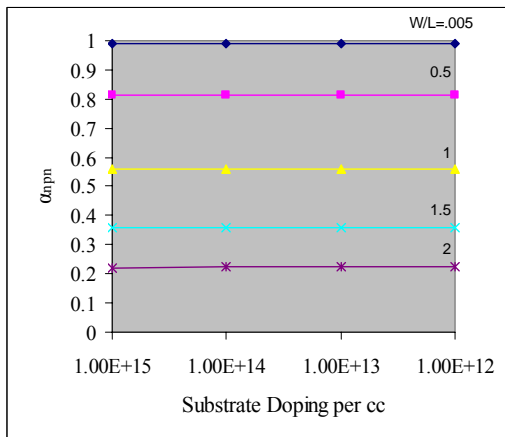


Figure-5. Current gain (α_{pnp}) vs. substrate-doping for different W/L ratio.

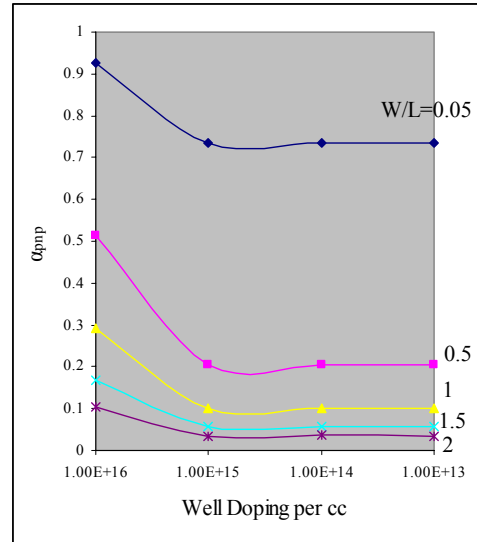


Figure-6. Current gain (α_{pnp}) vs well-doping for different W/L ratio.

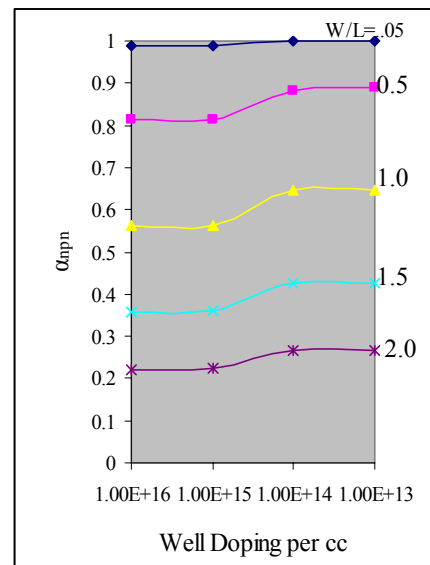


Figure-7. Current gain (α_{pnp}) vs. well-doping for different W/L ratio.

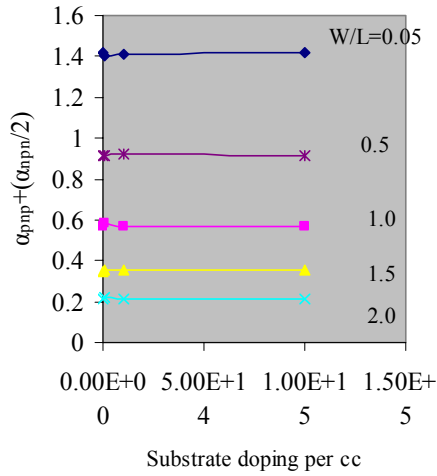


Figure-8. $[\alpha_{pnp} + \alpha_{npn}]/2$ vs substrate- doping for different W/L ratio.

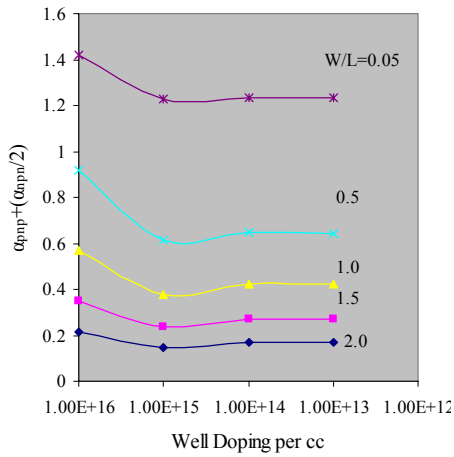
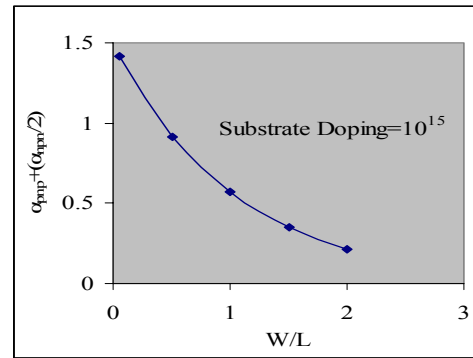
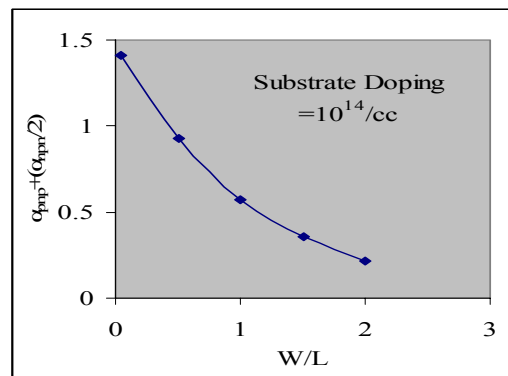


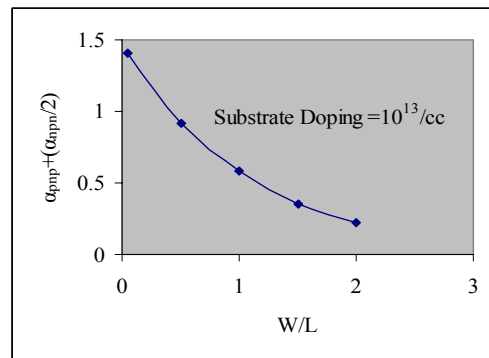
Figure-9. $[\alpha_{pnp} + \alpha_{npn}]/2$ vs. well- doping for different W/L ratio.



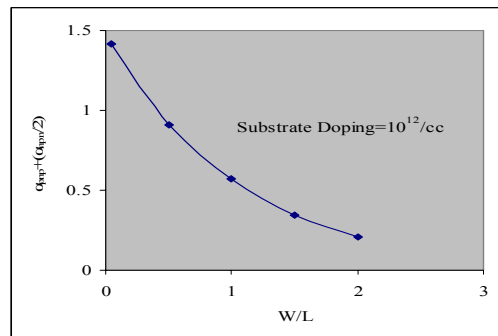
(a)



(b)

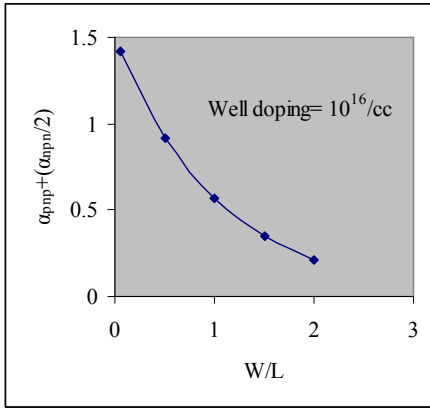


(c)

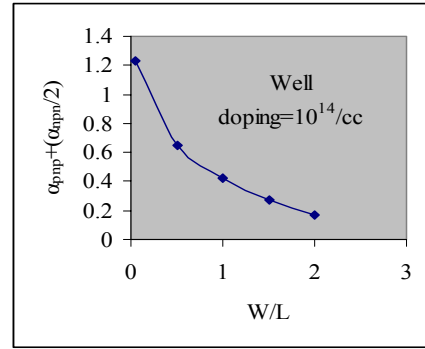


(d)

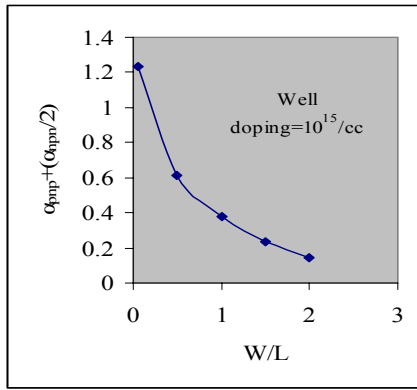
Figure 10(a)-(d). (W/L) ratio vs. $[(\alpha_{pnp}) + (\alpha_{npn})]/2$ for different substrate doping for different substrate doping.



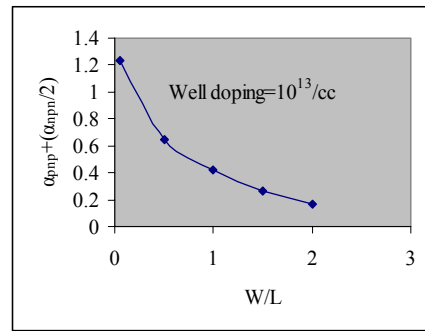
(a)



(c)



(b)



(d)

Figure 11(a)-(d). (W/L) ratio vs. $[(\alpha_{pnp}) (\alpha_{npn})/2]$ for different Well-doping.

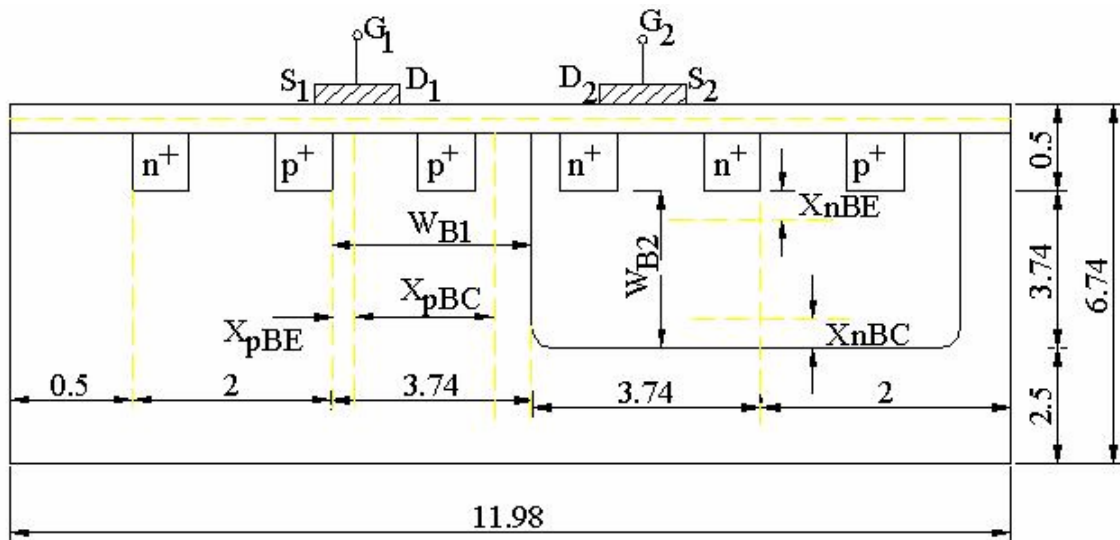


Figure-12.