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MULTICARRIER TRAPEZOIDAL PWM STRATEGIES BASED ON CONTROL FREEDOM DEGREE FOR MSMI

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ABSTRACT

This work proposes an additional clew for the carrier based PWM methods on control of multilevel inverters which is based on the combination of the Control Freedom Degree (CFD) and novel carrier/reference signals for multilevel cascaded inverter. The significance of the proposed CFD clew on multilevel PWM techniques are verified and well demonstrated by simulation for chosen five level inverter. This paper presents a novel approach for controlling the harmonics of output voltage of chosen Cascaded MultiLevel Inverter (CMLI) employing trapezoidal PWM switching strategies. Sub Harmonic PWM (SHPWM), Phase Shift PWM (PSPWM), Variable Frequency PWM (VFPWM) and Carrier Overlapping PWM (COPWM) techniques employed are evaluated for various modulation indices using spectrum of the output voltage and other performance measures such as crest factor, form factor etc and the use of inverter state redundancies to perform additional application specific control tasks. This paper focusses on MultiCarrier Trapezoidal PWM (MCTPWM) techniques with Phase Disposition (PD), Phase Shift (PS), Variable Frequency (VF) and Carrier Overlapping (CO) of carrier for the chosen CMLI. Simulations are performed using MATLAB/SIMULINK. It is observed that PD and CO methods provide output with relatively low distortion. It is also observed that CO is found to perform better since it provides relatively higher fundamental RMS output voltage and relatively lower stress on the devices.

Keywords: CMLI, THD, PWM, SHPWM, PSPWM, VFPWM, COPWM, Harmonics.

INTRODUCTION

Multilevel Voltage Source Inverter (VSI) structure is very popular especially in high power DC to AC power conversion applications. It offers several advantages that make it preferable over the conventional VSI .These include the capability to handle higher DC link voltage and improved harmonic performance. By using multilevel structure, the stress on each switching device can be reduced in proportional to the number of levels and thus the inverter can handle higher voltages. Consequently, in some applications it is possible to avoid expensive and bulky step-up transformer. Significant advantage of MLI is that several voltage levels leads to a better and more sinusoidal output voltage waveform. As a result, lower Total Harmonic Distortion (THD) is obtained. A new PWM scheme that used multiple trapezoidal modulating signals with a single triangular carrier is discussed in [1]. Multicarrier PWM methods for MLIs are extensively described in [2]. To minimize the harmonic distortion of the output of a PWM inverter, many methods based on modulation strategies have been proposed in [3]. The topologies upto five level have been proposed by Choi *et al.*, in [4]. Newton *et al.*, [5] discussed the control requirements for three and five level inverters. The idea of control degrees of freedom combination and the validity of the PWM strategies are demonstrated by simulation and experimentation of three and five level inverters by Hongyan Wang *et al.*, [6]. Chaturvedi *et al.*, [7] presented simulation studies on different control techniques for three and five level diode clamped MLI. Samir Kouro *et al.*, [8] introduced multicarrier PWM with DC-link ripple feed-forward compensation for MLI. Peng *et al.*, [9] developed a cascaded MLI for utility application. Martina Calais *et al.*, [10] investigated and analysed different multicarrier PWM methods for a single phase five level cascaded inverter. Three kinds of novel PWM methods for multilevel inverter are analysed by Yang Deng *et al.*, [11]. These methods utilized vertical offsets among carriers as the control freedom degree. Hong Yang Wu *et al.*, [12] presented a new clew for the research on carrier based PWM methods for multilevel inverter based on combinations of the control freedom degrees. The PWM techniques employed in inverters may be unipolar or bipolar type [13]. Harmonic reduction in MLI is achieved by increasing the number of staircase levels in the output. The process described by Arif Al-Judi *et al.*, [14] achieved more number of levels without the increase of number of voltage sources. This approach employed a specific switching sequence of non-equal voltage sources. Dahidah and Agelidis [15] proposed a new variation of selective harmonic elimination pulse width modulation technique suitable for a high power five level voltage source converters used in constant frequency utility application. This detailed literature survey reveals few papers only on MCTPWM and hence this work presents a novel approach for controlling the harmonics of output voltage of chosen CMLI employing trapezoidal PWM switching strategies. Simulations are performed using MATLAB/SIMULINK. Harmonic analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

MULTILEVEL INVERTER

Multilevel inverters are being considered for an increasing number of applications due to their high power capability associated with lower output harmonics and lower commutation losses. Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of AC load. Figure-1 shows a configuration of the single phase five level cascaded type Modular Structured Multilevel Inverter (MSMI). The MSMI is unique when compared to other types of multilevel inverters in the sense that it consists of several modules that require separate DC sources. Compared to other types of multilevel inverters, the MSMI requires less number of components with no extra clamping diodes or voltage balancing capacitors that only further complicate the overall inverter operation. As can be seen from Figure-1, each module of the MSMI has the same structure whereby it is represented by a single phase full-bridge inverter. This simple modular structure not only allows practically unlimited number of levels for the MSMI by stacking up the modules but also facilitates its packaging.

The operation of the MSMI can be easily understood. The load voltage is equal to the summation of the output voltage of the respective modules that are connected in series. The number of modules (M) which is equal to the number of DC sources required depends on the total number of positive, negative and zero levels (m) of the MSMI. It is usually assumed that m is odd as this would give an integer valued M. In this work, load voltage consists of five levels which include $+2V_{DC}$, $+V_{DC}$, 0, $-V_{DC}$ and $-2V_{DC}$ and the number of modules needed is 2. The following equation gives the relationship between M and m. M = (m-1)/2

The gate signals for chosen five level cascaded inverter are simulated using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index m_a and for various PWM strategies. Figure-2 shows a sample SIMULINK model developed for SHPWM method. The simulation results presented in this work in the form of the outputs of the chosen multilevel inverter are compared and evaluated.

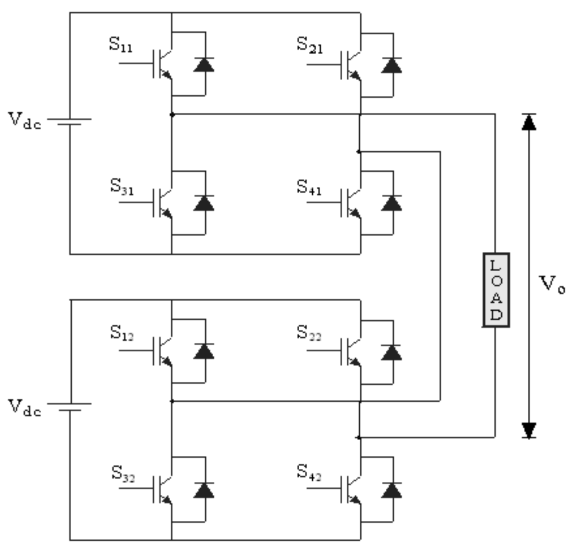

Figure-1. Five level MSMI.

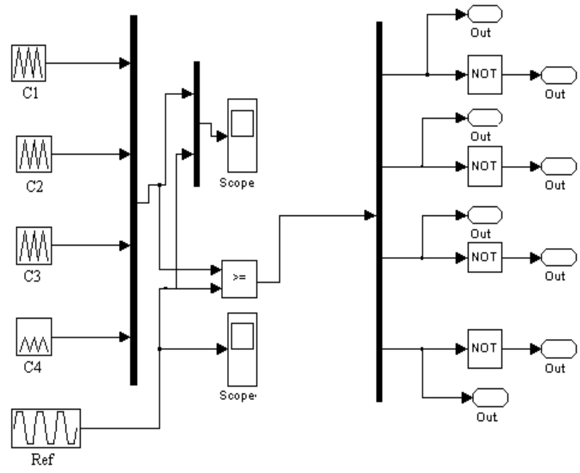

Figure-2. Sample PWM generation logic using SIMULINK model developed for SHPWM method.

CFD BASED MODULATION STRATEGIES

Carrier based PWM methods have more than one carrier that can be triangular waves or saw tooth waves and so on. As far as the particular carrier signals are concerned, there are multiple CFD including frequency, amplitude, phase of each carrier and offsets between carriers. The modulating/reference wave of multilevel carrier based PWM strategies can be sinusoidal or trapezoidal. As far as the particular reference wave is concerned, there is also multiple CFD including frequency, amplitude, phase angle of the reference wave and as in three phase circuits, the injected zero sequence signal to the reference wave. This paper focuses on multicarrier based trapezoidal PWM strategies which have been used in chosen CMLI. The following methods are employed in this study.

Sub harmonic PWM method

In SHPWM all the carriers are in phase. For an m-level inverter using bipolar multicarrier technique, (m-1) carriers with the same frequency f_c and same peak-to-peak amplitude A_c are used. The reference waveform has amplitude A_m and frequency f_m and it is centred about the zero level. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices switch off. The frequency ratio m_f is defined in the bipolar PWM strategy as follows: $m_f = f_c/f_m$ .The amplitude modulation index m_a is defined for this method as: $m_a = 2A_m/(m-1)A_c$ .The SHPWM method yields only odd harmonics for odd m_f and yields odd and even harmonics for even m_f. Figure-3 shows the multicarrier arrangement for SHPWM method for m_a = 0.8 and m_f = 22.

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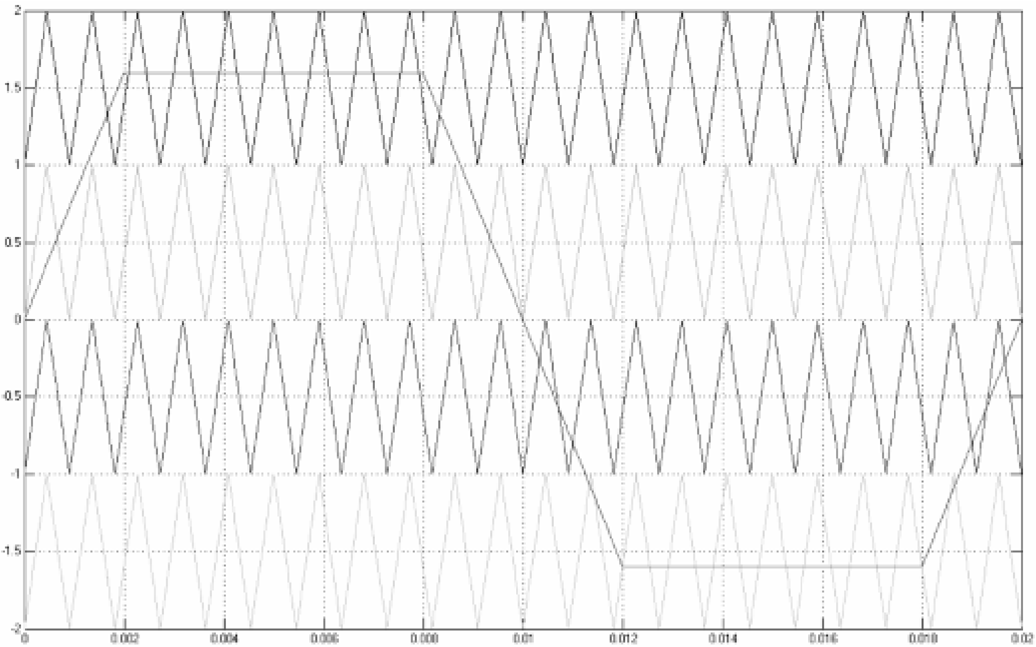

Figure-3. Multicarrier arrangement for SHPWM method.

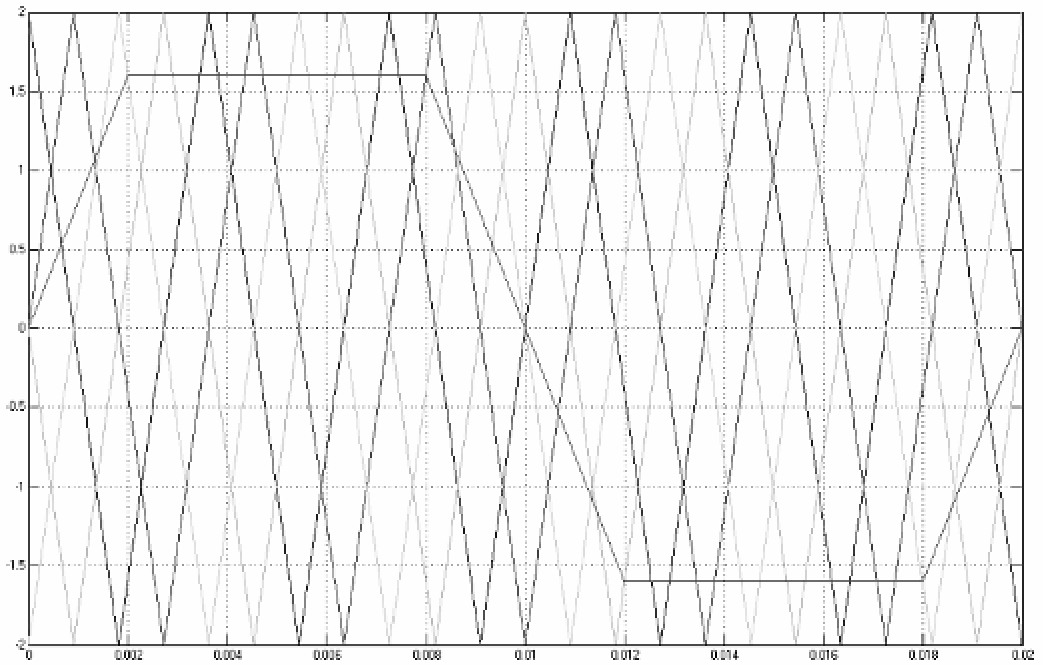

Figure-4. Multicarrier arrangement for PSPWM method.

Phase shift method

The phase shift multicarrier PWM technique uses four carrier signals of the same amplitude and frequency which are shifted by 90 degrees to one another to generate the five level inverter output voltage. The gate signals for the cascaded inverter can be derived directly from the PWM signals (comparison of the carrier with the trapezoidal reference). There is a certain degree of freedom in the allocation of the carriers to the inverter switches. In the case of sinusoidal reference (i) for odd m_f the waveforms have odd symmetry resulting in even and odd harmonics and (ii) for even m_f, PSPWM waves have quarter wave symmetry resulting in odd harmonics only. But in the case of trapezoidal reference, the waveforms have odd symmetry resulting in only odd harmonics. Figure-4 shows the multicarrier arrangement for PSPWM method for m_a = 0.8 and m_f = 22. The amplitude modulation index is defined for this strategy as: $m_a = A_m/ (A_c/2)$.

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Variable frequency PWM method

The number of switchings for upper and lower devices of chosen MLI is much more than that of intermediate switches in SHPWM using constant frequency carriers. In order to equalize the number of switchings for all the switches, variable frequency PWM strategy is used as illustrated in Figure-5 in which the carrier frequency of the intermediate switches is properly increased to balance the numbers of switching for all the switches.

The amplitude modulation index $m_a = \frac{2A_m}{(m-1)A_c}$.

Figure-5 shows the multicarrier arrangement for VFPWM method for m_a = 0.8 and m_f = 22.

Carrier overlapping PWM method

The COPWM method utilizes the CFD of vertical offsets among carriers. The principle of COPWM is to use several overlapping carriers with single modulating signal. For an m level inverter, m-1 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlap each other. The overlapping vertical distance between each carrier is $A_c/2$ in this work. The reference wave has the amplitude A_m and frequency f_m and it is centered in the middle of the carrier signals. The amplitude modulation index $m_a = \frac{A_m}{\left(\frac{m}{4}\right)A_c}$.The vertical offset of carriers for chosen five level inverter can be as illustrated in Figure-6. It can be seen that the four carriers are overlapped with other and the reference trapezoidal wave is placed at the middle of the four carriers. Figure-6 shows the multicarrier arrangement for COPWM method for m_a = 0.8 and m_f = 22.

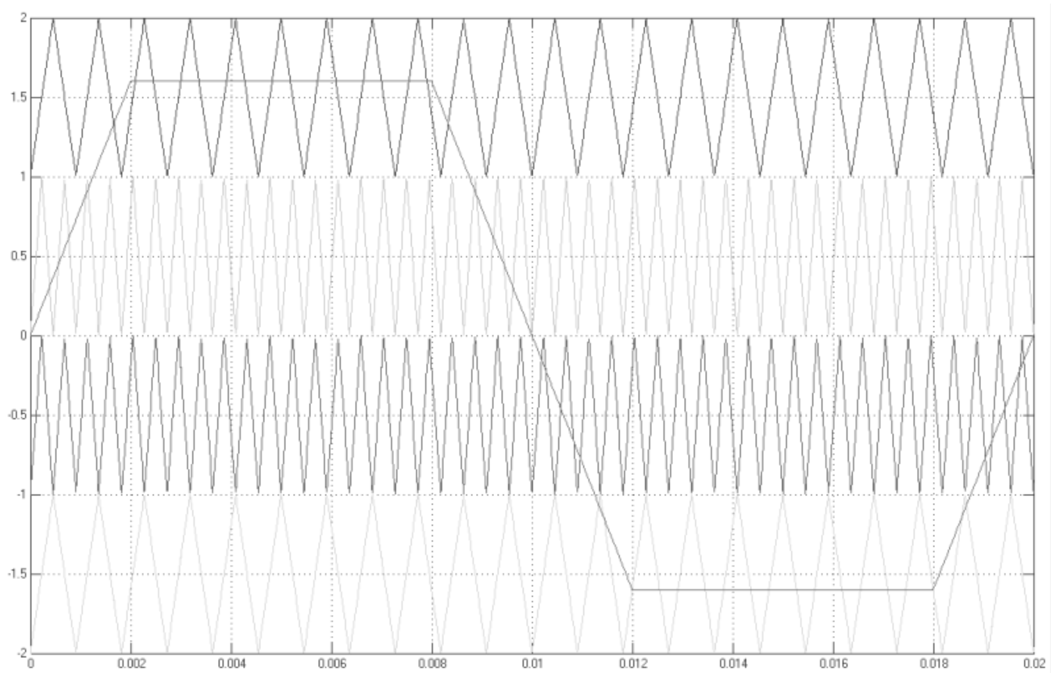

Figure-5. Multicarrier arrangement for VFPWM method.

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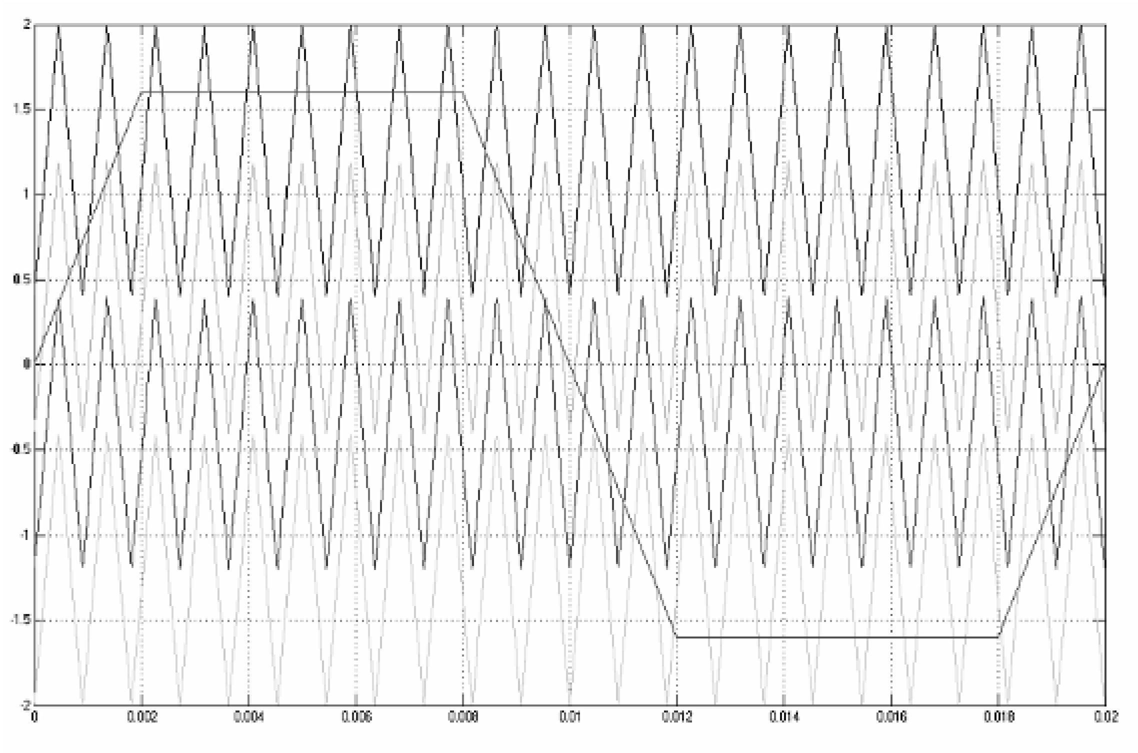

Figure-6. Multicarrier arrangement for COPWM method.

In this paper, m_f = 22 and m_a is varied from 0.6 to 1.m_f is chosen as 22 as a trade off in view of the following reasons: (i) to reduce switching losses (which may be high at large m_f) (ii) to reduce the size of the filter needed for closed loop control, the filter size being moderate at moderate frequencies.

SIMULATION RESULTS

The cascaded five level inverter is modelled in SIMULINK using Power System block set. Switching signals for MSMI are developed using bipolar PWM techniques discussed previously. Simulations are performed for different values of m_a ranging from 0.6 - 1. The corresponding %THD values are measured using the FFT block and they are shown in Table-1. Next Table displays the V_{rms} of fundamental of inverter output for same modulation indices. Tables 3-5 display respectively the corresponding crest factor, distortion factor and form factor. Figures 7-14 show the simulated output voltage of MSMI and corresponding FFT plots with above strategies but for only one sample value of m_a = 0.8. Figure-7 shows the five level output voltage generated by SHPWM strategy and its FFT plot is shown in Figure-8. From Figure-8 it is observed that the SHPWM strategy produces significant 3^{rd}, 7^{th}, 8^{th}, and 20^{th} harmonic energy. Figure-9 shows the five level output voltage generated by PSPWM strategy and its FFT plot is shown in Figure-10. From Figure-10, PSPWM strategy has significant amount of harmonic energy present in 3^{rd}, 7^{th}, 13^{th}, 15^{th} and 17^{th} harmonics. Figure-11 displays the five level output voltage generated by COPWM strategy and its FFT plot is shown in Figure-12. The FFT spectrum of COPWM strategy shows significant 3^{rd}, 7^{th}, 18^{th} and 20^{th} harmonic energy content in the inverter output. Figure-13 shows the five level output of VFPWM strategy where significant energy is present in the 3^{rd} and 20^{th} harmonics. The following parameter values are used for simulation: V_{DC} =100V and R (load) = 100 ohms.

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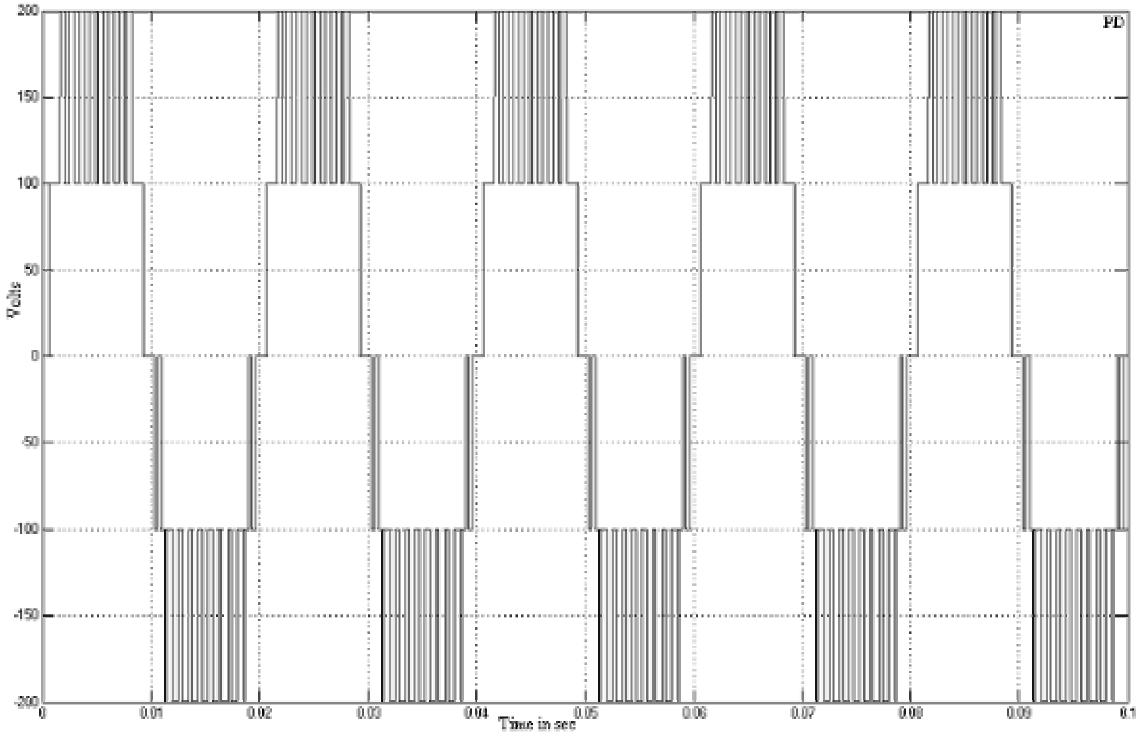

Figure-7. Output voltage generated by SHPWM method.

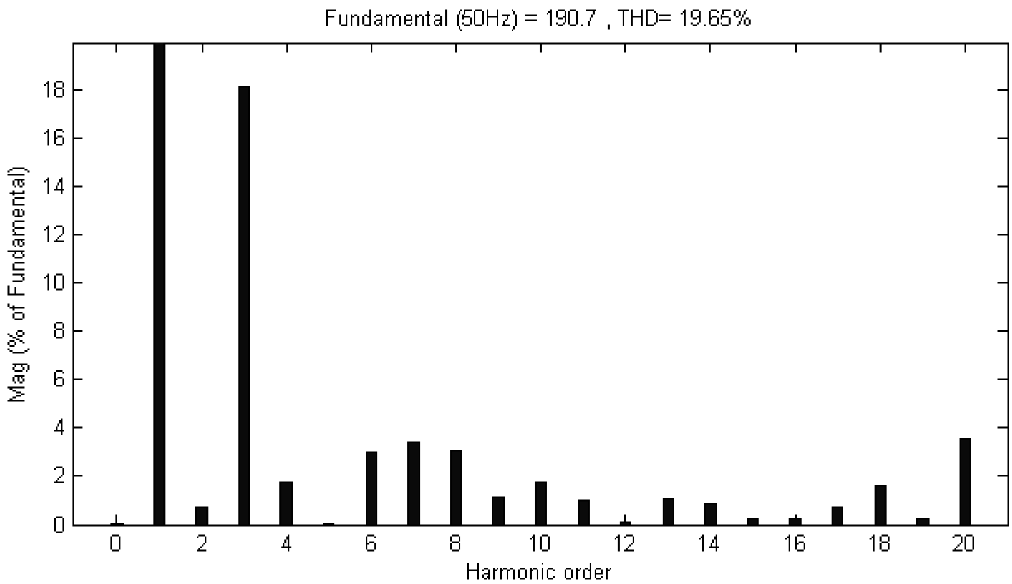

Figure-8. FFT plot for output voltage of SHPWM method.

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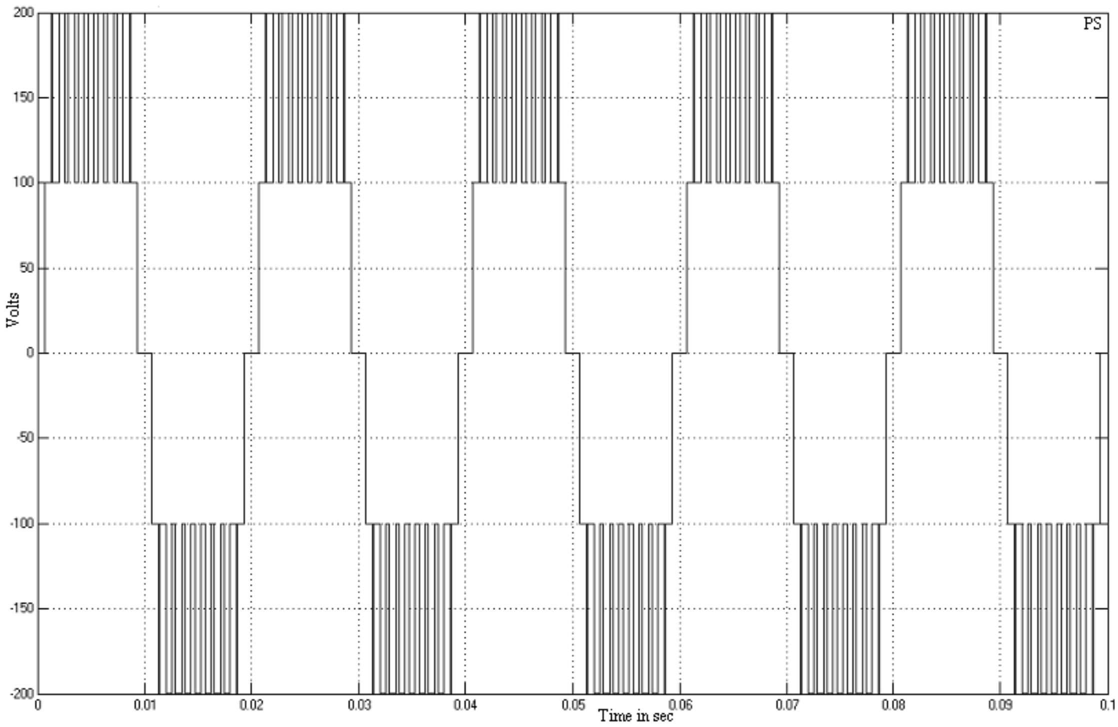

Figure-9. Output voltage generated by PSPWM method.

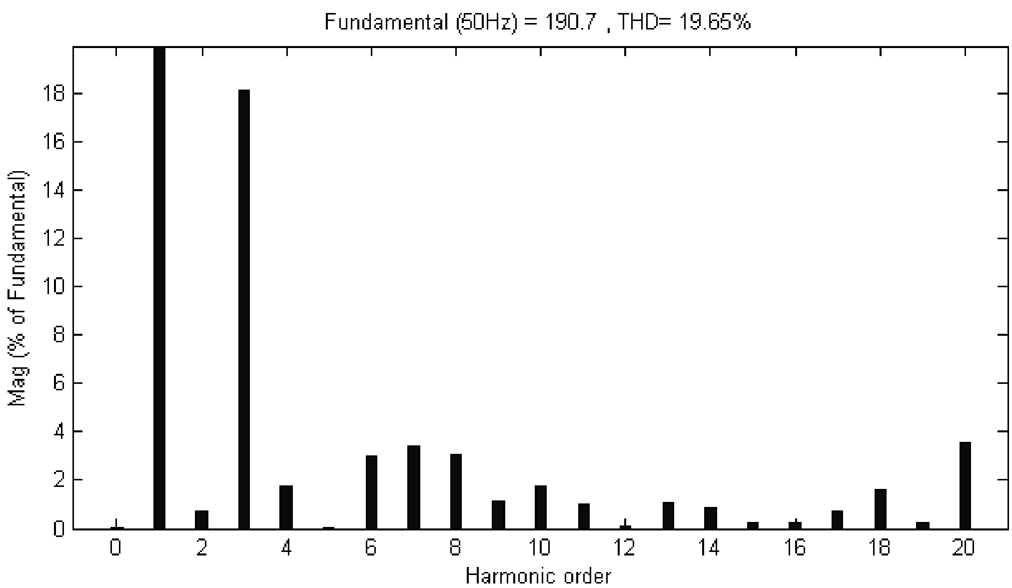

Figure-10. FFT plot for output voltage of PSPWM method.

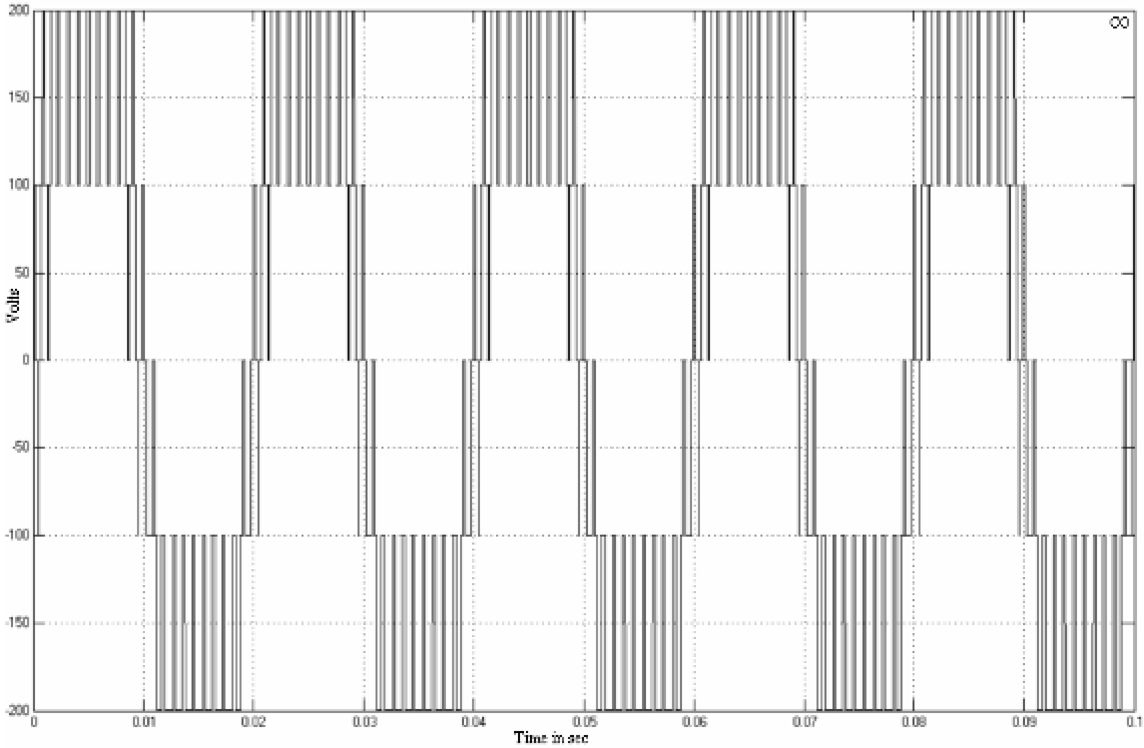

Figure-11. Output voltage generated by COPWM method.

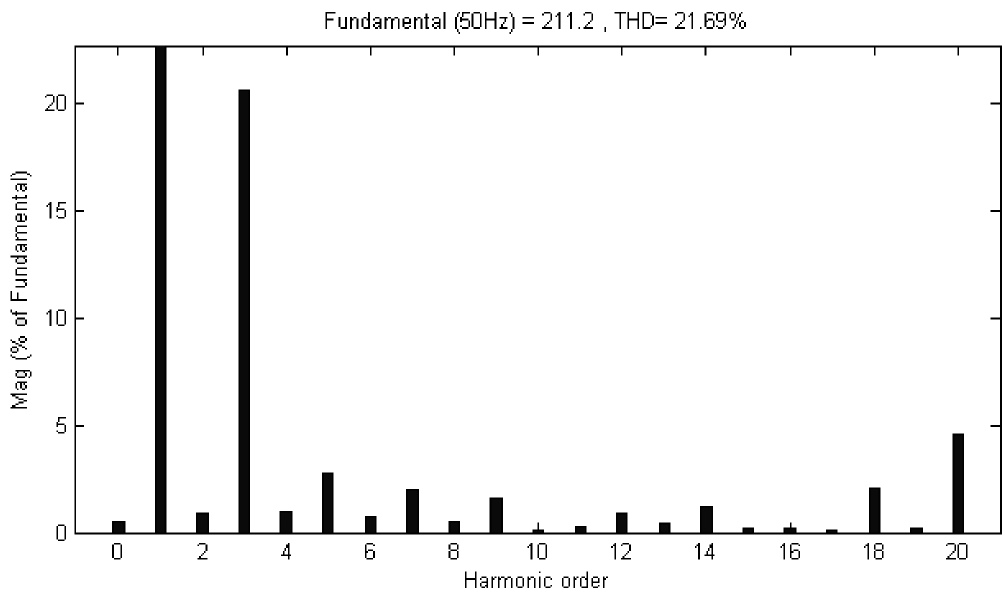

Figure-12. FFT plot for output voltage of COPWM method.

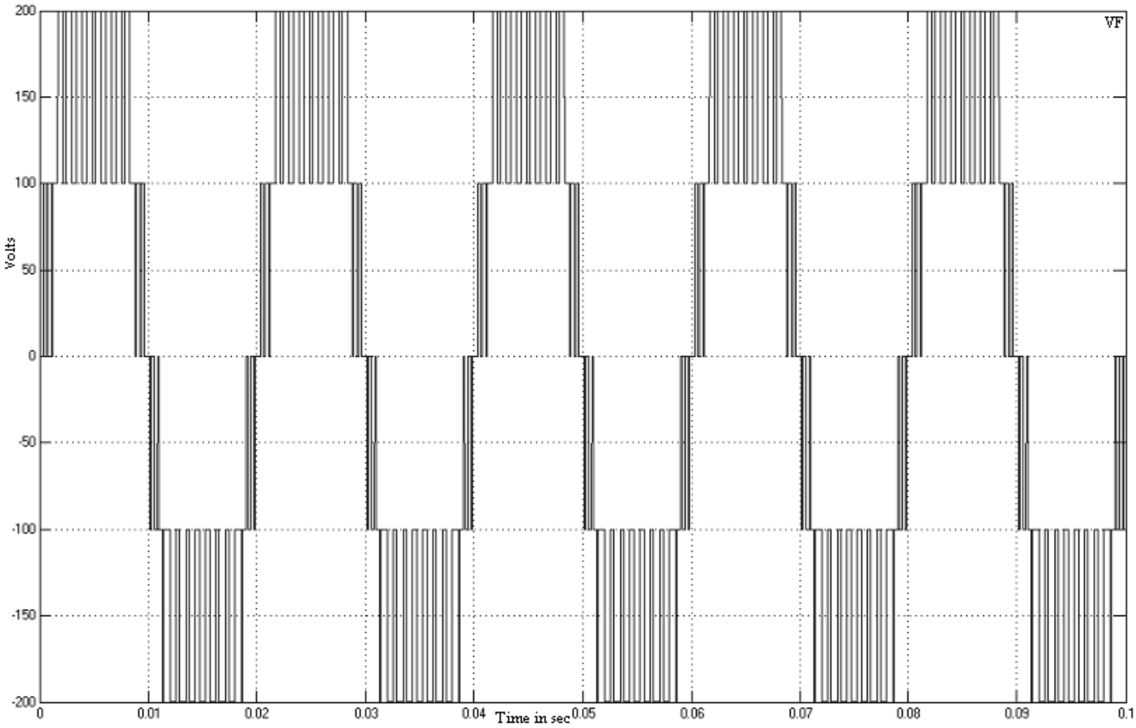

Figure-13. Output voltage generated by VFPWM method.

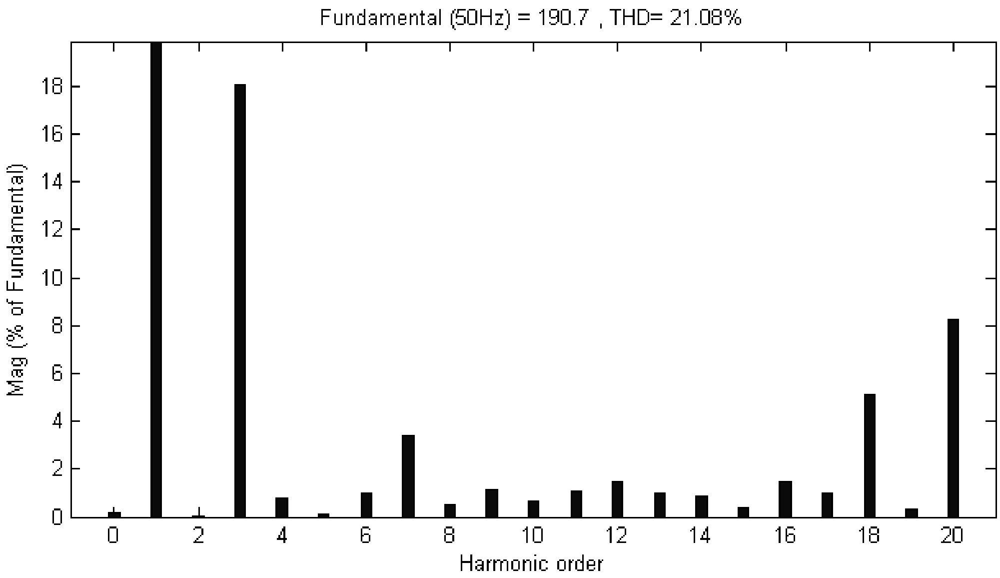

Figure-14. FFT plot for output voltage of VFPWM method.

Table-1. % THD for different modulation indices.

m_a	PD	PS	CO	VF
1	19.38	20.05	24.15	19.16
0.9	18.60	20.29	22.93	19.43
0.8	19.65	21.61	21.69	21.08
0.7	20.09	22.86	20.06	21.73
0.6	19.48	23.92	19	20.64

Table-2. VRMS (fundamental) for different modulation indices.

m_a	PD	PS	CO	VF
1	168.2	168.3	171.1	168.4
0.9	151.4	151.5	160.4	151.5
0.8	134.8	134.7	149.3	134.8
0.7	118	117.8	138.1	117.8
0.6	101	101	126.5	101.3

Table-3. Crest factor for different modulation indices.

m_a	PD	PS	CO	VF
1	1.167	1.165	1.136	1.944
0.9	1.299	1.294	1.215	1.944
0.8	1.456	1.451	1.309	1.938
0.7	1.661	1.655	1.418	1.935
0.6	1.944	1.925	1.552	1.939

Table-4. Distortion factor for different modulation indices.

m_a	PD	PS	CO	VF
1	0.021	0.020	0.024	0.019
0.9	0.020	0.020	0.024	0.020
0.8	0.020	0.020	0.020	0.020
0.7	0.020	0.019	0.022	0.019
0.6	0.020	0.019	0.020	0.020

Table-5. Form factor for different modulation indices.

m_a	PD	PS	CO	VF
1	272	8580	391	286
0.9	244	7729	222	3857
0.8	INF	INF	294	689
0.7	262	2014	1175	263
0.6	169	3462	INF	794

CONCULSIONS

It is observed from Table-1 that SHPWM and COPWM methods provide output with relative low distortion. Of the four strategies developed, COPWM is found to perform better since it provides relatively higher fundamental RMS output voltage (Table-2) and relatively lower stress on the devices (Table-3).

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