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DESIGN OF A MODEL OF MODERN VARIABLE RELUCTANCE TACHOGENERATOR (ELECTROMAGNETIC SENSOR) FOR MEASURING ANGULAR VELOCITY OF A ROTATING SHAFT USING FREQUENCY TO DIGITAL CONVERSION TECHNIQUES

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ABSTRACT

The objective of this research is to design a model of modern Variable Reluctance Tachogenerator (electromagnetic sensor) for measuring angular velocity of a rotating shaft using frequency to digital conversion techniques. The method used in this design is an adaptation of standard Tachogenerator design although the design utilized reasonable number of slots (60) in a disc, NE 572 as a special comparator and bubble resolver. These improved the sensitivity, speed and eliminate ±1 error that is inherent in most digital systems, respectively. The model was tested with a DC motor; and was able to measured angular velocity ranging from 100-1000rpm with their corresponding frequencies 16Hz -160Hz. The model is capable of measuring angular velocity of other device that the speed of revolution is not more than 10,000 rpm.

Keywords: model, tachogenerator, angular velocity measurement, frequency, bubbles resolver, digital conversion.

INTRODUCTION

In the modern days technology digital electronic instruments are preferred instead of analogue instruments, the use of digital instruments minimizes loading effects, reduce electrical noise and easy to read. Variable Reluctance Tachogenerator are generally used to measure angular velocity of a rotating shaft for example, the shaft could be rotor of motors, generators or other mechanical device. Tachogenerator are of different types; electronic, eddy - current and impulse. In this work electronic type is chosen because of its speed of operation, ease with which the display is read, its high accuracy and those basically consist of transducers, which converts the speed of rotation of the shaft into electrical signal. For it to work satisfactorily it must satisfy the following requirements such as variation in ambient temperature should have negligible effect on the Tachogenerator output (Website 2004a), the rectified output voltage should be strictly linear with respect to rotational speed and the ripple content in the rectified output signal must be as low as possible (Smith, 2007). Although the accuracy of the measurement of the angular velocity of the shaft depends on the uniform speed measured over a long period of time (Efedua, 2004). The method used in designing these components values is an adaptation of the standard Variable Reluctance Tachogenerator design only that the design improved on some existing problems by replacing comparator UA741 with NE 527 because of its fast response, 60 slots were used in the disc to improved the sensitivity and bubble resolver was included in the circuit to eliminate ±1 error that is inherent in most digital systems (Ali, 2006 and Ofua, 2004, Zakaria, 2009). Variable Reluctance Tachogenerator are hardly used by Nigerian industries accept in an area where they becomes indispensible this now prompted the emergence of this design. The aim of this work is to design and develop a model of Tachogenerator that will eliminate the deficiencies in the existing circuit of Tachogenerator and also to make it readily available in Nigerian market like any other digital instruments.

MATERIALS AND METHODS

Materials

The major components used in this design are special comparator (NE 527), Time base (555 timers), Disc with 60 slots, Photo detector (transistor) and Infra-red light emitting diode (IR-LED) (Data book, 2004). NE 527 was chosen instead of UA741 because it is a very fast response device and it slew at several thousand volts per micro second (Ofua, 2004); the time base was chosen because of it versatility and general-purpose in nature (Onuu *et al*., 2006); 60 slots were chosen to improve the sensitivity of the instrument instead of 15 or 30 slots that are more generally used in Variable Reluctance Tachogenerator (Ali, 2006 and Ofua, 2004) and the IR-LED was chosen because of its high efficiency, favorable wave and low power dissipation (Huagan, 2008); the photo detector was chosen because of its amplification factor, it amplifies small value of current from IR-LED to a sizable amount of current (Zheludev, 2007).

Other components like diode indicator, counters, decoders, differentiator and bubble resolver were chosen base on certain desirable characteristics they posses, availability, low cost and easy to maintain. The design, construction and the testing of the model was carried out in electronic Laboratory University of Benin, Nigeria in the year 2006.

Component design

The model consists of the following stages: power supply (two integrated circuit regulator), infra-red,

transmitter (photo diode), receiver circuit (photo detector), comparator, time base (crystal oscillator), control logic (differentiator) and n-bit binary counters as depicted in (Figure-1).

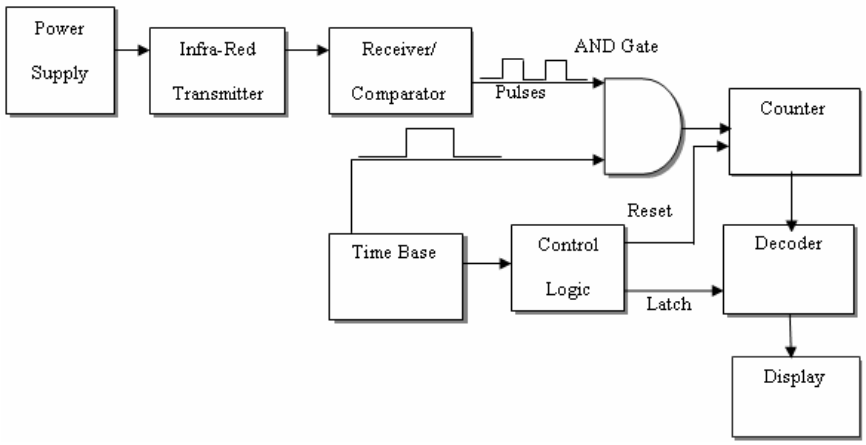

Figure-1. Block diagram of a variable reluctance tachogenerator.

Power supply unit

The power supply consist of step down transformer with input 240V, two rectifier stages, filter and regulator as shown in (Figure-2).

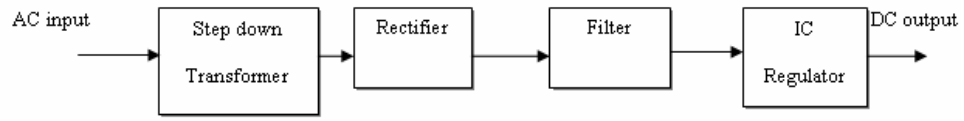

Figure-2. Block diagram of a power supply.

The step down transformer receives 240V a.c signal from source voltage and converts it to 12V d.c, the 12V is further send to rectifier circuit that rectify the d.c voltage, the ripple content of the d.c is then filtered and send to the IC regulator for smoothing, which is suitable for the operation of the circuit of the variable Reluctance Tachogenerator.

Step down transformer

The power rating of the dc transformer was determined as P = 4.8W, Eq. (1)

$$P = IV \quad (1)$$

While the primary current was obtained as $I_P = 27mA$, using Eq. (2).

$$I_P V_P = I_S V_S \quad (2)$$

Where V_P is the voltage of the primary winding, I_s is the secondary current of the secondary winding and V_S is the secondary voltage (Onohaebi *et al.*, 2006 and Thomas, 2004).

Rectifier stage

A full wave bridge rectifier was used to convert the step down transformer secondary voltage in to DC due to clipping and damping action of the diodes, a pulsating DC Voltage (ripple) is produce (Edward, 1976). In rectification, both the peak inverse voltage (PIV) and the current carrying capacity of the diode should be known; for a good design PIV and the forward current rating (I_F) must be at 2 to 3 times the input voltage and input current (Gary, 1974). The PIV diode was computed as PIV = 36V from Eq. (3) given by

$$PIV = 3V_S \quad (3)$$

i.e., V_S is the secondary voltage of the transformer (Robert, 2004), while the forward current was obtained as; $I_F = 1.5A$, using Eq. (4)

$$I_F = 3I_S \quad (4)$$

Filter stage

In order to have a steady or nearly pure DC voltage, a filter capacitor and voltage regulator is needed. The peak voltage rating of the capacitor used in this design was obtained as, $V_{Peak} = 17.04V$ from Eq. (5)

$$V_{Peak} = V_{m\sqrt{2}} \quad (5)$$

i.e., V_m is the peak secondary AC voltage (Mahta *et al.*, 2007), while the capacitor voltage rating was determined as $V_{cap} = 25V$. From Eq. (6)

$$V_{Cap} = 2V_{m\sqrt{2}} \quad (6)$$

And the capacitor rating from the ripple voltage analysis was computed as; V_r = 2.5V, from Eq. (7) given by

$$V_r = \frac{I_0}{2fC} \quad (7)$$

Where V_r is the ripple voltage; I_0 = DC current; f=main frequency and C = capacitance of a capacitor (Mahta, *et at*., 2007). From Eq. (8), the capacitance of the capacitor was also computed as C = 2200μF

Regulator stage

The value of the resistor (R_2) was obtained as R = 2Ω from Eq. (8), given by

$$V_{out} = V_{ref} = \left(1 + \frac{R_2}{R_1}\right) \quad (8)$$

V_{out} = output voltage and V_{ref} = reference voltage of the regulator, respectively (Donald *et al*., 1989)

Fuse protection

The purpose of using fuse in this design is to protect the input from excessive current drain when the main voltage goes high thereby protecting the circuit and transformer from being destroyed easily. The maximum primary current was determined as $I_{P\,(max)}$ = 0.288A using Eq. (9)

$$I_{p(Max)} = \frac{V_{in}}{R_P} \quad (9)$$

Where V_{IN} = input voltage (main voltage) and R_p=primary resistance (Mahta *et al*., 2007) usually ($I_P \geq I_{(Max)}$), so the fuse will burn thereby disconnecting the power to the transformer.

Infra-red transmitter stage

The infra red source was derived by the use of infra red light emitting diode, the LED was operated at current of I_d = 30mA, using Eq. (10) given by

$$I_d = \frac{V_{cc} - V_d}{R_3} \quad (10)$$

Where V_d is the diode drop (Ronald, 2004).

Comparator/infrared sensor stage

The comparator/infrared sensor circuit is shown in (Figure-6). Thus value of R_4 was obtained as 400Ω applying voltage divider to the comparator/infrared sensor circuit.

$$V_{ref} = \frac{R_4}{R_4 + R_5} V_{cc} \quad (11)$$

Where V = reference voltage at the non inverting terminal of the comparator chosen as 10V. When the infra light is interrupted the photo detector does not conduct then $V_{in} \approx V_{cc}$, the comparator tends to saturate at $-V_{cc}$ but the comparator is grounded, hence it goes down to zero volt. When the infrared light is not interrupted, V_{ref} becomes greater than V_{IN} ($V_{ref} > V_{in}$) and the comparator saturates at $+V_{cc}$ (Tokhein, 2003 and Ron, 2001). The diode at the output of the comparator indicates any time a clock pulse comes.

Control logic circuit

The control logic circuit is also shown in Figure-6; the control logic used in this design is a short time differentiator with short time constant given by;

$$\tau = R_9 C_4 \quad (12)$$

ț is the short time constant (Ronald, 2004) and the time constant was obtained as = 660ms from Eq. (12), the logic circuit is also used for resetting the signal any time the pulse is counted, the wave form such behavior is shown in Figure-3.

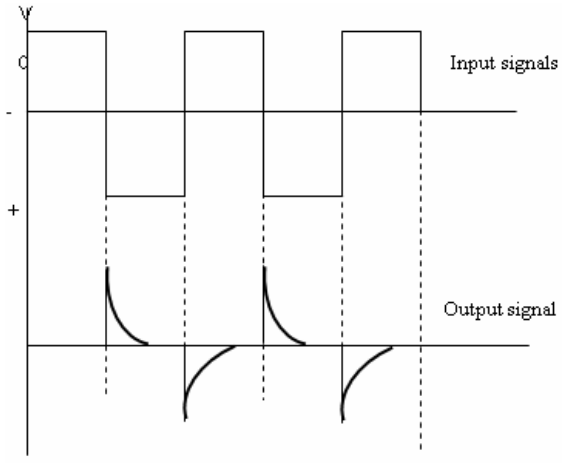

Figure-3. Wave form of control logic.

How D flip-flop eliminate bubbles

The circuit of the bubble resolver is shown Figure-6 as 4013A; the bubble resolver is use in the design as a synchronizer. The synchronizer's function is to remove or eliminate the ±1 counting error that is inherent in Tachogenerator circuit. The output of the AND gate does not come ON until the first clock arrives at the clock point of the D flip flop with the time base gating pulse, it opens when both pulses are HIGH and continuous until gating pulse from time base goes away (LOW), thus locks the measured interval (gating pulse) to the event signal pulse being measured and eliminate the bubble. The AND gate receive the output of the D flip flop (Morris, 2002). The wave form is shown in Figure-4.

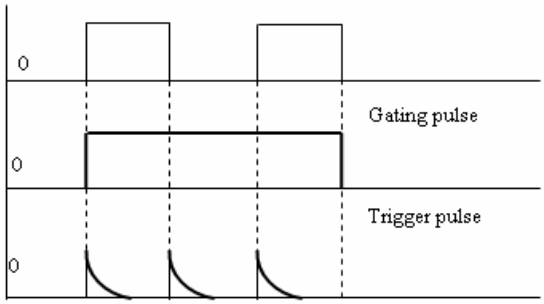

Figure-4. Wave forms of D flip flop.

Time base stage

The time base circuit is also shown in Figure-6; is use in this design as astable multi vibrator to generate a gating pulse of constant time duration of 1s. The capacitor C_1 charges towards the external resistor R_9 and R_{10}. The capacitor rises until it goes to 2/3 V_0 this the threshold voltage at pin 6 which drives the comparator to trigger the D flip flop causing the output at pin 7 to discharge the capacitor through R_{10}. The wave form of such behavior is shown in Figure-5.

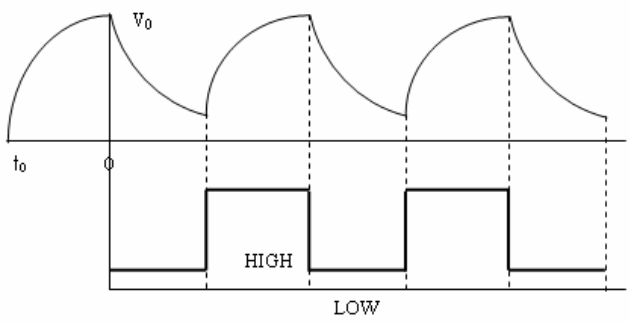

Figure-5. Astable response wave form.

The period required to charge the capacitor is given by

$$T_1 = 0.7(R_7 + R_8)C_1 \quad (13)$$

Where the period required to discharged the capacitor completely was obtained as 10ms from Eq. (14)

$$T_2 = 0.7R_8C_1 \quad (14)$$

The total time required to charge up and discharge the capacitor was computed as 1.001s from Eq. (15)

$$T = T_1 + T_2 \quad (15)$$

The frequency of oscillation was determined as f_0=0.999Hz from Eq. (16) given by

$$f_0 = \frac{1}{T} \quad (16)$$

Where T_1, T_2. and f_0 are the charging, discharging time and frequency of oscillation of the capacitor respectively (Ronald, 2004 and Williamson, 2005).

Disc design

The disc is made of plastic materials with 60 slots which allow the infra red light to pass through it, so that the light strikes on the photo detector base.

Let K be the speed in rpm; the number of slots determine the number of pulse likewise the frequency, therefore

$$k * 60 \text{ per minute, mean that}$$

$$\frac{60k}{60} = \frac{k}{1}, \text{since } 1\text{min} = 60s \quad (17)$$

This means that in every 1s a clock pulse and a gating pulse would come to the input of the D flip flop.

AND gate

The circuit has a single output and has two or three inputs, if both the input source coming from the bubble resolver and the comparator are high the in build diode will cause the output to be equal the input voltage plus the drop across the diode. Then the output will be at logic 1, if and only if the inputs are at logic 1. Otherwise the output will be at logic 0. The electronic symbolic diagram is shown in Figure-6. The truth Table of the AND gate operation is shown in Table-1.

Table-1. Truth Table of the AND gate.

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Mode of operation of the model of the variable reluctance tachogenerator

When the system is switch ON, the IR-LED emit light that passes through the slots in the disc, if the IR light strikes the photo detector base the photo detector conducts and offers low resistance at the non inverting terminal of the comparator, the comparator then compares the low voltage at the non inverting terminal with the fixed reference voltage at the inverting terminal to generate a HIGH (1) pulse at the output of the comparator. When the light does not strikes the photo detector base it does not conducts, offers high resistance at the non inverting terminal of the comparator; the comparator also compare the high voltage at the non inverting terminal with fixed reference voltage to generates a LOW (0) pulse at the output of the comparator. The time base generates a gating pulse of constant time duration of 1s which serves as the means of opening and closing the gates for trains of the pulses at the output of the comparator to pass through the AND gate. These trains of pulses are received by the n-binary counters processed and display the data.

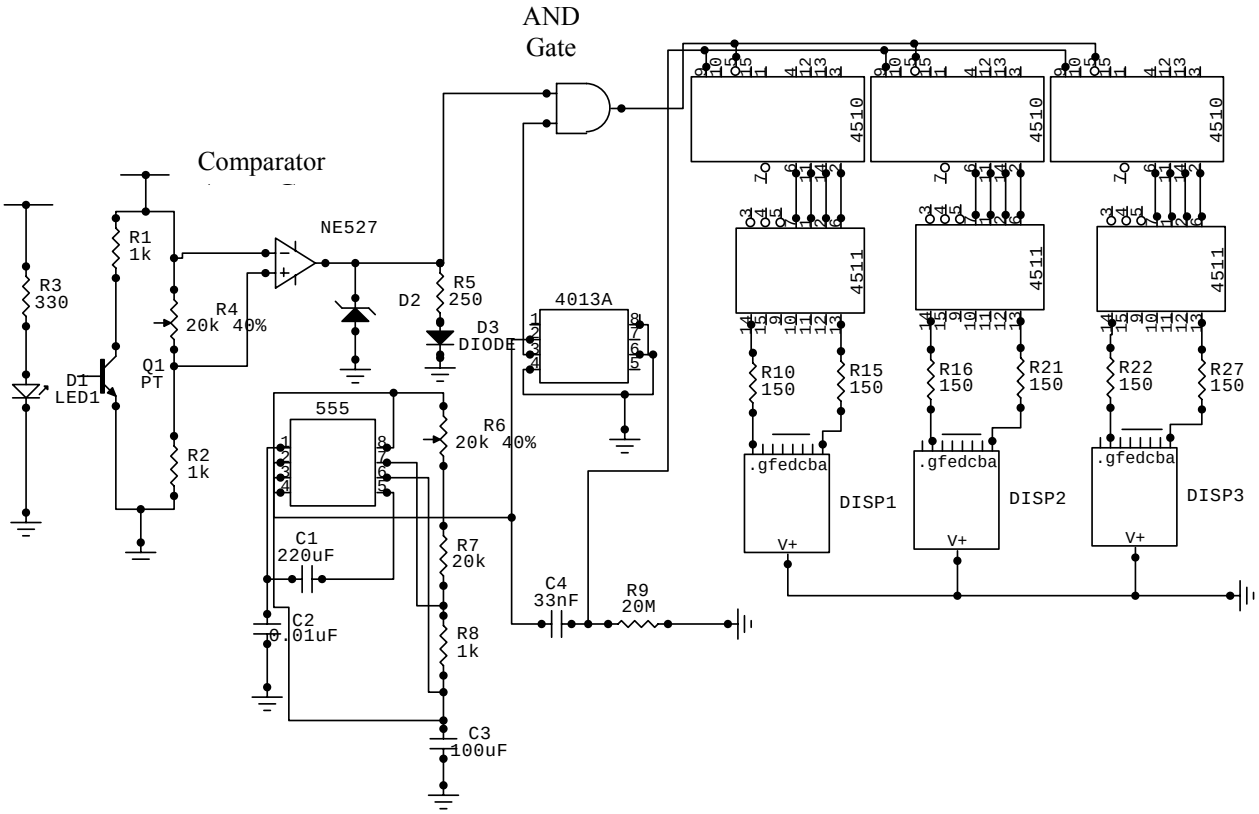

Figure-6. Circuit diagram of a variable reluctance tachogenerator.

PERFORMANCE TEST, RESULTS AND DISCUSSIONS

The time base unit was calibrated to give precisely gating pulse of 1s, the signal generator in the laboratory was set to a frequency of 16Hz (square wave) and the gating pulse was adjusted with the help of the variable resistor (R_6) in the time base unit until it gave a reading of 100rpm, to further confirm the accuracy of the calibration, the frequency was increase to 500Hz and the Tachogenerator gave a reading of 2000rpm, then some certain test were carried out at an interval of 16Hz as shown in Table-2 Which described fully the relationship between the angular speed (rpm) and the frequency in (Hz) as the frequency increases the speed also increases.

Most of the previous circuits of the Tachogenerator that we have seen in existence were deficient in the following areas; such as poor sensitivity or low efficiency, digital counting error of plus or minus 1. In most of the designs the number of slots in the disc is between 15 to 30 slots (Ali, 2006, Ofua, 2004, Zaria, 2008 and Website 2004a), this work improved the sensitivity by increasing the number of slots in the disc to 60 slots, the design also introduced a bubble resolver to eliminate the digital counting error of plus or minus one (1).

Table-2. Speed in (rpm) and the corresponding frequencies (Hz) or pulse per second.

Test	**Speed** (ω) in rpm	**Frequency** (f) in Hz
1	100	16
2	200	32
3	300	48
4	400	64
5	500	80
6	600	96
7	700	112
8	800	128
9	900	144
10	1000	160

This design used the CMDS version of integrated circuits throughout because mixing it up with other family of integrated circuits like in other designs could cause poor performance efficiency because it will definitely requires an interface which would be another design problem to check intensively. The ECL and the TTL logic families were avoided completely because of incompatibility with the CMDs circuitry.

Figure-3, described the operation of the control logic circuit. If we apply a constantly charging signal such square wave type signal to the input of the control logic the resultant output signal will be charged and

whose final shape is strictly dependent upon the value of C_4 and R_9 as shown in Figure-3 which is time constant of the combination of Resistor/capacitor.

Figure-4, explains how the D flip flop operates, the D flip flop tracks the input, making transitions with the match those of the input D. The D flip flop has only input if there is a HIGH on the D input when the clock pulse is applied, the flip flop SETs and stores 1 as HIGH. If there is a Low on the D input when the clock pulse is applied, the flip flop RESETs and stores a 0 as LOW as shown in Figure-4.

Figure-5, described the operation of the time base, the output V_0 the capacitor C_1 is charged by current flowing through R_7 and R_8. The threshold and trigger inputs monitor the capacitor (C_1) voltage and its reaches 2/3 V_0 (Threshold Voltage) the output becomes LOW and the discharge pin is connected to 0. The C_1 now discharges with the current flowing through R_8 into the discharge pin. When the voltage fall to $1/3V_0$ (Trigger Voltage) the output becomes HIGH again and the discharge pin is disconnected, allowing C_1 to start charging again. This cycle repeats continuously unless the RESET input is connected to 0V which forces the output low while the reset is 0V.

From the design despite a lot of assumption and approximation made, the design of Tachogenerator was achieved successfully the circuit is functional cheap and easy to maintain.

CONCLUSIONS

The design of the Variable Reluctance Tachogenerator for measuring angular velocity of the shaft using frequency to digital conversion techniques was achieved despite a lot of assumptions and approximations, the design improved the efficiency of the exiting circuit in the market by replacing the comparator UA 741 with NE 527, increased the number of slots in the disc to 60 slots instead of the known 15-30 slots and bubble resolver is included in the circuit to eliminate ±1 error that is inherent in most digital systems. This model is capable of measuring angular velocity of shaft although is hardly used by Nigerian industry accept in an area where they come indispensible; if this is develop by our local industries in Nigeria in no distant time Tachogenerator will be available in the market as other digital instruments.

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