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OPTIMUM SPACE VECTOR PWM ALGORITHM FOR THREE-LEVEL INVERTER

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ABSTRACT

A Three-Level Voltage Source Inverter is used increasingly to supply a variable frequency and variable voltage for variable speed applications. A suitable pulse width modulation technique is employed to obtain the required output voltage at the line side of the inverter. This paper studies popular multi-level topology, Diode Clamped or Neutral Point Clamped for three-level. Two methods of Sine-triangle and two methods of Space Vector Pulse Width Modulation are employed to generate the modulation wave. These modulation waves are compared against a triangular carrier to generate the PWM signals for the three phases. In SVPWM methods, a revolving reference voltage vector is provided as voltage reference instead of three phase modulating waves used in SPWM. The magnitude and frequency of the fundamental component in the line side are controlled by the magnitude and frequency, respectively, of the reference vector. Space Vector Modulation Technique has become the important PWM technique for three phase Voltage Source Inverters because of its increased dc bus utilization and reduced harmonic distortion compared to SPWM. The four PWM methods are simulated in MATLAB/SIMULINK software and are compared for THD and Capacitor Balance. Programs are carried out using Embedded Editor functions and Matlab editor functions. The simulation study reveals that Space vector PWM utilizes dc bus voltage more effectively, generates less THD and improved capacitor balance when compared to Sine PWM.

Keywords: Space Vector PWM, SPWM, three-level inverter, diode clamped inverter, capacitor balance, total harmonic distortion.

INTRODUCTION

Increased power demand in power electronics industry urge development in power handling capacity of semiconductor devices. In spite of that, it is a constraint to make use a single power semiconductor device in medium and high power applications, since the maximum voltage supported remains an obstacle. Three-level pulse-width modulation (PWM) voltage-source inverters (VSI) are the converters of choice for many high-power applications such as medium-voltage motor drives both in industrial and other applications. Figure-1 shows the most popular type of three-level inverters, the three-phase diode clamped or neutral-point-clamped voltage source inverter [1-8]. Compared with conventional two-level inverters, a three-level inverter has several favorable features of blocking the dc link voltage to half thus reduce the voltage stress on switching devices to half, lower common mode voltage steps, low output voltage harmonic and current ripple for the same switching frequency in addition to the capability of handling higher voltages.

As shown in Figure-1, each leg in three-level inverter is constituted by four controllable switches with two clamping diodes. Two equal capacitors splits the DC bus voltage into three voltage levels +E/2, 0, -E/2 thus the name 3-level. Clamping diodes blocks the reverse voltage of the capacitor and provide connection to the neutral point. The three states available with a single leg are in Table-1 [9]. The complementary switch pairs are (S_{i1}, S_{i1}') and (S_{i2}, S_{i2}') where i is the phase indicator (i = a, b, c). V_{io} is the voltage between phase and fictive mid-point of the dc link.

Table-1. Three-level inverter switch states

State/Switch	Si1	Si2	Si1'	Si2'	Vio
1	ON	ON	OFF	OFF	E/2
0	OFF	ON	ON	OFF	0
-1	OFF	OFF	ON	ON	-E/2

In NPC inverters, maintaining the voltage balance between the capacitors is important for proper operation of the topology.

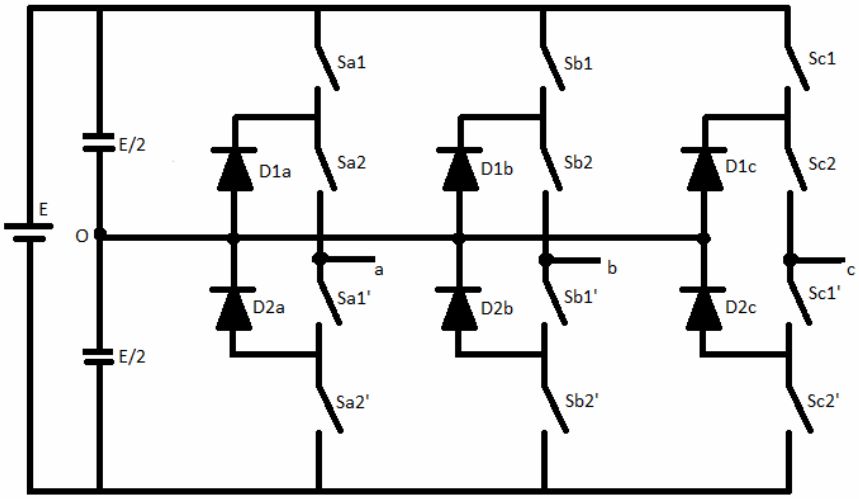

Figure-1. Three-level inverter.

PWM strategies not only address the primary issues viz, low THD, effective dc bus voltage utilization etc but also take care of secondary issues like EMI reduction, switching loss, better spreading of harmonics over the spectrum. PWM generation methods can be broadly classified into Sine-Triangle carrier PWM (SPWM) and Space Vector based PWM (SVPWM) [10-12].

SPWM considers two methods, General Common Mode SPWM (GCMSPWM) and Modified Common Mode (MCMSPWM).

In SVPWM, two methods based on the concept of three hexagons (SVPWM-3H) and four regions (SVPWM-4R) are modeled and compared [2-8]. Bus Clamped technique is used in SVPWM-3H, when reference vector revolves in Hexagon 2 to reduce the THD.

Simulation software Matlab/Simulink is used for simulation studies. The programs are carried out using Matlab Embedded Functions and Embedded Matlab Editor Functions. The theoretically studied three-level inverter is simulated for open loop and for a balanced three phase voltage system.

SINE-TRIANGLE CARRIER PWM

In sine-triangle carrier modulation each phase reference voltage is compared with two identically shaped but offset triangle carrier waveforms. Many techniques have been proposed for sine-triangle carrier modulation: Unipolar in Phase Disposition carriers, Unipolar Phase Opposition Disposition carriers and Bipolar carrier Phase Disposition [10-12]. The switching frequency is the frequency of the carriers, and their amplitude is related to the dc-link voltage. As shown in Figure-2 when the reference voltage Vr of a phase is greater than the positive carrier Va1, the phase switches to positive link; when Vr is less than negative carrier Va2, it switches to negative link; otherwise, it switches to the dc-link neutral.

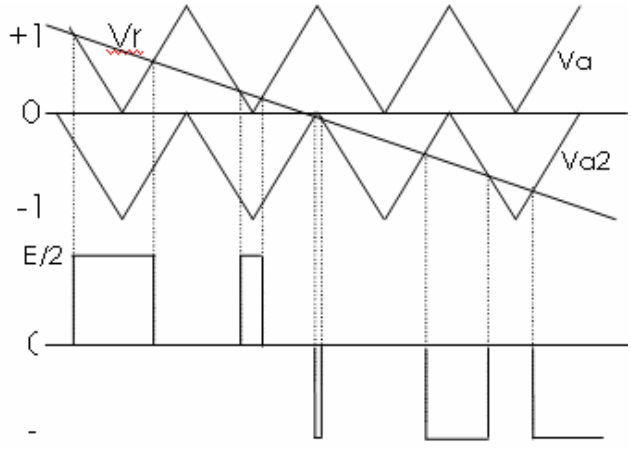

Figure-2. Sine-carrier PWM and pulses.

GCMSPWM

In multilevel inverters, based on the modulation index (m) defined in (1), modulator takes different shapes. For high modulation index of 0.866, intermediate outer triangles (region 3 of all six sectors Figure-11) are not traversed, resulting in a waveform, very similar to that of a two-level centered space-vector modulator. As modulation index decreases to less than 0.866, the waveforms look very different, unique of the three-level behavior.

The centered space-vector modulation injects a particular common-mode harmonic function into balanced three-phase voltage reference. This common-mode injection can be obtained through (2).

$$m = \frac{A_m}{(n-1)A_c} \quad (1)$$

'n' the level of the inverter.

$V_1cm = -1/2(Max(V_1in) + Min(V_1in))$; I = a, b, c (2)

MCMSPWM

Function (2) is sufficient for m = 0.866, the same as the two-level case; for m<0.866, the common mode

takes different functions at different instants of time as shown in Table-2 [4].

Table-2. Three-level common mode function.

Condition	CM
$Mid < 0$ and $(Max - Min) < 1$	$\frac{Min}{2}$
$Mid > 0$ & $(Max - Min) < 1$	$\frac{Max}{2}$
$Mid < 0$ $(Max - Min) > 1$ $(1 - Max) > -Mid$	$-\frac{1 - Max}{2}$
$Mid > 0$ $(Max - Min) > 1$ $(1 + Min) > Mid$	$-\frac{1 + Min}{2}$
others	$-\frac{Max + Min}{2}$

Generated modulation signals are compared against two triangular carriers to generate PWM pulses for the three phases. The frequency of the carrier signal is very high compared to the modulating signal. The magnitude and frequency of the fundamental component in the line side are controlled by changing the magnitude and frequency of the modulating signal. Linear control is available between 0% and 78.5% of six step voltage values, which results in poor voltage utilization. Available maximum fundamental component improvement with reduced harmonics is obtained through SVPWM.

SPACE VECTOR PWM

Space Vector PWM (SVPWM) method is an intensive advanced computation PWM method and possibly the best technique for variable frequency application.

In SVPWM method, the voltage reference is provided using a revolving reference vector. In this case magnitude and frequency of the fundamental component in the line side are controlled by the magnitude and frequency, respectively, of the reference voltage vector. Space vector modulation utilizes dc bus voltage more efficiently and generates less harmonic distortion in a three phase voltage source inverter.

Mathematical modeling of SVPWM

The revolving voltage reference vector is obtained assuming a balanced set of voltages (3)

$$\begin{aligned} v_{an} &= V_m . \sin \omega t \\ v_{bn} &= V_m . \sin\left(\omega t - 2\pi/3\right) \\ v_{cn} &= V_m . \sin\left(\omega t - 4\pi/3\right) \end{aligned} \quad (3)$$

Three phase reference voltages are transformed into diphase α-β components by Clark's transformation (4).

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \quad (4)$$

$$V_{ref} = \sqrt{(V_\alpha)^2 + (V_\beta)^2} \; ; \; \theta = \tan^{-1}\left(V_\beta / V_\alpha\right) \quad (5)$$

Where è is the angle varies from 0 to 2ð.

Amplitude and angle of the reference vector are found from (5).

Table-3 shows the three states of three legs of the three-level inverter shown in Figure-1. From Table-1, the pole voltages are shown for $3^3 = 27$ space vectors in Table-3. Pole voltages are related to phase voltages by (6).

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -\frac{1}{3} \\ -\frac{1}{3} & 2/3 & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & 2/3 \end{bmatrix} \cdot \begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} \quad (6)$$

Calculated corresponding phase voltages, di-phase voltages and the magnitude of the reference voltage vector Vref are obtained from (6), (4) and (5) and are shown in Table-3. Sa, Sb and Sc are the states of the three legs of the three level inverter. S_{a1}, S_{a2}, S_{b1}, S_{b2}, S_{c1} and S_{c2} are the switches of the upper leg of the three phases and S_{a1}', S_{a2}', S_{b1}', S_{b2}', S_{c1}' and S_{c2}' are the complementary switches that constitute the lower leg of the three phases a, b and c respectively shown in Figure-1.

Table-3. Three-level inverter's 27 States and output voltages.

Sa	Sb	Sc	Sa1	Sa2	Sb1	Sb2	Sc1	Sc2	Va0	Vb0	Vc0	Van	Vbn	Vcn	Vá	Vâ	Vres	Vv	Sn
0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	V0	1
1	0	0	1	1	0	1	0	1	E/2	0	0	E/3	-E/6	-E/6	E/√6	0	E/√6	V11	2
0	-1	-1	0	1	0	0	0	0	0	-E/2	-E/2	E/3	-E/6	-E/6	E/√6	0	E/√6	V12	3
1	1	0	1	1	1	1	0	1	E/2	E/2	0	E/6	E/6	-E/3	E/√24	E/√8	E/√6	V21	4
0	0	-1	0	1	0	1	0	0	0	0	-E/2	E/6	E/6	-E/3	E/√24	E/√8	E/√6	V21	5
0	1	0	0	1	1	1	0	1	0	E/2	0	-E/6	E/3	-E/6	-E/√24	E/√8	E/√6	V31	6
-1	0	-1	0	0	0	1	0	0	-E/2	0	-E/2	-E/6	E/3	-E/6	-E/√24	E/√8	E/√6	V32	7
0	1	1	0	1	1	1	1	1	0	E/2	E/2	-E/3	E/6	E/6	-E/√6	0	E/√6	V41	8
-1	0	0	0	0	0	1	0	1	E/2	0	0	-E/3	E/6	E/6	-E/√6	0	E/√6	V42	9
0	0	1	0	1	0	1	1	1	0	0	E/2	-E/6	-E/6	E/3	-E/√24	-E/√8	E/√6	V51	10
-1	-1	0	0	0	0	0	0	1	-E/2	-E/2	0	-E/6	-E/6	E/3	-E/√24	-E/√8	E/√6	V52	11
1	0	1	1	1	0	1	1	1	E/2	0	E/2	E/6	-E/3	E/6	E/√24	-E/√8	E/√6	V61	12
0	-1	0	0	1	0	0	0	1	0	-E/2	0	E/6	-E/3	E/6	E/√24	-E/√8	E/√6	V62	13
1	1	1	1	1	1	1	1	1	E/2	E/2	E/2	0	0	0	0	0	0	V7	14
1	0	-1	1	1	0	1	0	0	E/2	0	-E/2	E/2	0	-E/2	E.√3/√8	E/√8	E/√2	V8	15
0	1	-1	0	1	1	1	0	0	0	E/2	-E/2	0	E/2	-E/2	0	E/√8	E/√2	V9	16
-1	1	0	0	0	1	1	0	1	-E/2	E/2	0	-E/2	E/2	0	-E√3/√8	E/√8	E/√2	V10	17
-1	0	1	0	0	0	1	1	1	-E/2	0	E/2	-E/2	0	E/2	-E√3/√8	-E/√8	E/√2	V11	18
0	-1	1	0	1	0	0	1	1	0	-E/2	E/2	0	-E/2	E/2	0	-E/√2	E/√2	V12	19
1	-1	0	1	1	0	0	0	1	E/2	-E/2	0	E/2	-E/2	0	E.√3/√8	-E/√8	E/√2	V13	20
-1	-1	-1	0	0	0	0	0	0	-E/2	-E/2	-E/2	0	0	0	0	0	0	V14	21
1	-1	-1	1	1	0	0	0	0	E/2	-E/2	-E/2	2E/3	-E/3	-E/3	E.√2/√3	0	E√2/√3	V15	22
1	1	-1	1	1	1	1	0	0	E/2	E/2	-E/2	E/3	E/3	-2E/3	E/√6	E/√2	E√2/√3	V16	23
-1	1	-1	0	0	0	1	0	0	-E/2	E/2	-E/2	-E/3	2E/3	-E/3	-E/√6	E/√2	E√2/√3	V17	24
-1	1	1	0	0	1	1	1	1	-E/2	E/2	E/2	-2E/3	E/3	E/3	-E√2/√3	0	E√2/√3	V18	25
-1	-1	1	0	0	0	0	1	1	-E/2	-E/2	E/2	-E/3	-E/3	-2E/3	-E/√6	-E/√2	E√2/√3	V19	26
1	-1	1	1	1	0	0	1	1	E/2	-E/2	E/2	E/3	-2E/3	E/3	E/√6	-E/√2	E√2/√3	V20	27

The 27 state space vectors of three-level inverter are shown in Figure-4 and Table-3. According to magnitude the 27 voltage vectors are categorized into four groups: Zero vectors (ZV), Small Vectors (SV), Medium Vectors (MV) and Large Vectors (LV).

- Zero vectors are (000), (111), and (-1-1-1) at the origin, connecting the output to zero potential point thus producing a voltage or current amplitude of zero.
- Small vectors are double vectors and are again subdivided into Upper and Lower small vectors. The six vectors (100), (110), (010), (011), (001), (101) are Upper Small Vectors (USV) and (0-1-1), (00-1), (-10-1), (-100), (-1-10), (0-10) are the six Lower Small Vectors (LSV) with equal magnitude of E/√6. These vectors connect the ac outputs to two consecutive DC-link voltage levels. The pair of vectors that produce same voltage are (100, 0-1-1), (110, 00-1), (010,-10-1), (011,-100), (001,-1-10) and (101, 0-10).
- Medium vectors are (10-1), (01-1), (-110), (-101), (0-11), and (1-10) have the magnitude of E/√2. The length of these vectors defines the maximum amplitude of the reference vector for linear modulation and steady-state conditions, which is √3/2 the length of the large vectors. These vectors produce voltage imbalances in the capacitors and thus must be compensated.
- Large vectors are (1-1-1), (11-1), (-11-1), (-111), (-1-11), and (1-11).These vectors generate highest ac voltage with magnitude E.√2/3. In fact, these six vectors are equivalent to six active two-level vectors.

SVPWM-3H

In this the concept of three-hexagon (3H) is utilized in generation of pulses. Three-level inverter

shown in Figure-3 is defined by three hexagons with 18 sectors: Hexagon 1, 2 and 3 [1].

Hexagon 1 (Figure-3a) consists of six sectors a, b, c, d, e and f. The vectors in this hexagon are $\vec{V}_{11}$, $\vec{V}_{21}$, $\vec{V}_{31}$, $\vec{V}_{41}$, $\vec{V}_{51}$, and $\vec{V}_{61}$ are Upper Small Vectors and $\vec{V}_{12}$, $\vec{V}_{22}$, $\vec{V}_{32}$, $\vec{V}_{42}$, $\vec{V}_{52}$, and $\vec{V}_{62}$ are Lower Small Vectors and their magnitude (Table-3) is limited to E/√6, half of the magnitude of the vector in Hexagon 3.

Hexagon 2 (Figure-3b) consists of six sectors g, h, I, j, k and l with six medium vectors. The vectors in this hexagon are$\vec{V}_{8}$, $\vec{V}_{9}$, $\vec{V}_{10}$, $\vec{V}_{11}$, $\vec{V}_{12}$, and $\vec{V}_{13}$. From Table-3 the magnitude of these vectors is E/√2.

Hexagon 3 (Figure-3c) consists of six sectors m, n, p, q, r and s with six large vectors. The vectors in this hexagon are$\vec{V}_{15}$,$\vec{V}_{16}$,$\vec{V}_{17}$,$\vec{V}_{18}$,$\vec{V}_{19}$, and $\vec{V}_{20}$, have the magnitude of E.√2/3 (Table-3).

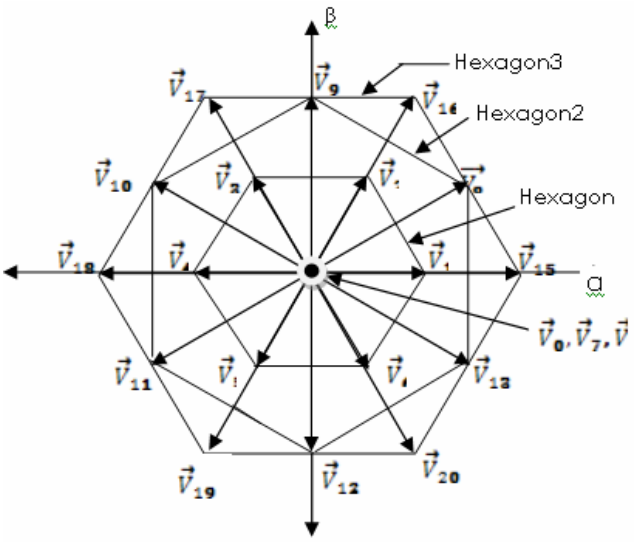

Figure-3. Three-level inverter space vectors.

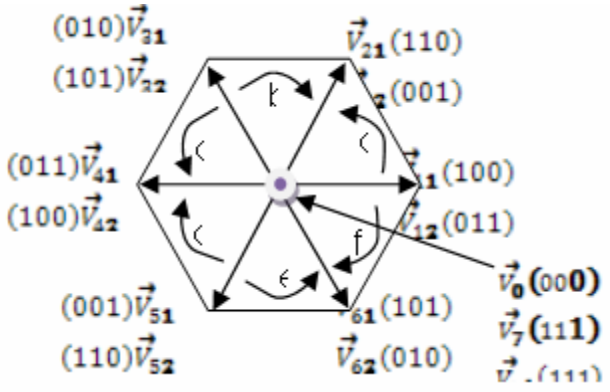

Figure-3(a). Hexagon1 space vectors.

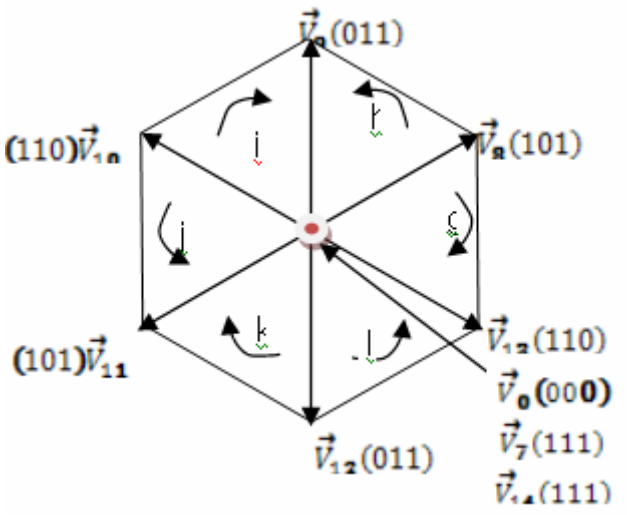

Figure-3(b). Hexagon 2 state space vectors.

Gating pulse generation

The reference vector Vref is located in any one of the 18 sectors (each of 60 degrees) from 3 hexagons, where each sector is limited by any two adjacent vectors V_λ and $V_{\lambda+1}$ as shown in Figure-4.

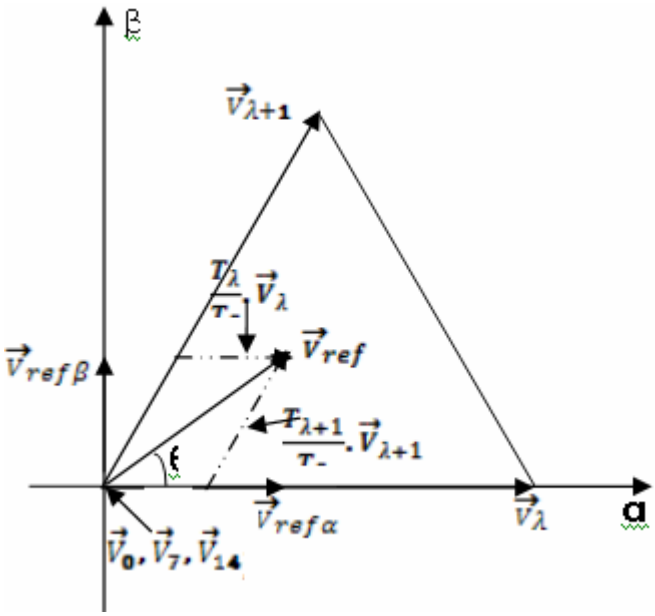

Figure-4. Space vector dwelling time calculation.

The $\vec{V}_{ref}$ is obtained by (7)

$$\vec{V}_{ref} = \frac{T_\lambda}{T_S}\vec{V}_\lambda + \frac{T_{\lambda+1}}{T_S}\vec{V}_{\lambda+1} \quad (7)$$

$$T_S = T_\lambda + T_{\lambda+1} + T_Z \quad (8)$$

T_S is the sampling time, T_λ and $T_{\lambda+1}$ are the dwelling times of $\vec{V}_\lambda$ and $\vec{V}_{\lambda+1}$,respectively. T_Z is the duration of the three zero vectors $\vec{V}_0$, $\vec{V}_7$, and $\vec{V}_{14}$.

$$\vec{V}_{ref} = \vec{V}_{ref\alpha} + \vec{V}_{ref\beta} \quad (9)$$

$$\theta = \tan^{-1}\left(\left[V\right]_{ref\beta} / V_{ref\alpha}\right) \quad (10)$$

Proper distribution of T_λ, $T_{\lambda+1}$ and T_z builds a symmetrical SVPWM pulse, where all switches of the inverter's half-bridge have the same state in the centre and in the two ends.

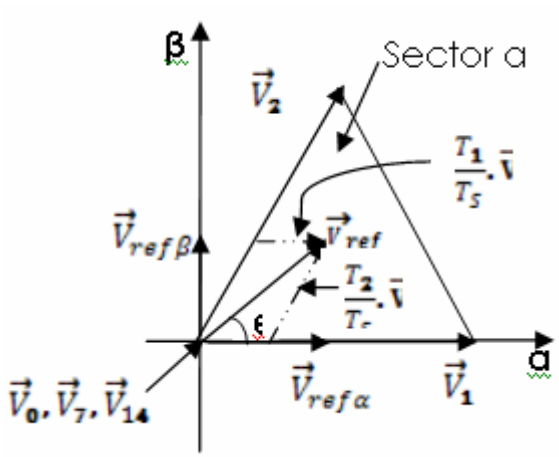

Figure-4(a). Sector a for T1, T2 calculation.

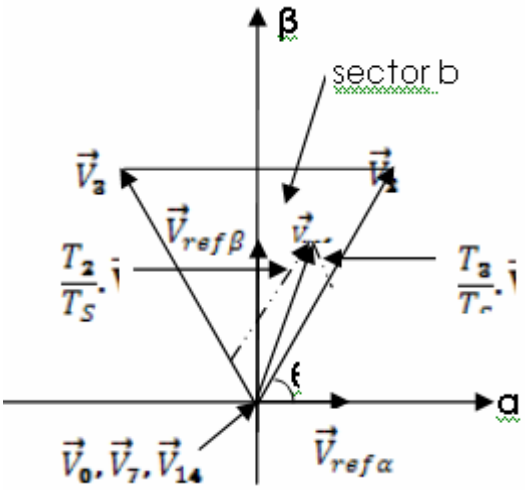

Figure-4(b). Sector b for T2, T3 calculation.

Replacing $\vec{V}_\alpha$ for $\vec{V}_{ref\alpha}$ and $\vec{V}_\beta$ for $\vec{V}_{ref\beta}$ the time calculations for various sectors are:

For sector 'a' of hexagon1 (Figure-4a) the time calculations are:

$$V_\alpha . T_S = V_1 . T_1 + V_2 . T_2 . \cos 60 \quad (11)$$

$$V_\beta . T_S = V_2 . T_2 . \sin 60 \quad (12)$$

$$T_1 = \frac{\left(V_\alpha - V_\beta/\sqrt{3}\right)}{V_1} . T_S \quad (13)$$

$$T_2 = \frac{2}{\sqrt{3}} . \frac{V_\beta}{V_1} . T_S \quad (14)$$

For sector 'b' in hexagon1 (Figure-4b) the time calculations are:

$$V_\alpha . T_S = V_2 . T_2 . \cos 60 - V_3 . T_3 . \cos 60 \quad (15)$$

$$V_\beta . T_S = V_2 . T_2 . \sin 60 + V_3 . T_3 . \sin 60 \quad (16)$$

$$T_3 = \frac{\left(-V_\alpha + V_\beta/\sqrt{3}\right)}{V_3} . T_S \quad (17)$$

$$T_2 = \frac{\left(V_\alpha + V_\beta/\sqrt{3}\right)}{V_2} . T_S \quad (18)$$

For sector g in Hexagon 2 (Figure-4c) the time calculations are:

$$V_\alpha . T_S = V_8 . T_8 . \cos 30 + V_{13} . T_{13} . \cos 30 \quad (19)$$

$$V_\beta . T_S = V_8 . T_8 . \sin 30 - V_{13} . T_{13} . \sin 30 \quad (20)$$

$$T_8 = \frac{\left(V_\alpha/\sqrt{3} + V_\beta\right)}{V_8} . T_S \quad (21)$$

$$T_{13} = \frac{\left(V_\alpha/\sqrt{3} - V_\beta\right)}{V_{13}} . T_S \quad (22)$$

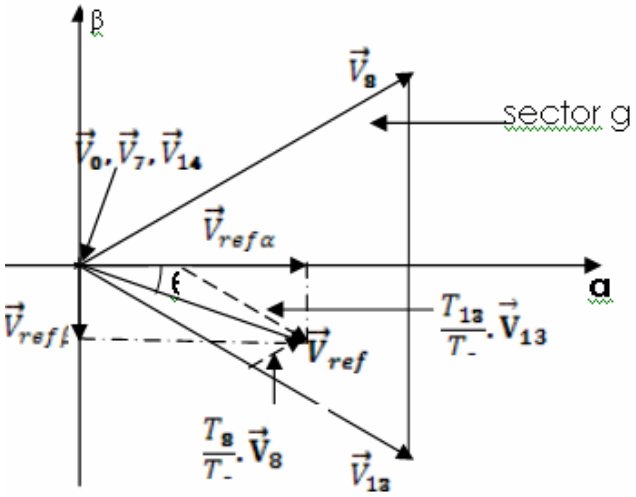

Figure-4(c). Sector g for T8, T13 calculation.

$$V_\alpha . T_S = V_8 . T_8 . \cos 30 \quad (23)$$

$$V_\beta . T_S = V_8 . T_8 . \sin 30 + V_9 . T_9 \quad (44)$$

$$T_8 = \frac{2}{\sqrt{3}} . \frac{V_\alpha}{V_8} . T_S \quad (25)$$

$$T_9 = \frac{\left(-V_\alpha/\sqrt{3} + V_\beta\right)}{V9} . T_S \quad (26)$$

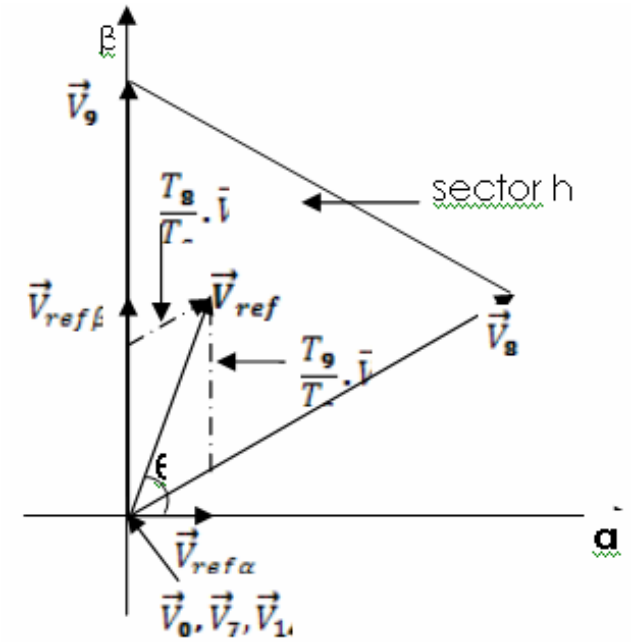

Figure-4(d). Sector h for T8, T9 calculation.

The sector time calculation of Hexagon3 is similar to that of Hexagon 1.

The sequence of space vectors and switch duration for Hexagon 1, 2 and 3 are shown in Figures 5(a), 5(b) and 5(c).

In Hexagon 1,

$T_1 = T_{11} + T_{12}$; $T_2 = T_{21} + T_{22}$; $T_z = T_0 + T_7 + T_{14}$;

$T_s = T_1 + T_2 + T_z$

In Hexagon 2, $T_z = T_0 + T_7 + T_{14}$; $T_s = T_8 + T_9 + T_z$

In Hexagon 3, $T_z = T_0 + T_7 + T_{14}$; $T_z = T_{15} + T_{16} + T_z$

When the reference vector revolves in Hexagon 2, bus clamped technique is used to reduce the THD. In sector 'g' 'a' phase is clamped to positive bus, in sector 'h' phase 'c' is clamped to negative bus, in sector 'i' phase 'b' is clamped to positive bus, in sector 'j' phase 'a' is clamped to negative bus, in sector 'k' phase 'c' is clamped to positive bus and in sector 'l' phase 'b' is clamped to negative bus.

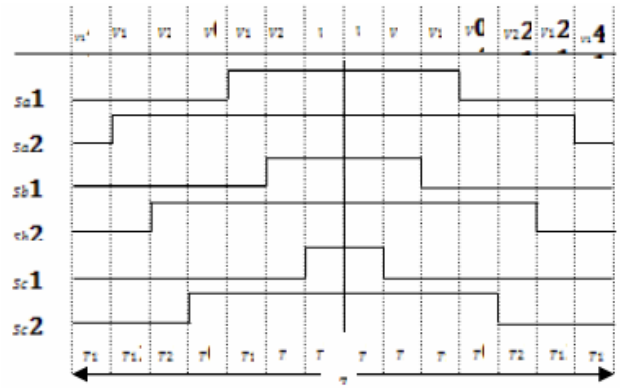

Figure-5(a). Space vector switching sequence of sector a.

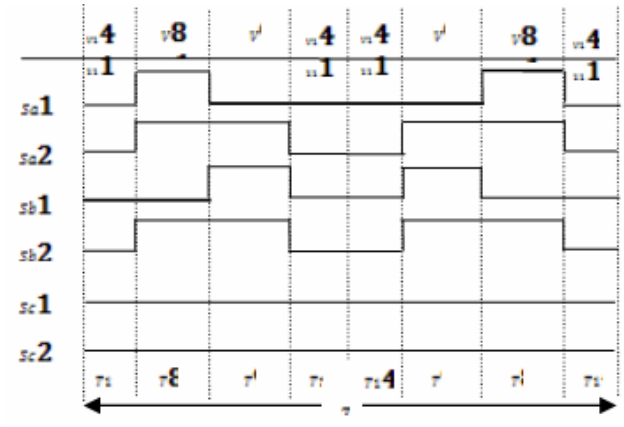

Figure-5(b). Space vector switching sequence of sector h.

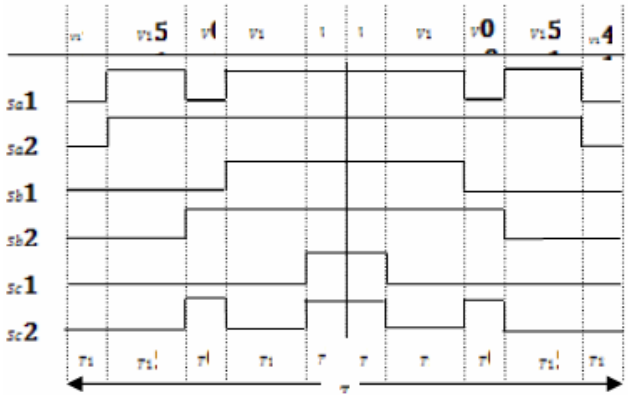

Figure-5(c). Space vector switching sequence of sector m.

SVPWM-4R

In this, the concept of four-region (4R) is utilized in generation of pulses [2-8]. The space vector diagram now is divided into six sectors, each of 60 degrees. Sector1begins at zero degrees and sector6 ends at 360 degrees. The sequence of space vectors for each region is represented in directions in Figure-6.

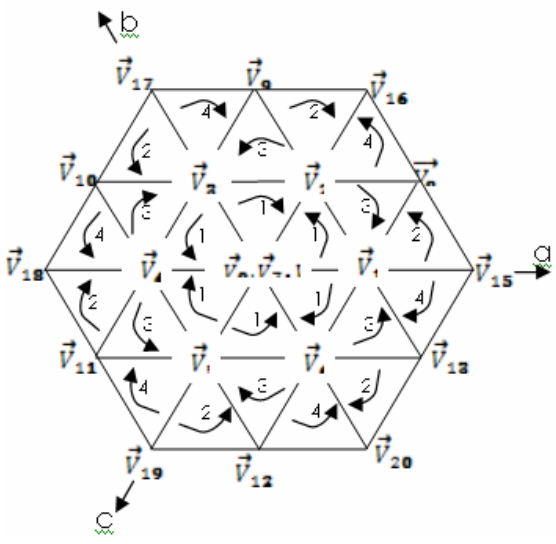

Figure-6. Four region space vector of three-level inverter.

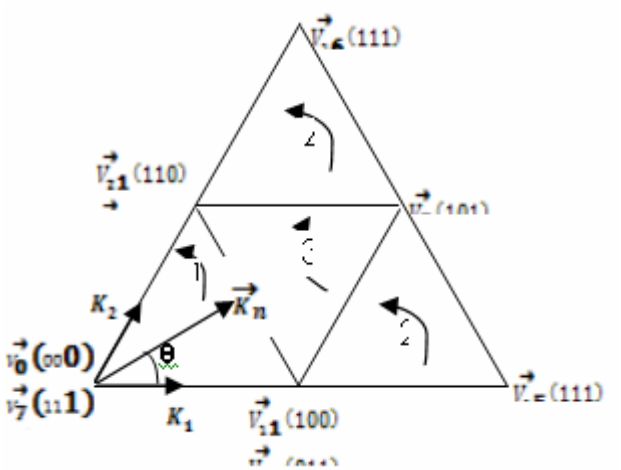

Figure-7. Sector1 and its 4 regions.

From Figure-7 and from Park's transformation the g-h di-phase components are:

$$K_1 = K_n.\left(\cos\theta - \frac{1}{\sqrt{3}}\sin\theta\right) \quad (27)$$

$$K_2 = K_n.\frac{\sin\theta}{\sin\left(\pi/3\right)} \quad (28)$$

Assuming two-unit length for large vector, the division of sector into regions considers the following logic.

If $K_1 < 1$, $K_2 < 1$ and $[(K]_1 + K_2) < 1$ then K_n or reference vector is in region 1.

$K_1 > 1$, reference vector is in region 2.

$K_1 < 1$, $K_2 < 1$ and $[(K]_1 + K_2) > 1$, reference vector is in region 3.

$K_2 > 1$, reference vector is in region 4.

Calculation of vector output intervals

After the determination of switching PWM patterns, the concrete vector output intervals can be calculated as follows. Assuming that the command vector **V** is located in sector S1 shown in Figure-7, the vector output intervals can be calculated according to the following vector equation:

$$T_s\vec{V}_{ref} = T_1\vec{V}_1 + T_2\vec{V}_2 + T_3\vec{V}_3 \quad (29)$$

$$T_s = T_1 + T_2 + T_3 \quad (30)$$

Where $\vec{V}_1, \vec{V}_2, \vec{V}_3$ are the nearest triangle vectors (NTV) [12], [1] and T_1, T_2, T_3 are the corresponding vector output intervals. T_s is the PWM control period. Among the triangles shown in Figure-7, NTV is the triangle where the tip point of the reference vector belongs. Utilizing these three voltage vectors, the reference and output volt-seconds are matched every PWM cycle. The time length of each vector is calculated and summarized in Table-4. In the Table-4, T_s is the PWM period, k_n is the modulation index (magnitude of the reference voltage vector normalized by $E_{dc}/\sqrt{3}$, and θ is the angle from '*a*' phase.

For example, if the command vector $\vec{V}_{ref}$, is located in area 'l', the surrounded three voltage vectors are $\vec{V}_1 = \vec{V}_0$, $\vec{V}_2 = \vec{V}_{s1}$, $\vec{V}_3 = \vec{V}_{s2}$, and the corresponding vector output intervals are $T_1 = T_0$, $T_2 = T_{s1}$, $T_3 = T_{s2}$. Selection of nearest three vectors to generate reference vector minimize the switching frequency of the device and electromagnetic interference and improves the quality of the output voltage spectra.

Table-4. SVPWM-4R space vector duration.

Region 1	Region 3
$T_1s1 = 2.K_1n.T_1s.\sin[(\pi/3 - \theta)]$) $T_{s2} = 2.K_n.T_s.\sin\theta$ $T_z = T_s - T_{s1} - T_{s2}$	$T_{s1} = T_s(1 - 2.K_n.\sin\theta)$ $T_{s2} = T_s\left(1 - 2.K_n.\sin[\left(\frac{\pi}{3} - \theta\right]\right)$ $T_m = T_s\left(2.K_n\sin[\left(\frac{\pi}{3} + \theta\right] - 1\right)$
Region 2	**Region 4**
$T_{s1} = 2T_s\left(1 - K_n\sin[\left(\frac{\pi}{3} + \theta\right]\right)$ $T_{i1} = T_s\left(2.K_n.\sin[\left(\frac{\pi}{3} - \theta\right] - 1\right)$ $T_m = 2.K_n.T_s.\sin\theta$	$T_{s2} = 2.T_s\left(1 - K_n.\sin[\left(\frac{\pi}{3} + \theta\right]\right)$ $T_{i2} = T_s(2.K_n.\sin\theta - 1)$ $T_m = 2.T_s.K_n\sin[\left(\frac{\pi}{3} - \theta\right]\right)$

The sequence of space vectors and switch duration for Region 1, 2, 3 and 4 are shown in Figures 8(a), 8(b), 8(c) and 8(d), respectively.

In Region 1, $T_{s1} = T_{11} + T_{12}$; $T_{s2} = T_{21} + T_{22}$; $T_z = T_0 + T_7 + T_{14}$; $T_s = T_{s1} + T_{s2} + T_z$

In Region 2, $T_{s1} = T_{11} + T_{12}$; $T_{i1} = T_{15}$; $T_m = T_8$; $T_s = T_{s1} + T_{i1} + T_m$

In Region 3, $T_{s1} = T_{11} + T_{12}$; $T_{s2} = T_{21} + T_{22}$; $T_m = T_8$; $T_s = T_{s1} + T_{s1} + T_m$

In Region 4, $T_{s2} = T_{21} + T_{22}$; $T_{i2} = T_{16}$; $T_m = T_8$; $T_s = T_{s2} + T_{i2} + T_m$

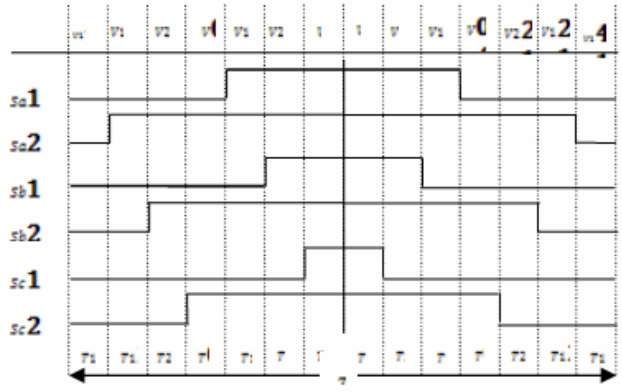

Figure-8(a). Region 1 space vector switching sequence.

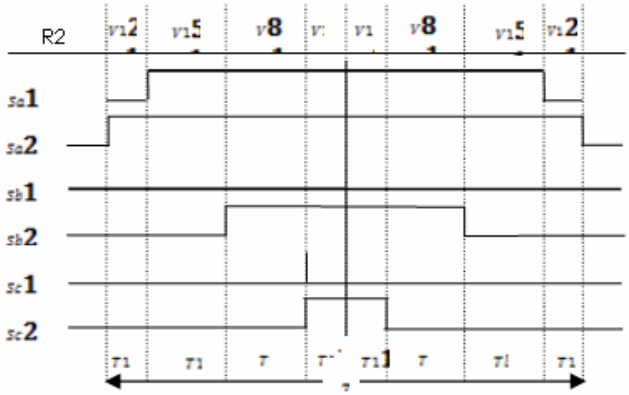

Figure-8(b). Region 1 space vector switching sequence.

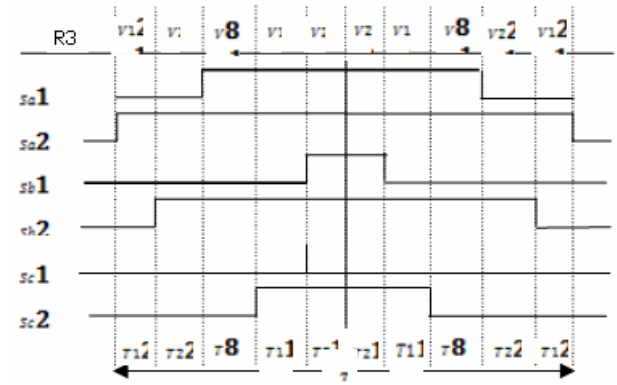

Figure-8(c). Region 3 space vector switching sequence.

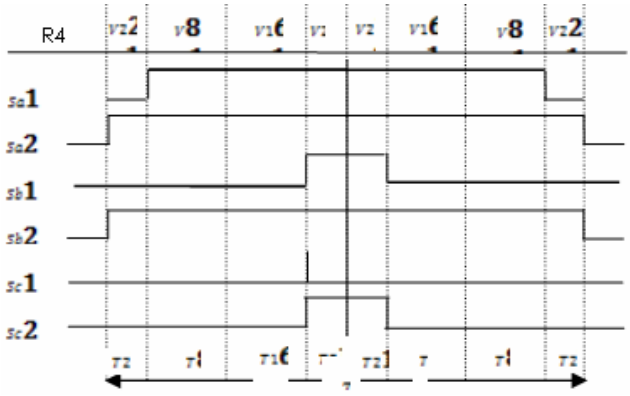

Figure-8(d). Region 4 space vector switching sequence.

BALANCING OF DC-LINK CAPACITOR VOLTAGES

The vector groups defined in section SVPWM ZV, SV, MV, LV affect the balancing of the DC-link capacitor voltages [2, 3, 8]. The ZV and LV do not affect the neutral-point voltage. The MV is somewhat effective on improving voltage unbalance with single switching state and thus the balancing cannot be provided. The SV is the most effective for balancing because USV has charging action, connecting the neutral point to upper capacitor or positive terminal and LSV has discharging action, connecting the neutral point to lower capacitor or negative terminal affecting the neutral point current in opposite ways. Thus special care must be paid in the selection between USV and LSV.

Under unbalanced capacitor charges the equilateral triangles shown in Figure-6 are not possible. We can control the neutral point voltage using SV group either by closed loop or by open loop control.

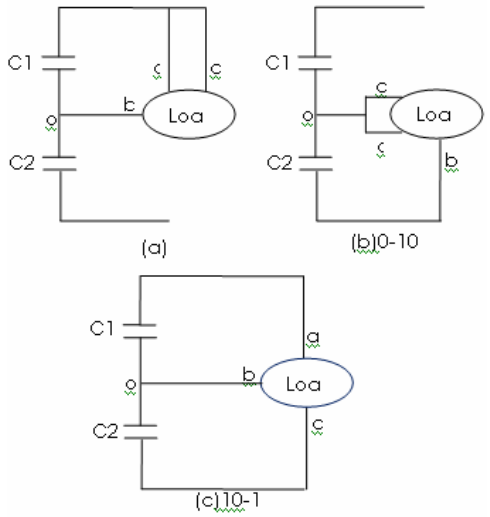

Figure-9. Capacitor charge for space vector V6, V8.

Figures 9(a) and 9(b) shows DC-link capacitor charging and discharging due to vectors Upper state and Lower state of V6. Capacitor C2 charges for the state V61 (101) and discharges during the state V62 (0-10). This states, usage of SV balances the capacitor charge. If the load is inductive these two switching states are almost symmetrical during the switching period and then the DC-link capacitor voltages can be balanced. Figure-9c is for the vector V8.

SIMULATION RESULTS

The four PWM techniques with three-level inverter are modeled and simulated at constant switching frequency of 1500Hz for different modulation indices.

GCMSPWM and MCMSPWM line, phase, pole and dc link capacitor voltages are shown in Figures 10, 11, 12, 13 and Figures 14, 15, 16 and 17, respectively at modulation index of 0.8. GCMSPWM and MCMSPWM technique show similar performance concerned to THD.

SVPWM-3H results at modulation index of 0.9 are shown in Figures 18, 19, 20 and 21.

SVPWM-4R results at modulation index of 0.7 are shown in Figures 22, 23, 24 and 25.

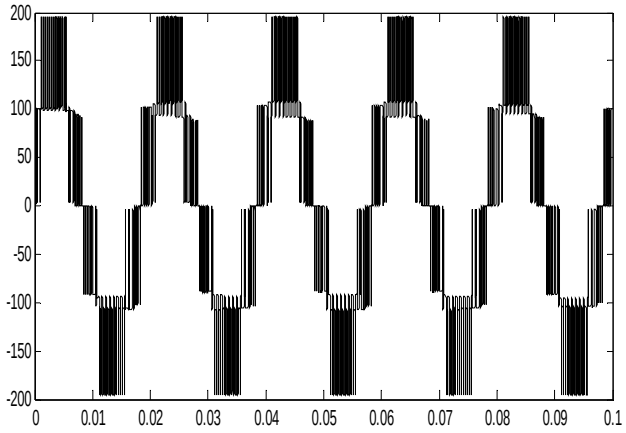

Figure-10. GCMSPWM line voltage.

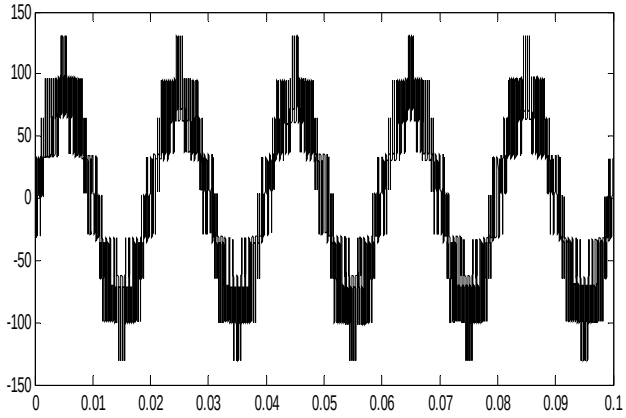

Figure-11. GCMSPWM phase voltage.

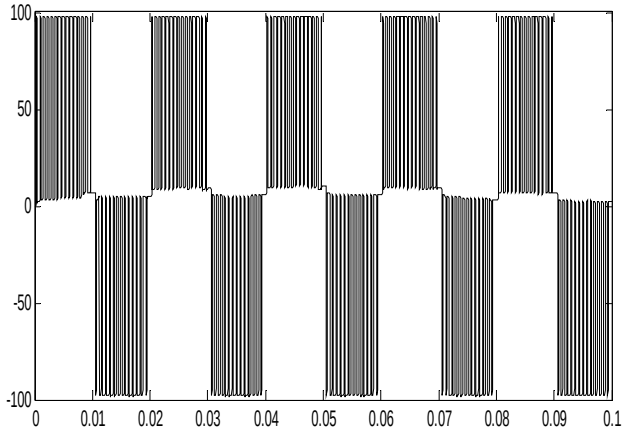

Figure-12. GCMSPWM pole voltage.

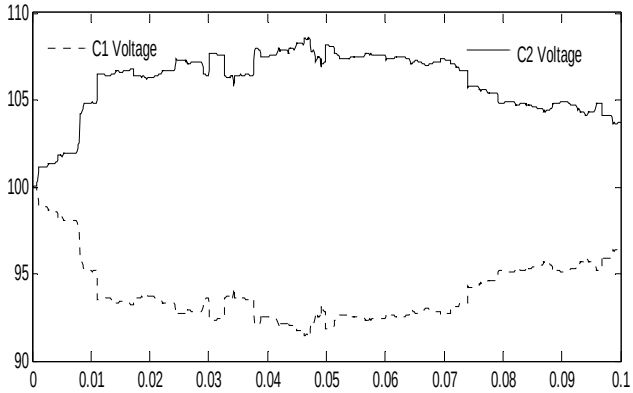

Figure-13. GCMSPWM DC link capacitor voltages.

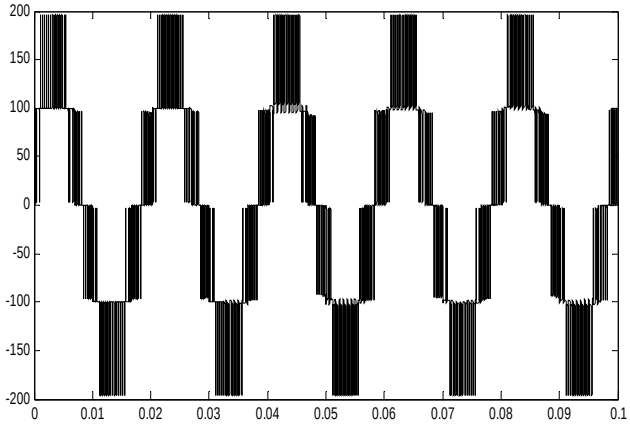

Figure-14. MCMSPWM line voltage.

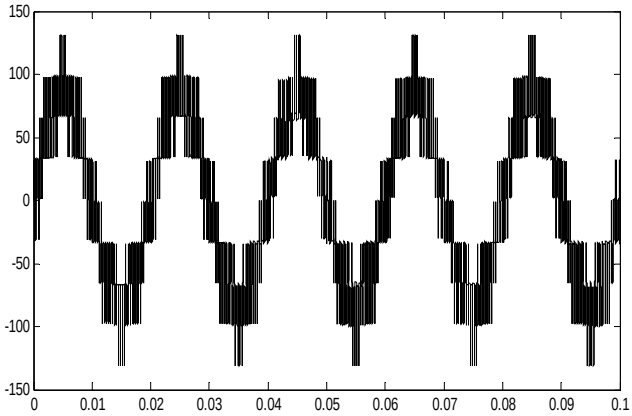

Figure-15. MCMSPWM phase voltage.

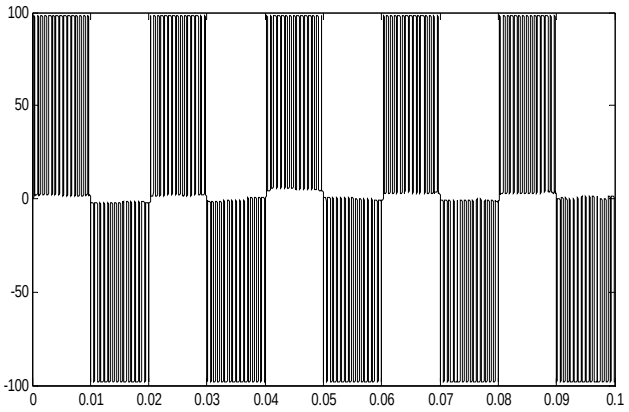

Figure-16. MCMSPWM pole voltage.

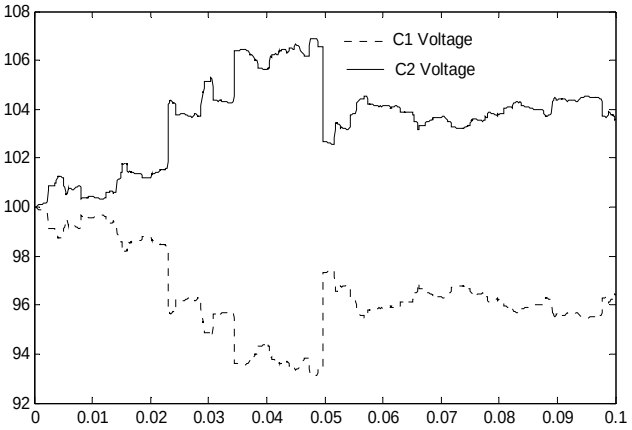

Figure-17. MCMSPWM DC link capacitor voltage.

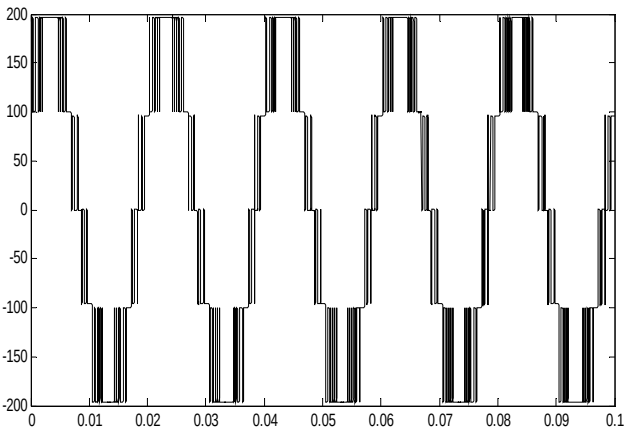

Figure-18. SVPWM-3H line voltage.

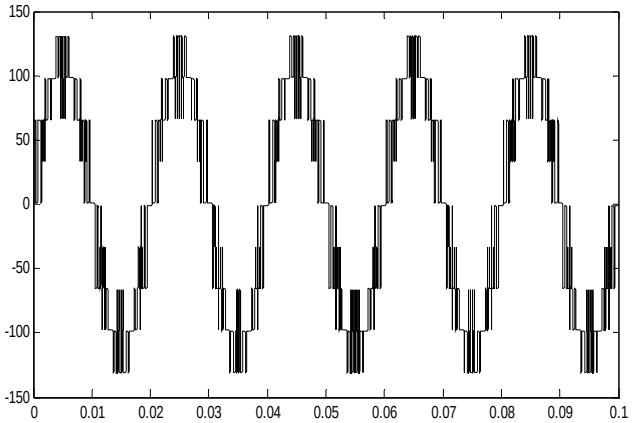

Figure-19. SVPWM-3H phase voltage.

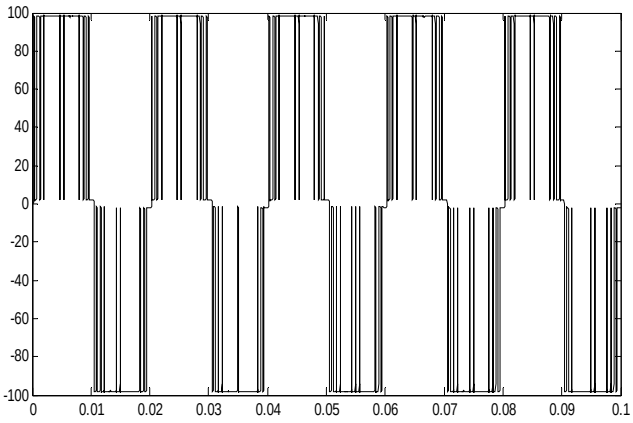

Figure-20. SVPWM-3H pole voltage.

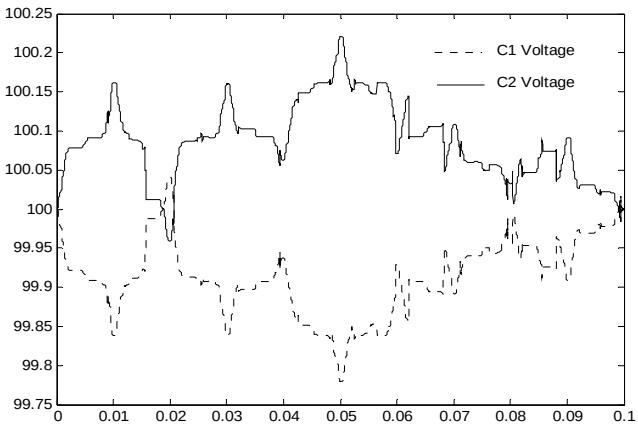

Figure-21. SVPWM-3H DC link capacitor voltages.

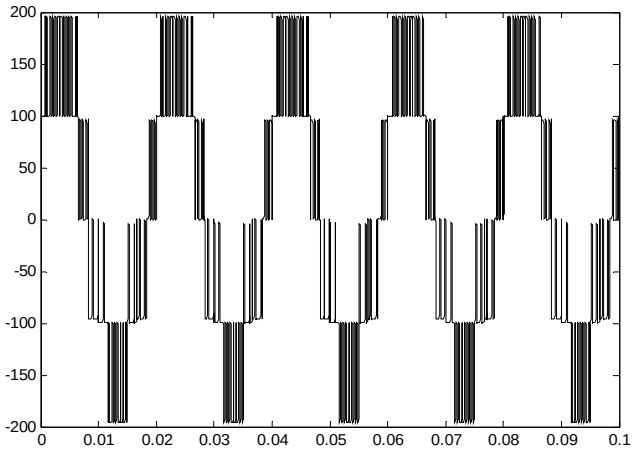

Figure-22. SVPWM-4R line voltage.

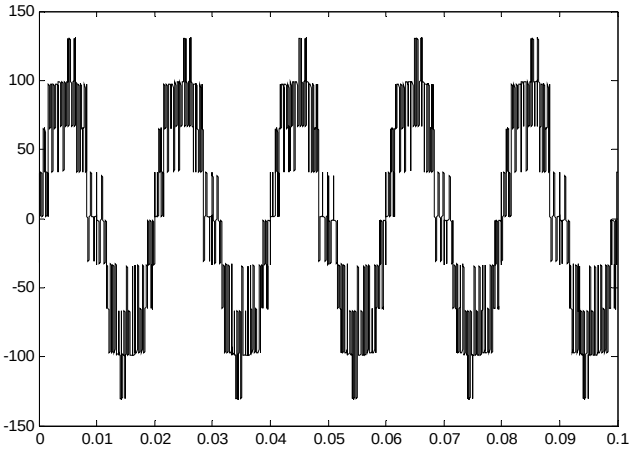

Figure-23. SVPWM-4R phase voltage.

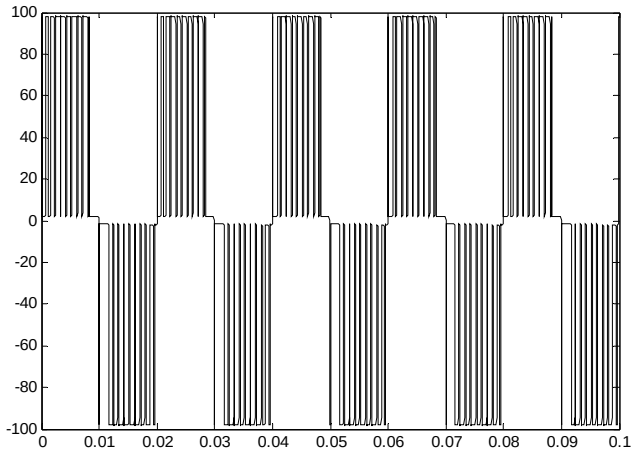

Figure-24. SVPWM-4R pole voltage.

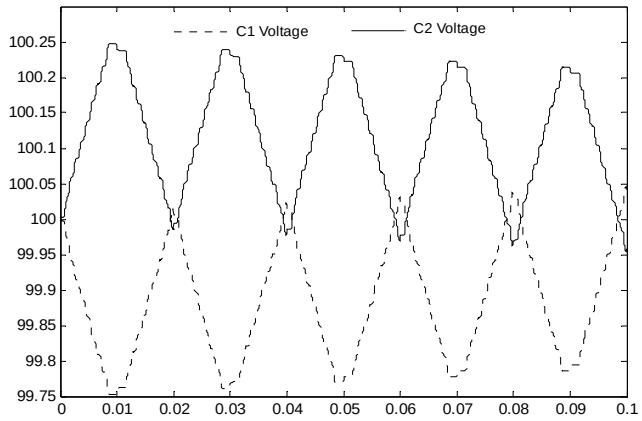

Figure-25. SVPWM-4R DC link capacitor voltages.

Figure-26 shows the performance curve, modulation index Vs Total Harmonic Distortion of a three-level inverter run on four PWM techniques.

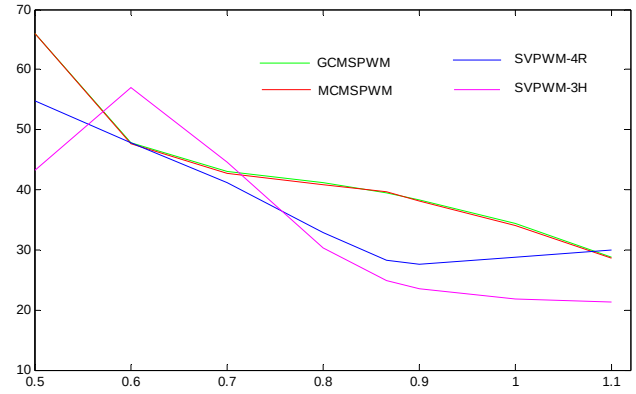

Figure-26. THD Vs modulation index.

CONCLUSIONS

The capacitor voltage unbalance is high in GCMSPWM and MCMSPWM compared to SVPWM-3H and SVPWM-4R.

SVPWM-3H technique show better performance with reduced total harmonic distortion during under modulation region and increased modulation index beyond 0.75 and is obtained by using bus-clamped technique.

Between 0.55 and 0.75 of modulation index, SVPWM-4R technique has shown better performance with reduced THD.

REFERENCES

[1] Hind Djeghloud, Hocine Benalla. Space Vector Pulse Width Modulation Applied to the Three-Level Voltage Inverter.

[2] Nikola Celanovic, Dushan Boroyevich. 2000. A Comprehensive Study of Neutral-Point Voltage Balancing Problem in Three-Level Neutral-Point-Clamped Voltage Source PWM Inverters. IEEE Transactions on Power Electronics. 15(2): 242-249.

[3] P.F. Seixas, M.A. Severo Mendes, P. Donoso-Garcia and A.M.N. Lima. 2000. A Space Vector PWM Method for Three-Level Voltage Source Inverters. pp. 549-555.

[4] Fei Wang. 2002. Sine-Triangle versus Space-Vector Modulation for Three-Level PWM Voltage-Source Inverters. IEEE Transactions on Industry Applications. 38(2): 500-506.

[5] B. Kaku, I. Miyashita and S. Sone. 1997. Switching Loss minimized Space Vector PWM for IGBT three-level inverter. IEE Proc.-Electrical Power Appl. 144(3): 182-190.

[6] Ayse Kocalmis and Sedat Sünter. Modelling and simulation of a multilevel inverter using Space vector modulation technique.

[7] Ayse Kocalmis and Sedat Sünter. Simulation of a Space Vector PWM Controller for a Three-Level Voltage-Fed Inverter Motor Drive. pp. 1915-1920.

[8] Hyo L. Liu, Nam S. Choi and Gyu H. Cho. DSP based space vector PWM for three-level Inverter with dc-link voltage balancing IECON'91.

[9] José Rodríguez, Jih-Sheng Lai and Fang Zheng Peng. 2002. Multilevel Inverters: A Survey of Topologies, Controls, and Applications. IEEE Transactions on Industrial Electronics. 49(4): 724-738.

[10] Leon M. Tolbert and Thomas G. Habetler. 1998. Novel Multilevel Inverter Carrier-Based PWM Methods. IEEE IAS Annual Meeting, St. Louis, Missouri. October 10-15. pp. 1424-1431.

[11] P. Palanivel and Subhransu Sekhar Dash. 2009. Multicarrier Pulse Width Modulation Based Three Phase Cascaded Multilevel Inverter Including over Modulation and Low Modulation Indices. International Journal of Engineering Studies, ISSN 0975-6469. Research India Publications. pp. 71-82.

[12] P. Palanivel and Subhransu Sekhar Dash. 2009. Comparative Study of Constant Switching Frequency and Variable Switching Frequency Multicarrier Pulse width Modulation for Three Phase Cascaded Multilevel Inverter. International Journal of Recent Trends in Engineering. 2(2): 49-52.