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TWO HARMONIC ELIMINATION IN CURRENT SOURCE INVERTER FED DRIVES - A UNIFIED APPROACH

V. Rajini[1] and P. Saranya[2]
SSN College of Engineering, Anna University, Chennai, Tamil Nadu, India
E-Mail: rajiniv@ssn.edu.in

ABSTRACT

The Selective Harmonic Elimination (SHE) for Current Source Inverter (CSI) fed drives is presented in this paper. The PWM patterns for selective harmonic elimination are generated using a unified approach. The conventional methods cannot handle more than a few harmonics as the independent chop angles are restricted to 30^o. In this work, a combination of chops as well as short circuit pulses are utilized to selectively eliminate lower order harmonics with minimum switching frequency.

Keywords: selective harmonic elimination, current source inverter, shorting pulses.

1. INTRODUCTION

One of the most suitable drive packages for high power adjustable speed application where regeneration is required is current source inverter feeding an induction motor. The CSI can generally be divided into pulse width-modulation (PWM) CSI and load-commutated inverters (LCIs). The former uses symmetrical gate turn-off (GTO) or integrated gate-commutated thyristor (IGCT) as a switching device, whereas the latter employs silicon-controlled rectifier (SCR) devices. Generally speaking, the current-source converters feature a simple converter structure, low switch count, low switching dv/dt, and reliable over current/short-circuit protection. The main drawback lies in its limited dynamic performance due to the use of large dc choke. High-power CSI drives in the megawatt range are widely used in the industry [2, 3]. The conventional three-phase current source inverter has the shortcoming of introducing increased lower order harmonics in the output currents which give rise to losses, noise and torque pulsation in the machine, specially at lower frequency of operation. To overcome these drawbacks, the selective harmonic elimination technique is proposed along with evenly distributed short circuit pulses. Elimination of several low order harmonics is usually very important in CSI's to avoid possible resonance between the input/output filter capacitance and an input/output circuit inductance. To eliminate a number of harmonics selectively, an approach similar to VSI [6] can be applied to CSI, keeping in mind that in addition to usual half wave and quarter wave symmetry to avoid even harmonics, the waveform before and after $\pi/6$ in a PWM-SHE should be an inverse mirror image to always ensure continuity of the current for CSI. Thus, the conventional techniques cannot be directly applied to CSI. On the other hand, three phase CSI's are not dual systems for three phase VSI's. For the VSI, independent angles are specified between 0 and $\pi/2$. However, selective harmonic elimination (SHE) methods available in the literature for CSI are simply based on independent chop angles between 0 and $\pi/6$. These conventional SHE methods cannot handle more than a few harmonics [10, 13] because of the imitation in the chop angles

2. SHE IN CURRENT SOURCE INVERTERS

A three-phase output can be obtained from the configuration of six switches as shown in Figure-1. Each switch conducts for 180'. Two switches remain ON at any instant of time. When S1 is ON, terminal A is connected to the positive terminal of the DC current source. When transistor S4 is switched ON, terminal A is brought to the negative terminal of the DC current source.

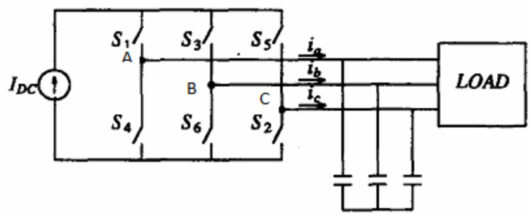


Figure-1. A current source inverter.

There are six modes of operation in a cycle and the duration of each mode is 60'. The switches are numbered in the sequence of their gating (12, 23, 34, 45, 56, 61) and are shifted from each other by 60° to obtain three-phase balanced currents. This conventional unmodulated CSI provides 120^o square output line current as shown in Figure-2 that contains harmonic components having magnitude of 1/ h of the fundamental where h is the order of the harmonic. The harmonic spectrum of Figure-2 is given in Figure-3 where the lower order harmonics are dominant.

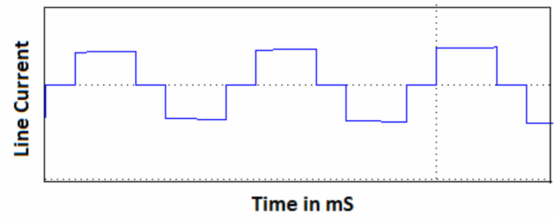


Figure-2. Line current in CSI.

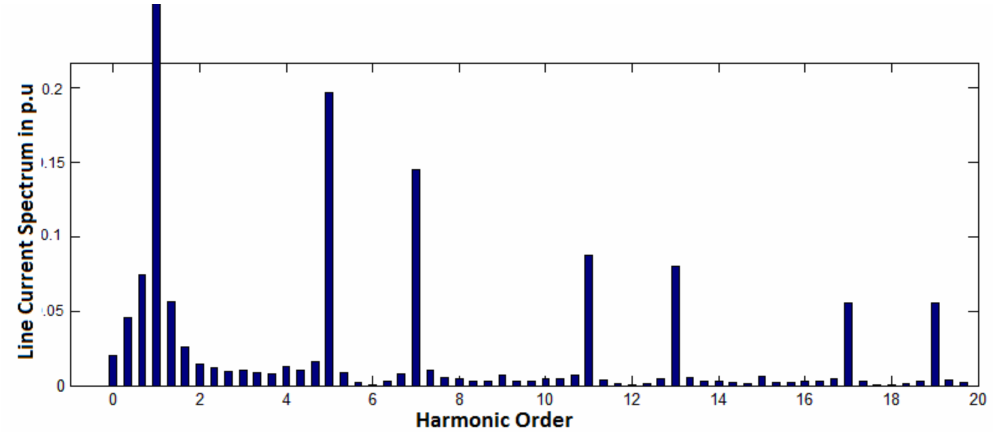


Figure-3. Harmonic spectrum of line current in CSI.

A number of pulse-width modulated (PWM) current source inverters (CSI) are generally employed with high switching frequency to obtain a near-sinusoidal output voltage and current. The proposed CSI with selective harmonic elimination (SHE) operates with low switching frequency, which minimizes the switching losses. This requirement becomes increasingly important as the rated voltage of the motor is increased. In this work, a generalized PWM- SHE method is taken to eliminate lower order harmonics. The undesirable lower order harmonics of a square wave can be eliminated by creating notches on the square wave at predetermined angles as shown in Figure-4.

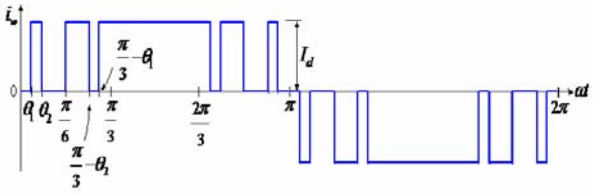


Figure-4. Output with notches required to eliminate two harmonics.

In Figure-4, one cycle of output is shown with half-wave symmetry and quarter-wave symmetry. It can be shown that the two notch angles θ_1 and θ_2 can be found to eliminate two significant harmonic components and control the fundamental current. A large number of harmonic components can be eliminated if the waveform can accommodate additional notch angles.

$$iw(wt)=\frac{ao}{2}+\sum_{n=1}^{\infty} an\sin(nwt)+bn\cos(nwt) \tag{1}$$

∞

Due to half wave symmetry, a0 and bn are equal to zero and an is given by equation

$$a_n=\frac{4}{\pi}\int_0^{\frac{\pi}{2}} i_w(\omega t)\sin(n\omega t)d(\omega t) \tag{2}$$

Therefore,

$$i_w(\omega t)=\sum_{n=1}^{\infty} a_n\sin(n\omega t) \tag{3}$$

$$a_n=\frac{4I_{dc}}{\pi}\times\begin{cases}\int_{\theta_1}^{\theta_2}\sin(n\omega t)d(\omega t)+\ldots+\int_{\theta_k}^{\frac{\pi}{6}}\sin(n\omega t)d(\omega t)+ & \\ \int_{\frac{\pi}{3}-\theta_k}^{\frac{\pi}{3}-\theta_{k-1}}\sin(n\omega t)d(\omega t)+\ldots+\int_{\frac{\pi}{3}-\theta_1}^{\frac{\pi}{2}}\sin(n\omega t)d(\omega t) & \text{k = odd;}\\ \int_{\theta_1}^{\theta_2}\sin(n\omega t)d(\omega t)+\ldots+\int_{\theta_{k-1}}^{\theta_k}\sin(n\omega t)d(\omega t)+ & \\ \int_{\frac{\pi}{6}}^{\frac{\pi}{3}-\theta_k}\sin(n\omega t)d(\omega t)+\ldots+\int_{\frac{\pi}{3}-\theta_1}^{\frac{\pi}{2}}\sin(n\omega t)d(\omega t) & \text{k = even.}\end{cases} \tag{4}$$

To eliminate *nth* harmonic, set *an* = 0. So,

$$F_i(\theta_1,\theta_2,\theta_3,\ldots,\theta_k)=0 \qquad i=1,2,\ldots,k \tag{5}$$

For 5th and 11th harmonic elimination, the notch angles can be determined by solving the two non-linear transcendental equations 6 and 7.

$$F_1 = \cos(5\theta_1) + \cos(5(\Pi / 3 - \theta_1)) - \cos(5\theta_2) - \cos[5(\Pi / 3-\theta_2)) - \cos(5\Pi / 6) = 0 \quad (6)$$

$$F_2 = \cos(11\theta_1) + \cos(11(\Pi / 3 - \theta_1)) - \cos(11\theta_2) - \cos(11(\Pi / 3-\theta_2)) - \cos(11\Pi / 6) = 0 \quad (7)$$

The equations (6) and (7) are solved by Resultant Theory [9] using Wolfram Mathematica, wherein the nonlinear transcendental equations are first converted in to linear polynomial equations and solved. The chopping angles for 5th and 11th harmonic elimination are computed as $\theta_1 = 12.96'$ and $\theta_2 = 19.14'$. Table-1 shows the switching angles determined using the resultant theory for single and two harmonics elimination.

Table-1. Switching angles for SHE.

Harmonics to be eliminated	**Switching Angles**	
	Θ1	**Θ2**
5	18	-
7	21.43	-
11	24.55	-
13	25.38	-
5,7	7.93	13.75
5,11	12.96	19.14
5,13	14.48	21.12
7,11	15.23	19.37
7,13	16.58	20.79

With these switching angles, the line current for 5th and 11th harmonic elimination are obtained as shown in Figure-5. The harmonic spectrum of the line current shown in Figure-5 is given in Figure-6 from which it is clear that the 5th and 11th harmonics are not totally eliminated.

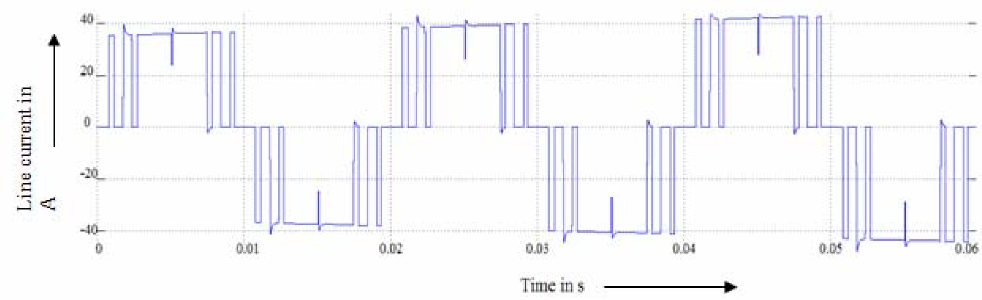


Figure-5. Line current for 5th and 11th harmonics elimination with switching angles given in Table-1.

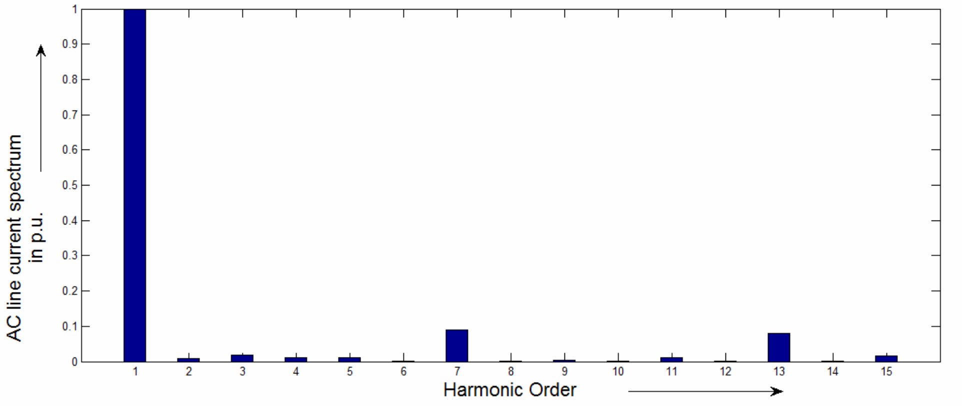


Figure-6. Harmonic spectrum of line current shown in Figure-5.

The similar results were observed for the other cases also. The line current waveform obtained for 7th and 11th harmonic elimination and the corresponding harmonic spectrum are shown in Figures 7 and 8, respectively. Hence, it could be understood that the switching angles given in Table-1 can only mitigate and not completely eliminate harmonics as expected.

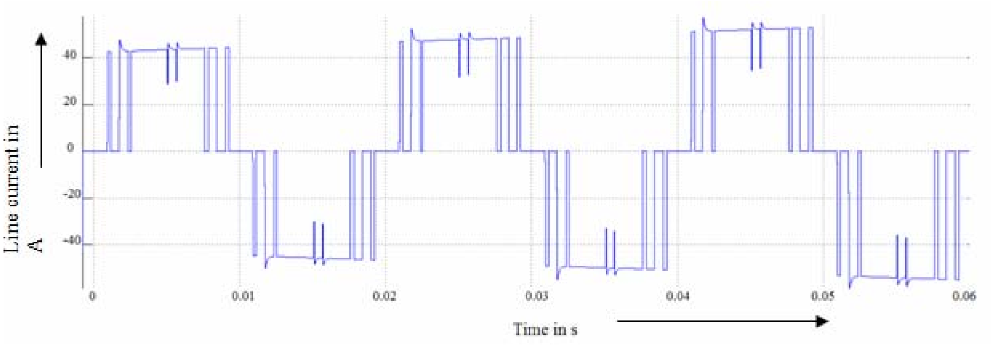


Figure-7. Line current for 7th and 11th harmonics elimination.

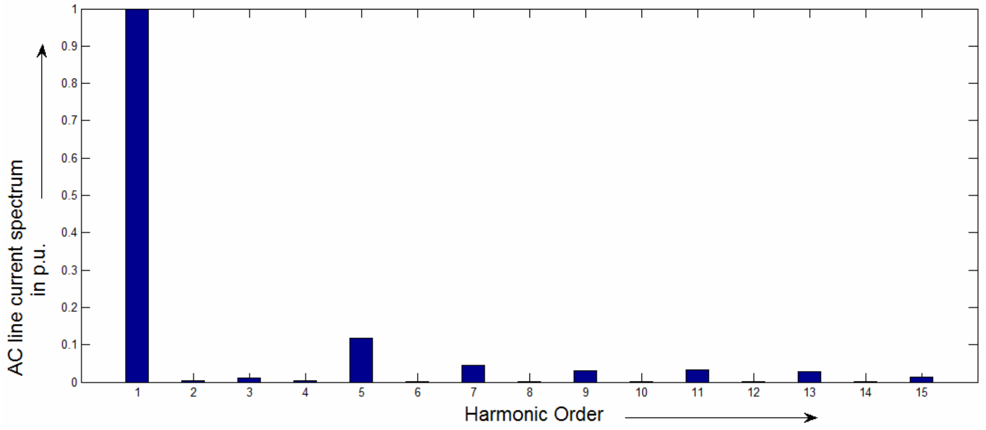


Figure-8. Harmonic spectrum of line current shown in Figure-7.

3. GENERALIZED PWM SHE

Many different PWM patterns and strategies have been reported in the literature for harmonic elimination in CSI. These include many different on-line methods like, sinusoidal pulse width modulation, SPWM or off-line methods like, selective harmonic elimination and magnitude modulation and PWM-SHEM patterns for fundamental magnitude control and harmonic reduction [6]. There is a restriction for the CSI PWM patterns as in addition to usual half wave and quarter wave symmetry to avoid even harmonics, the waveform before and after π/6 in a PWM-SHEM should be an inverse mirror image to always ensure continuity of the current. Also, Unlike VSI, the DC bus in a CSI can be shorted momentarily because of the DC link inductor. This property can be utilized to create more flexible PWM patterns for CSIs. The required ac line currents can become zero simultaneously for a given PWM pattern. This is the case when null line waveforms are required. Under this condition, the dc-link current in CSIs must circulate through either the switches 1 and 4, 3 and 6, or 5 and 2 to avoid interrupting the dc-link current. To provide the shorting paths, additional gating pulses are required. However, because the number of possible configurations for positioning these short circuit pulses increases as the number of eliminated harmonics increases, a generalized method is quite essential for constructing suitable PWM patterns in reasonable time. Recently, several researchers have tried to minimize the harmonic content of the output current in CSI by using short circuit pulses. [6]. these shorting pulses should be symmetrically distributed other wise they will result in unbalanced operation.

Hence, in this work, a generalized PWM-SHE strategy based on short circuit pulse positioning has been reported for two harmonic elimination though it can be extended for any number of harmonic elimination. The combination of chops and shorting pulses are used to selectively eliminate any two of the lower order harmonics with minimum switching frequency.

The number of independent angles ‘E’ required for a SHE pattern can be obtained using a general equation given below.

$$E = 2N+1,\ N = 1, 2, 3\ldots. \tag{8}$$

For elimination of two lower order harmonics, the values of N are 2 and hence, the numbers of independent angles to be determined are 5 which include the short circuit pulses also. Now, with the known chop angles given by Table-1, the number of shorting pulses ‘S’ required can be calculated using equation 9.

$$\begin{aligned} S &= (N+2)/2 \quad \text{if N is even} \\ &= (N+1)/2 \quad \text{if N is odd} \end{aligned} \tag{9}$$

Hence, for N = 2, the number of shorting pulses are 2 and the number of transitions 'T' is given by equation 10.

$$T = 3N/2 \quad \text{if } N = \text{even}$$
$$= (3N + 1) \quad \text{if } N = \text{odd} \qquad (10)$$

It could be noted that the relation between E, T and S can be given by equation 11.

$$E = T+S \qquad (11)$$

The number of chops per cycle per switch 'C' and the corresponding switching frequency 'f_s' are also given by equations 12 and 13, respectively.

$$C = 4N + 2 \quad \text{if } N = \text{even,}$$
$$= 4N + 3 \quad \text{if } N = \text{odd} \qquad (12)$$

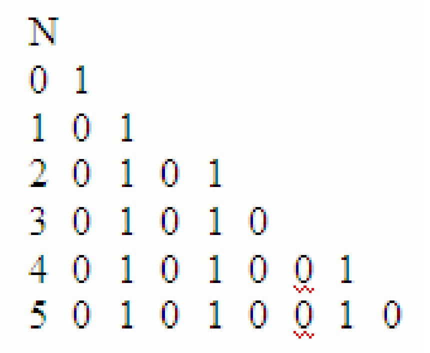
$$fs = f_b C \qquad (13)$$

Where f_b is the fundamental frequency. The Table-2 shows the values of E, T, S for various values of N. The allocation of shorting pulses in the region 0 to π/6 is given in Table-3. It may be noted that in Table-3, 0 represents transition without shorting pulse and 1 represents transition with shorting pulse.

Table-2. Relation between E, T and S with N.

N	0	1	2	3	4	5
E	1	3	5	7	9	11
T	0	2	3	5	6	8
S	1	1	2	2	3	3
C	2	7	10	15	18	23

Table-3. Allocation of shorting pulses.



N
0 1
1 0 1
2 0 1 0 1
3 0 1 0 1 0
4 0 1 0 1 0 0 1
5 0 1 0 1 0 0 1 0

The scope of the present work is limited to two harmonic elimination and hence, the generalized PWM pattern is presented only for it. However, it may be noted that this method may be extended to any number of harmonic elimination. For n^{th} harmonic elimination in Ia, the current can be given by equation.

$$Ia = 4Idc/n\pi\,(\cos n\theta_1 - \cos n\theta_2 + \cos n\pi/6 - \cos n(\pi/3 - \theta 3) + \cos n(\pi/3 - \theta 1) - \cos n(\pi/3 + \theta 2) + \cos n(\pi/3 + \theta 3) - \cos n\pi/2 \qquad (14)$$

The system of non linear transcendental equations are solved to find the chop angles. Figure-9 gives the generalized PWM pattern for two harmonic elimination.

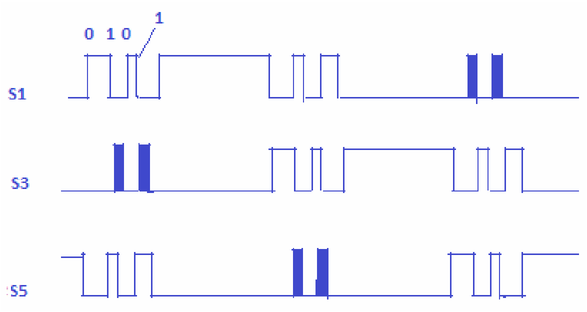


Figure-9. Generalized PWM pattern for two harmonic elimination.

The chop angles are independent only in region π/6, the pattern given in Figure-9 is redrawn between 0 and π/2 in Figure-10. With the SHE pattern obtained for different two harmonic elimination, the line currents are obtained. The line current for 5th and 7th harmonic elimination with shorting pulses is shown in Figure-11 and the corresponding harmonic spectrum is shown in Figure-12.

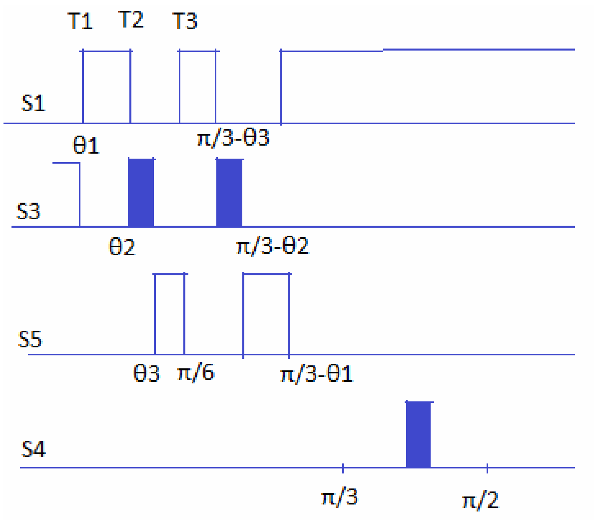


Figure-10. PWM pattern in the region 0-π/2.

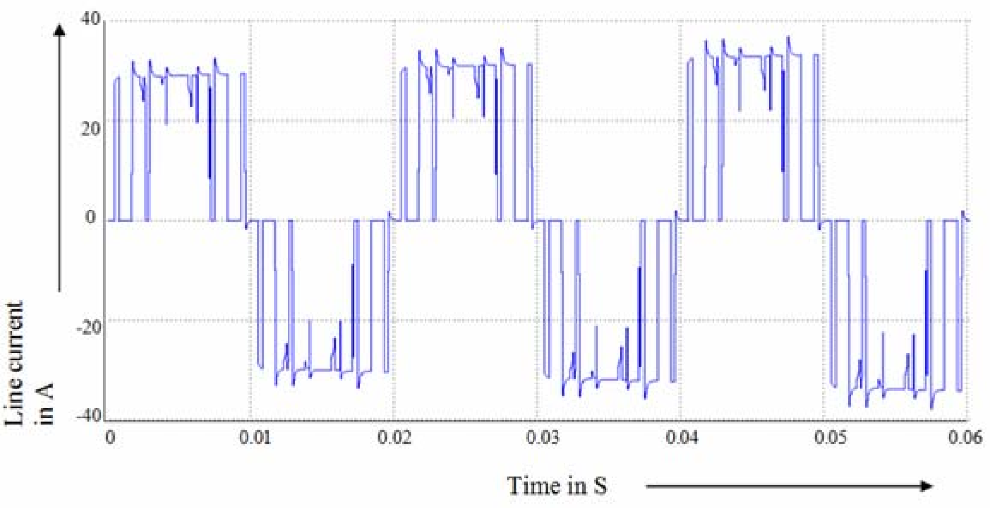


Figure-11. Line current for 5th and 7th harmonic elimination with shorting pulses.

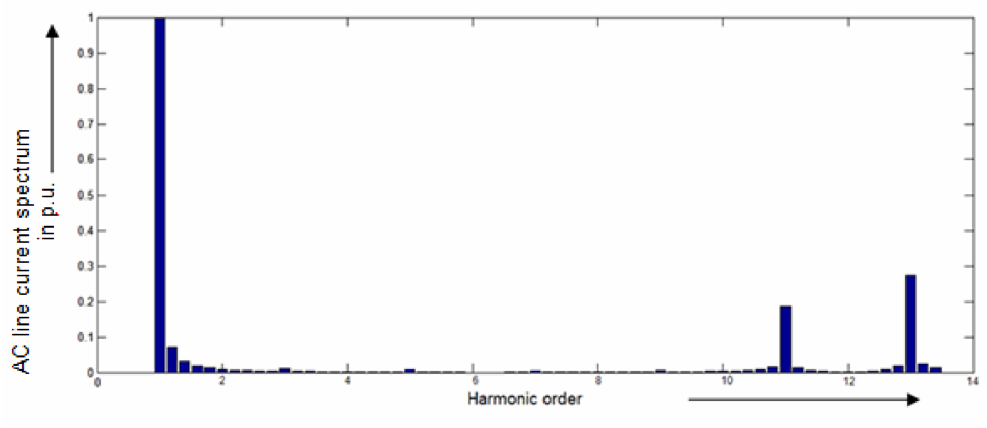


Figure-12. Harmonic Spectrum for 5,7th harmonic elimination for line current in Figure-11.

In the same way, the line currents and their spectrums for 5, 11 and 5, 13 are shown in Figure-13. Figure-14 gives similar results for 7, 11 and 7, 13th elimination.

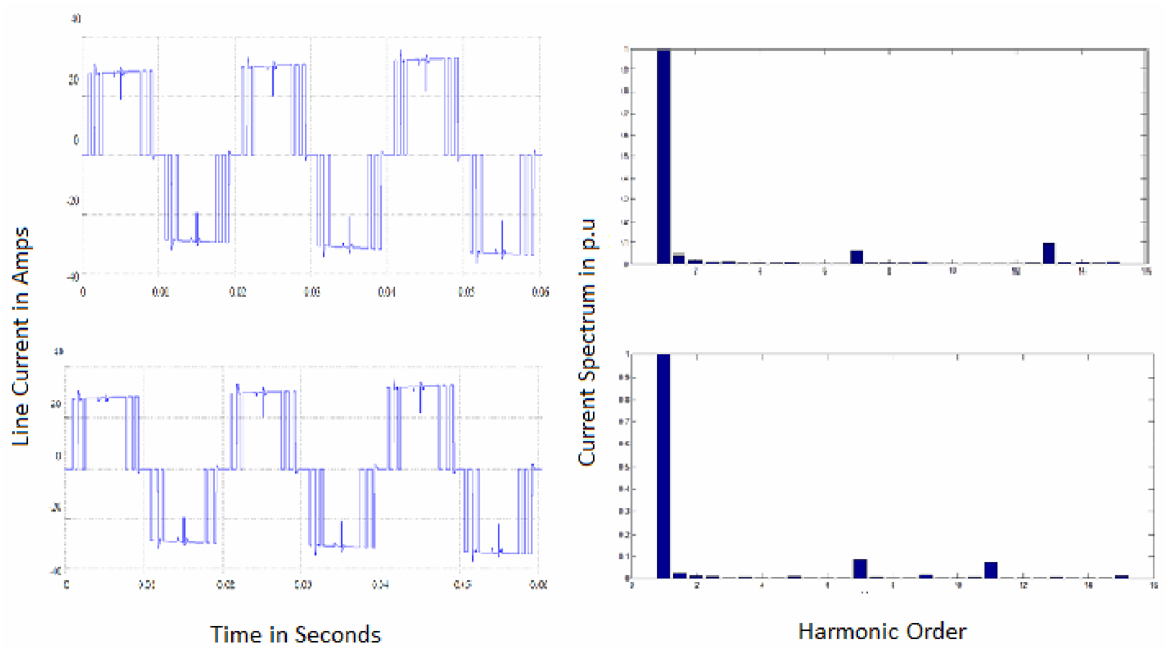


Figure-13. Line current and its harmonics for; a) 5, 11 and b) 5,13th harmonic elimination using Generalized PWM.

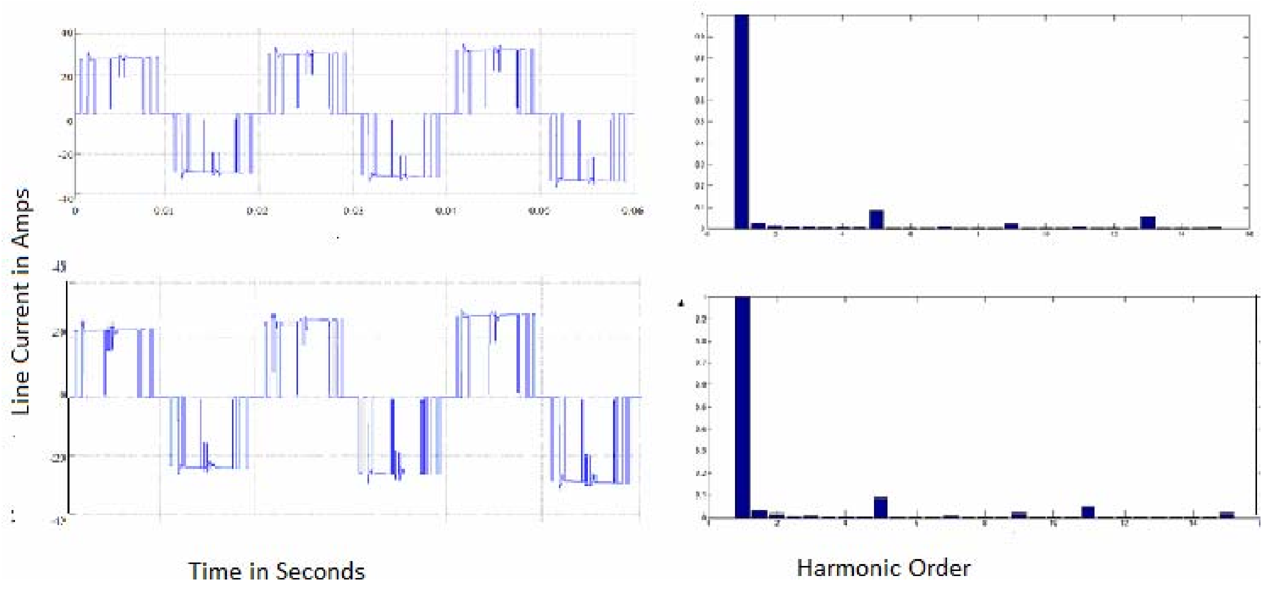


Figure-14. Line current and its harmonics for; a) 7, 11 and b) 7,13th harmonic elimination using generalized PWM.

4. HARDWARE IMPLEMENTATION OF SHE

The Hardware setup of a Three-phase current source inverter feeding a resistive load is as shown in Figure-15.

Figure-15. Hardware setup of three-phase CSI.

The power circuit comprises of a three-phase current source inverter feeding a resistive load. Since the harmonic analysis is made only for inverter output line current, the load is taken as resistive. The input DC side of the current source inverter is fed by stiff current source which is developed by connecting a DC voltage source in series with reactor/inductor. Generally GTO devices are used for current source inverter in case of high power applications. Also, since selective harmonic elimination scheme operates at low switching frequency, GTO devices are efficient to operate. For the proposed prototype model of current source inverter, the IGBTs are suitable but since they are more expensive, the cost effective MOSFETs (7N60) are chosen. The forward blocking devices used in series with the switching devices are the power diodes (1N5408). The value of the DC link reactor/inductor is calculated as follows.

$$L_{min} = V/\left(\omega s^{*}\left[Imax - i(0^{+})\right]\right) \quad (12)$$

$V = 1.414 * 30 = 42.42$ V

$\omega_s = (2 * 3.1415 * 500)/60$ [since $f_s = 500$Hz]

$= 52.35$ rads/second

$I_{max} - i(0^{+}) = 24$ A

Where

$i(0^{+}) = 8$A

Therefore, $L_{min =}$ 33.76 mH ~ 34 mH.

The control circuit is shown in Figure-16. The Control circuit is developed with PIC microcontroller, optocoupler unit and their supply units i.e., 5V regulated power supply for PIC microcontroller and 12V regulated power supply for optocoupler unit. The PIC 18F4550 microcontroller is programmed to produce the gating pattern as desired, by incorporating the selective harmonic elimination method. PORTB is used as a I/O port, with only 6 pins for output. The 20MHz external crystal oscillator is used. The optocoupler circuit provides the necessary isolation between the controller and the power circuit. It also provides the gating pulse with voltage (V_{GS}) required to trigger on the MOSFET switch. The Hardware setup of the control circuit with PIC 18f4550 microcontroller is as shown in Figure-16.

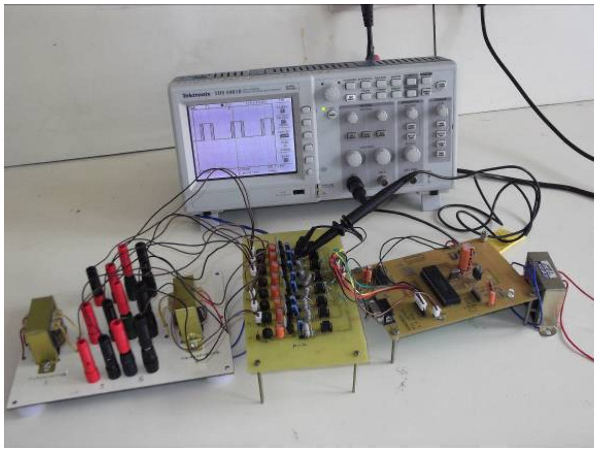


Figure-16. Hardware setup of control circuit with PIC 18f4550 microcontroller.

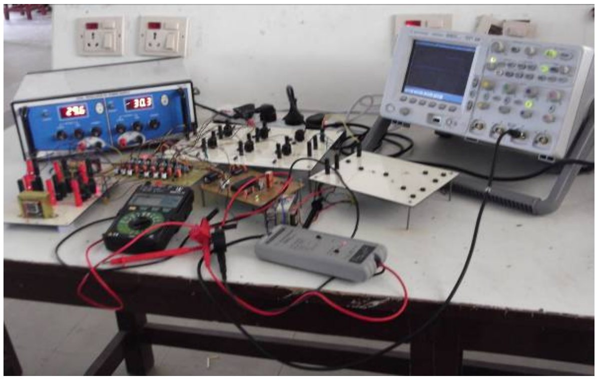


Figure-17. Hardware setup including both power circuit and control circuit.

5. EXPERIMENTAL RESULTS

The waveforms are recorded using Agilent Technologies Mixed signal Oscilloscope (MSO6014A). The gating pulse pattern for the elimination of two harmonics i.e., 5th and 11th harmonics is recorded as shown in Figure-18. For 5th and 11th harmonic elimination the output line voltage waveform and output line current waveform is obtained as shown in Figure-19 and Figure-20, respectively. The resulting harmonic spectrum is of the form as shown in Figure-21 and is measured using Fluke 345 power quality clamp meter.

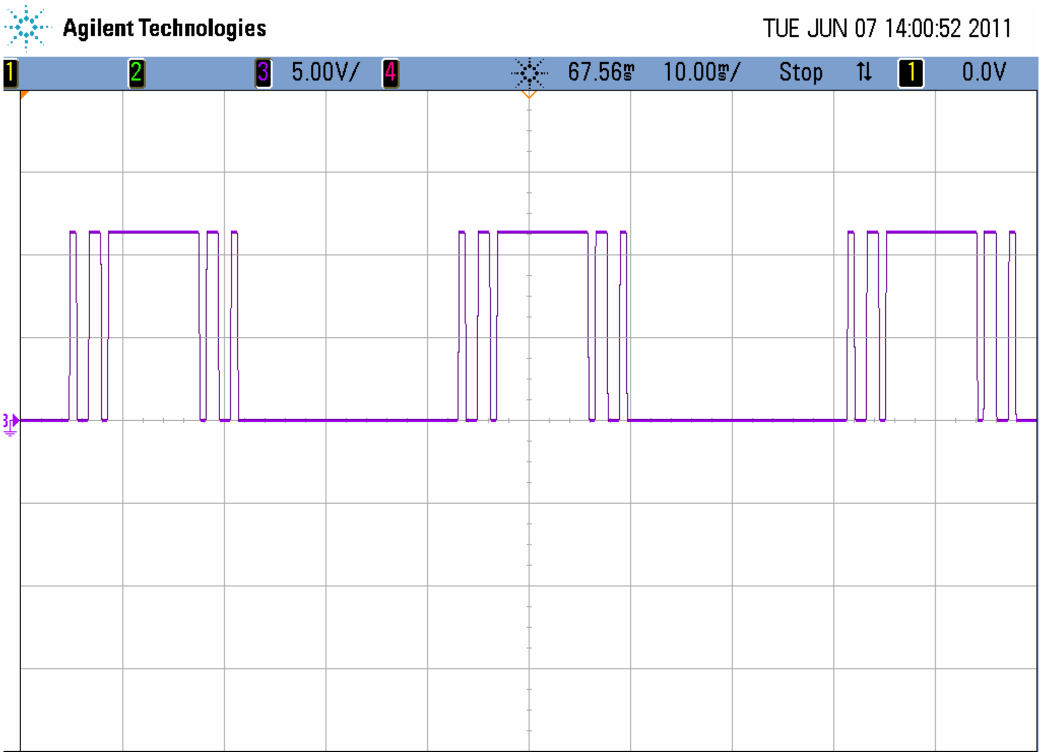


Figure-18. Gating pulse pattern for 5th, 11th SHE.

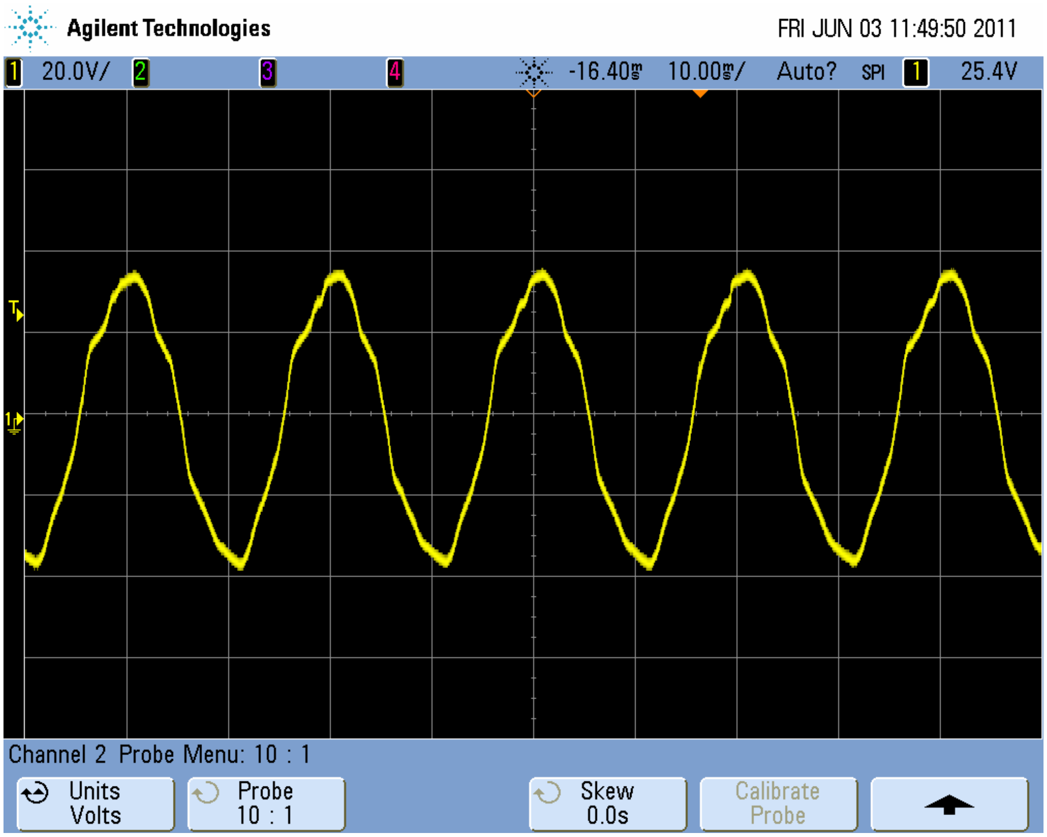


Figure-19. Line voltage for 5th and 11th harmonic elimination.

6. CONCLUSIONS

The independent switching angles for Selective Harmonic Elimination technique using "Resultant Theory" in the region between 0 and 30' degrees are evaluated and a generalized technique for PWM-SHE for two harmonic elimination has been developed in this work. These PWM patterns are given as the gating signals for the switches in CSI simulated using MATLAB/SIMULINK software. The simulation results approves that this generalized technique works successfully. The conventional selective harmonic elimination method will not be sufficient for eliminating the harmonics completely and hence can be used as methods for mitigating them. The simulation and the experimental results validate the same. The generalized PWM-SHE methodology proposed in this work is found to eliminate the selected harmonics completely. The implementation of generalized PWM-SHE need to be done either by logic circuits or by DSP processors.

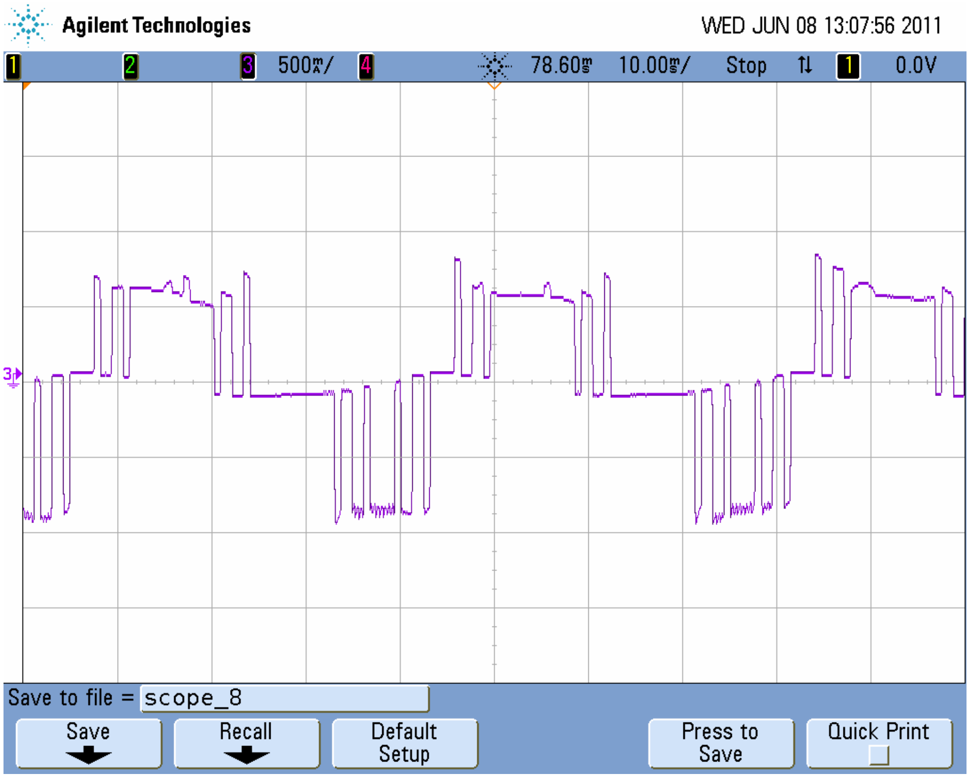


Figure-20. Line current for 5th and 11th harmonic elimination.

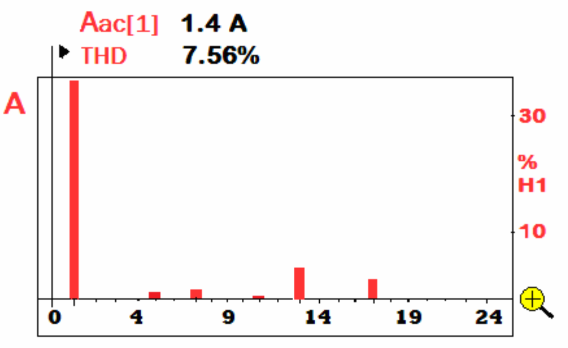


Figure-21. Harmonic spectrum of line current recorded.

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