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HIGHER TEST PATTERN COMPRESSION FOR SCAN BASED TEST VECTORS USING WEIGHTED BIT POSITION METHOD

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ABSTRACT

Present System on Chip (SoC) complexity has brought new challenges in volume of test pattern, low power testing and area complexity. This also shows that implementing huge test pattern and its corresponding storage space are the major problems. Due to this large number of test patterns the data transition time is also increased. This paper considers this problem in scan based test pattern. This proposed approach is based on the compression of huge test pattern by weighted bit position. Test patterns with unspecified bits are considered for specified values and partitioned into necessary weighted value. Depending upon weighted bit position specified test bit is compressed. This in turn reduces the test pattern for scan based testing. The proposed technique tested on ISCAS89 shows significant compression achieved on scan based test pattern.

Keywords: test pattern, scan, compression, weighted bit position, partition group.

1. INTRODUCTION

Today's System on Chip (SoC) complexity continues to grow in various design aspects. This challenge focuses on reducing the following parameters: test pattern, storage space, transition time, area complexity and power consumption. This evaluation shows that one of the major drawbacks of SoC design testing is its huge test pattern and its corresponding memory storage space. As per the above assessment huge test pattern is directly proportional to huge transition time and storage space resulting in voluminous test pattern and increasing manufacturing cost per chip testing in the semiconductor industry. This has led to exponential transition time and power consumption that has reached the limits of design reliability. This large test data also exceeds the memory capacity of automatic test equipment (ATE). This creates serious challenges for external ATE. These huge integrated complexities challenges the scan based testing of sequential circuits. By 2013, 1000X compression will be required as predicted by International Technology Roadmap for Semiconductor (IRTS) 2005 [1].

Test data compression can be classified into four different categories depending upon how test patterns are handled in compression method. If compression occurs on fixed number of test pattern and produces fixed number of compressed output, then it belongs to fixed to fixed category. Similarly, if compression occurs on variable test pattern and produces variable number of compressed output, then it belongs to variable to variable category. Other combination techniques such as fixed to variable test pattern and variable to fixed test pattern are also possible. Among these categories fixed to fixed scheme is chosen in this paper for weighted bit position analysis.

2. EXISTING METHODS

The problem of reducing test pattern for SoC has been analyzed from various aspects. Many techniques for scan based test pattern compression have been summarized in [2].

Reductions of Test patterns through scan chain concealment are discussed in [3], which uses XOR network in scan based design. Dual speed LFSR was proposed in [4] to reduce test pattern. This deals with two different LFSR. The normal LFSR is used as conventional LFSR reseeding and an additional LFSR is used to mask patterns. This also depends on the test pattern's transition density. Nonlinear combinational expanders are discussed in [5] and [6]. In paper [5], two alternatives are possible for techniques that do not have a complete encoding. Bypassing the dictionary requires adding an extra bit to each code word to indicate whether it is coded data or not. Automatic Test Pattern Generation (ATPG) should be constrained, so that it only generates test data that are contained in the dictionary as in [6]. This scheme is used to reduce the number of specified bits and the number of transitions at the same time. In the LFSR reseeding based test compression [7] method, the don't care bits in test pattern are filled with necessary pseudo-random code. It increases reasonable encoding efficiency of LFSR reseeding.

The different cases discussed above explain the complexities of achieving reduced test data compression. Of all the methods, fixed to fixed category promises to be the best in terms of achieving required compression. Here, the compression occurs on fixed test patterns producing fixed number of compressed output.

The rest of this paper is organized as follows: Section 3 presents the proposed method of finding partition, unspecified filling and weighted bit position technique. The proposed algorithm has also been described in Section 3. Experimental results for large ISCAS89 benchmark circuits are conducted in Section 4. Finally conclusion on this work is preceded in Section 5.

3. PROPOSED METHOD

In this section, the proposed method shows how to reduce the number of test pattern in scan based design. This paper proposes the concept of compression method by identifying its corresponding weighted bit position. Huge volume of test pattern is compressed to achieve reduced number of test patterns. Scan based input test pattern is considered for weighted bit position to achieve higher compression ratio. Weighted bit position compression technique proposed here is based on partitioning each and every scan test pattern into necessary value of weighted blocks.

Each and every input test pattern contains the combination of '0', '1' and 'X' (unspecified). Thus it is possible to identify the specified bit and unspecified bit in the given test patterns. Specified bits are the collection of '0' and '1' combination. In unspecified bits, only 'X' is identified. These unspecified bits are more in test patterns compared with specified bits. Every unspecified bit is assigned random values of '0' and '1' which lead to excessive transition activity in scan based design resulting in unsuitable selection.

In this paper, filling unspecified test pattern with specified binary values is considered using Zero filling and One filling methods. Zero filling specifies all unspecified bits to corresponding '0' value. For one filling, it specifies all unspecified bits to corresponding '1' value. This above method promises to attain low transition in scan based design.

Table-1 shows the relationship between weighted levels with bit partition of test pattern for 7 levels only. It is possible to increase both weight level values and partition values. For an example Weight 4 shows the level of "8 4 2 1" and weight 5 shows the level of "16 8 4 2 1". Thus for weight 4, it is possible to compress 16 test bits. Thus depending upon weight level, test pattern can be compressed for appropriate values.

Table-1. Weighted levels Vs bit partition.

Weighted levels	Test pattern bit partition
3	9
4	16
5	32
6	64
7	128

Following example illustrates the procedure of the proposed algorithm named weighted bit position based compression method. Given test patterns TP1 contain 32 test vectors with the combination of '0', '1' and 'X'. Unspecified bit (X) is filled by zero fill (or) one fill technique. If one fill (TP1 (One)) and zero fill (TP1 (Zero)) technique leads to a sequence of consecutive 1's or consecutive 0's then high compression can be achieved.

In such techniques weighted bit position (as described previously) can be applied for required compression. Contrary to this we can't achieve our expected compression if we have a random combination of '0' and '1' among a given stream of 32 bits. As a sample demonstration, it is examined below that in TP1 (C-Zero) second half of bit is compressed to "1111" by calculating its weighted bit position satisfying our expectation of achieving desired compression.

TP1 = 0 0 1 0 1 1 1 1 1 1 0 0 0 0 X X
0 X X X X 0 0 0 0 0 0 0 0 0 0 X X

TP1 (One) = 0 0 1 0 1 1 1 1 1 1 0 0 0 0 1 1
0 1 1 1 1 0 0 0 0 0 0 0 0 0 1 1

TP1 (zero) = 0 0 1 0 1 1 1 1 1 1 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

TP1 (C-zero) = 0 0 1 0 1 1 1 1 1 1 0 0 0 0 0 0
1 1 1 1

The following algorithm describes the process of the prescribed method

Algorithm weighted bit position partitioning
(tlength, tlines, tp, p, ctp)

Input
tlenghth = Length of each test pattern
tlines = Number of test pattern lines
tp = Total test pattern contains tlines each with tlength
p = Number of test pattern partition

Output
ctp = Compressed test pattern

initialize I = 0
for each line in tp

a). Find partition size:
If (tlength % p) = 0 then
Split the line in the exact 'partition' number. Each consists of exactly (tlength/p) number of test bits. Use this test bit for compression

Else
Split the line into partition number, and find remaining bits as
n = (tlength % p). Set the size for the first (p-1) number as ((tlenegth/p) +1) number of bits. For the last partition append (p-n) number of 'X' and make its size as ((tlenegth/p) +1). Use this test bit for compression
b). Filling unspecified test bits with corresponding zero (or) one fill technique
c). Finding proper weighted bit partitioning
d). Calculate (Ctp) compression ration

The proposed algorithm is considered for compression based on weighted bit position technique. This algorithm focuses on four major stages as follows: Finding partition size, filling unspecified bits, identifying proper weighted bit position and calculating compression ratio.

In the initial stage, length of scan test pattern (tlength) is partitioned into necessary partition (p). If 'tlength' is divisible by 'p' then test bit is considered for compression. If 'tlength' is not divisible by proper 'p',

then consider for appending unspecified bits value (X). This will reduce unnecessary transition in scan based design. In the second stage unspecified bits (X) are filled with proper zero fill (or) one fill technique. This increases compression ratio in scan based design. In the third stage proper weighted bit position is applied, as discussed above. In the last stage appropriate weighted bit position partition is considered for compression process.

4. EXPERIMENTAL RESULTS

This section describes the proposed experimental performance, to evaluate the efficiency of test pattern compression. This is achieved by partitioning of test pattern by weighted bit positioning technique. The proposed method is implemented using VHDL and C language and tested with full scan version of the ISCAS89 benchmark circuits. Test patterns used in these experiments were obtained by using Mintest dynamic compaction algorithm [8]. Table-2 describes the number of test patterns, number bits per patterns and total number of bits for different ISCAS89 circuits. All the provided test patterns target at 100% fault coverage. Compression ration (CR) is given as, Difference between total benchmark test patters by proposed test patterns and divided by Total benchmark test pattern. Compression ratio (CR) = (Total pattern - Proposed pattern) / (Total pattern).

Each and every test pattern was considered with corresponding weighted bit position and partitioned into several blocks. Depending upon weighted bit position partitioning, the test patterns are considered for compression ratio.

Table-2. ISCAS89 benchmark circuits for analyzing test patterns [8].

ISCAS circuit	No of test pattern	No of bits Per pattern	Total Number of bits
S5378	111	214	23754
S9234	159	247	39273
S15850	126	611	76986

Table-3 shows the different weighted level bits for one fill method related to ISCAS89 benchmark circuits. The compression ratio for different weighted level bits is given in percentage.

Table-3. Experimental results for various weighted level bits (%).

ISCAS circuit	4-bit Weighted level	5-bit Weighted level	6-bit Weighted level	7-bit Weighted level
S5378	30.8	17.2	14	0.3
S9234	18	0.7	0.3	0
S15850	41.2	37.5	25.8	18.4

Figure-1 represents the experimental results of ISCAS89 benchmark circuit for one fill technique.

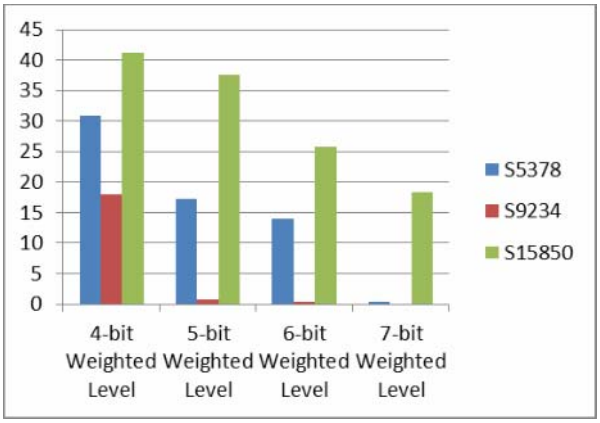

Figure-1. Experimental results for weighted levels and compression ratio for one fill method.

Table-4 shows experimental results for various weighted levels based on one fill and zero fill techniques. Higher compression ratio is observed in 4 bit weighted level compared with other weighted levels. Table-4 shows that proposed method has an increase in 5% to 16% when compared with Dual LFSR [4] method.

In Figure-2, the experimental results for proposed weighted bit position are compared with existing method Dual LFSR [4]. Proposed weight level is considered for 4 and its corresponding partition is 16 as in Table-1. Results show the compression ratio (CR) comparison for various ISCAS89 benchmark circuits. It is well understood that the proposed algorithm achieves more compression ratio than the existing method.

Table-4. Comparison of dual-LFSR [4] with proposed method (%).

ISCAS circuit	Dual LFSR [4]	One fill in proposed method	Zero fill in proposed method
S5378	25	30	30.8
S9234	24	22.3	18
S15850	25	38.9	41.2

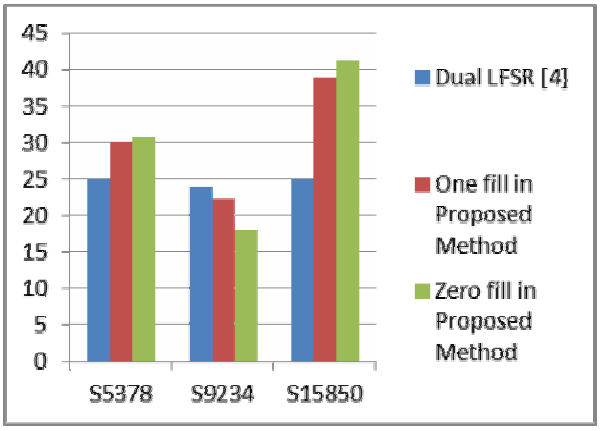

Figure-2. Comparison with existing dual -LFSR [4].

5. CONCLUSIONS

The present challenge of reducing test pattern is one of the most important tasks in SoC testing. It is very particularly noticed in scan based test patterns. This paper proposes an efficient compression algorithm based on weighted bit position. The proposed algorithm partitions each and every test pattern. Then each partition is carefully considered for including zero and one filling method to unspecified bits. Finally weighted bit position is considered for compression. Experimental results for the ISCAS89 benchmark circuits show that 5% to 16% of test pattern is reduced significantly. This also promises that memory storage space and transition time is reduced.

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