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# INVESTIGATION OF $f_t$ AND NON-QUASI-STATIC DELAY IN CONVENTIONAL AND JUNCTIONLESS MULTIGATE TRANSISTORS USING TCAD SIMULATIONS

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**ABSTRACT**

In this paper, a comparative study between conventional and junctionless multi-gate transistors is made with respect to unity gain cut-off frequency ($f_t$) and non-quasi static (NQS) delay using TCAD simulations. The comparison is done with and without leakage current ($I_{OFF}$) matching. Two structures, typical FinFET like trigate structure and gate all around structure with circular cross section, are considered in this study. It is found that compared to junctionless transistor, conventional devices show better $f_t$ and lesser NQS delay in both trigate and GAA transistors. When the $I_{OFF}$ matching constraint is met by adjusting the gate electrode work function, the conventional devices show no or weak $I_{OFF}$ dependency due to screening effect whereas junctionless devices show strong dependency on $I_{OFF}$, with respect to $f_t$ and NQS delay.

**Keywords:** triple gate, junctionless transistor, $f_t$, NQS, GAA, TCAD.

## 1. INTRODUCTION

In recent years, multigate field-effect transistors (MuGFETs) with higher channel controllability such as double-gate FinFETs (S. Nuttinck *et al*., 2007; A. Kranti *et al*., 2007a), triple-gate FinFETs (A. Dixit *et al*., 2005; A. Kranti *et al*., 2007b), fully depleted silicon-on insulator MOSFETs (F. Balestra *et al*., 1987; F. E. Mamouni *et al*., 2008), and gate-all-around (GAA) silicon nanowire (SNW) MOSFETs (S. H. Lee *et al*., 2009; Deyuan Xiao *et al*., 2009; Wei-Ting Lai *et al*., 2011) have been proposed as the solutions bearing immunity to SCEs, which enables to expect continuous downscaling of the devices. Recently, Junctionless (JL) transistors have been proposed as a novel structure to make a breakthrough for the junction-induced design issues (J.P. Colinge *et al*., 2010a; C.W. Lee *et al*., 2010a; J.P. Colinge *et al*., 2010b). To have a good electrostatic control and good sub threshold characteristic, GAA nanowire junctionless transistors of 3 nm gate length has been investigated (L.Ansari *et al*., 2010).

Comparative study between conventional and junctionless multigate transistor have already been explored in literature with respect to DC characteristics like leakage current, drain induced barrier lowering (DIBL), gate induced drain leakage (GIDL), threshold voltage and sub threshold slope (C.W. Lee *et al*., 2010b; C.W. Lee *et al*., 2009; C.W. Lee *et al*., 2010c; S.J. Choi *et al*., 2011). Analog/RF performance metrics are yet to be compared in detail. Recently the intrinsic gain of trigate junctionless transistors are compared with conventional inversion mode devices (R.T. Doria *et al*., 2011). Various RF parameters like $f_t$, $f_{max}$, transport time delay, distributed channel resistances are compared for junctionless SNW with conventional SNW MOSFETs (S. Cho *et al*., 2011).

In this paper, we study $f_t$, and non-quasi-static delay of the conventional and junctionless multigate transistors. Two different device structures, triple-gate (TG) FinFET and gate-all-around (GAA) transistor with the circular cross section have been considered here. To make this comparison more fair and effective, the leakage current of the two sets of device have been matched. This paper is organized as follows. Next section describes the simulation methodology for the two sets of novel device structures which are of interest. Section III discusses the simulation results and discussions. Finally section IV provides conclusion.

## 2. SIMULATION METHODOLOGY

### 2.1 TCAD simulator

Sentaurus TCAD simulator from Synopsys (Synopsys, 2008-09) is used for this study. The simulator has many facilities and the following modules are used in this study.

- **Sentaurus structure editor (SDE):** This is used to create the device structure, to define doping, to define contacts, and to generate mesh for device simulation.
- **Sentaurus device simulator (SDEVICE):** This is used to simulate all DC, AC and transient characteristics. In the simulations, Fermi-Dirac statistics, modified local density approximation for carrier confinement, and field-dependent mobility are used.
- **Tecplot and Inspect:** These are used to view the results.

### 2.2 Generation of structure

The device structures are generated using SDE. Figures 1 and 2 show conventional triple gate (TG) and junctionless TG transistors, respectively with its side and top views. Figures 3 and 4 depict the conventional and junctionless gate-all-around (GAA) transistors, respectively with its circular cross-sectional and top views.

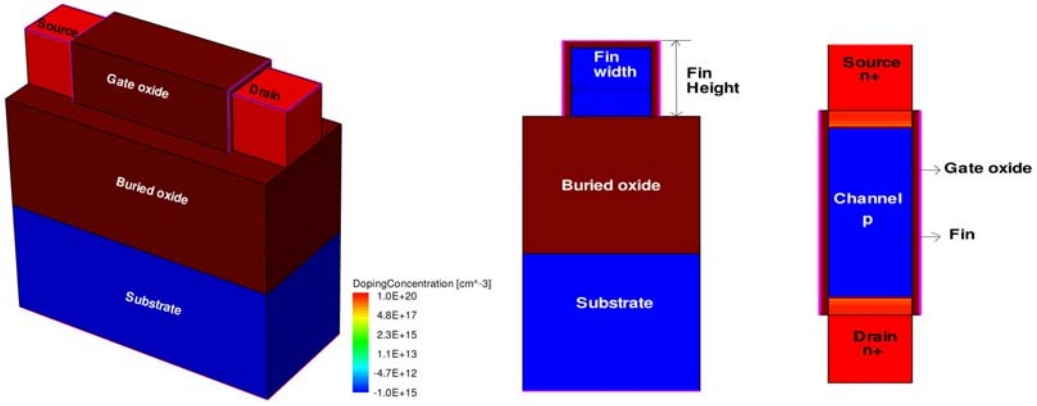


**Figure-1.** 3-D structure of conventional TG with their cross -sectional views (both side and top views).

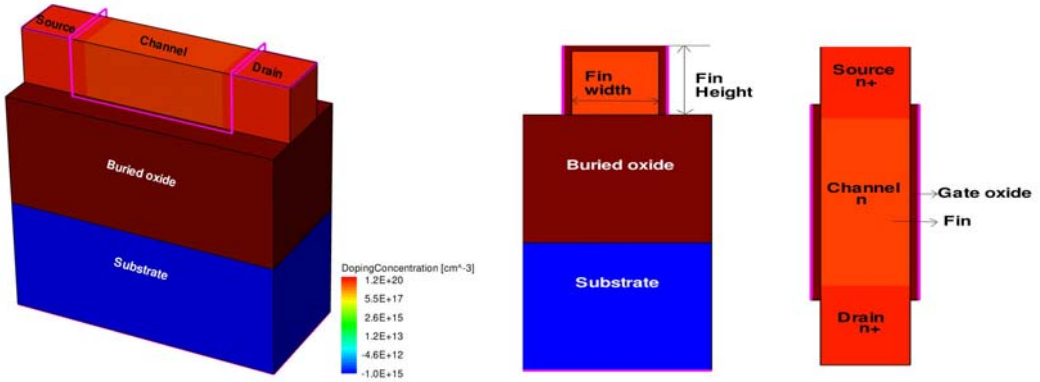


**Figure-2.** 3-D structure of junctionless TG with their cross-sectional views (both side and top views).

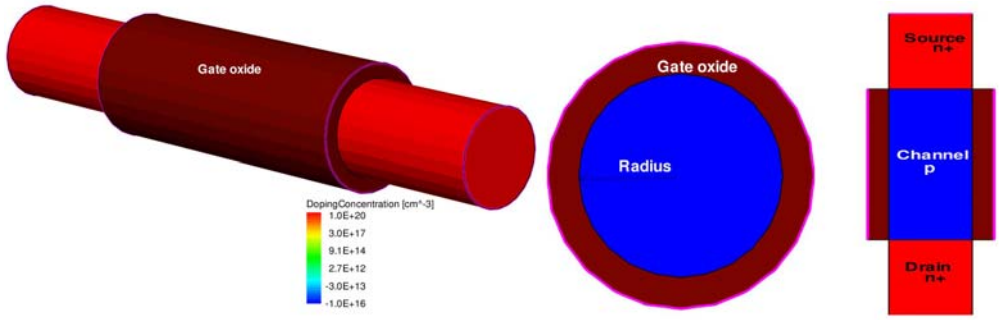


**Figure-3.** 3-D structure of conventional GAA with their cross -sectional views (both side and top views).

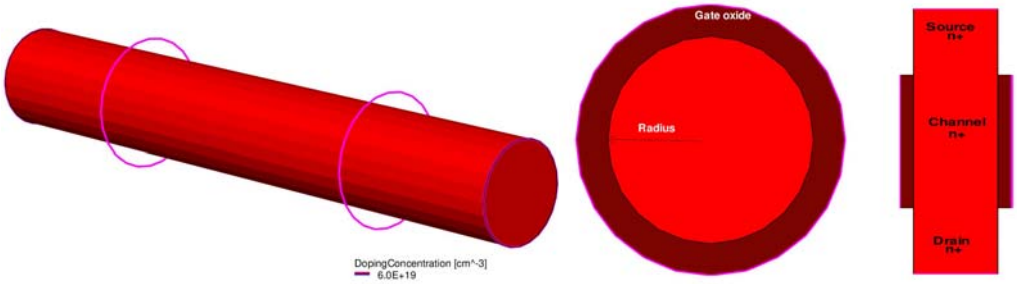


**Figure-4.** 3-D structure of junctionless GAA with their cross-sectional views (both side and top views).

**2.3 Simulation of $I_d$-$V_g$ characteristics**

This section presents calibration and simulation of $I_d$-$V_g$ characteristics of all the four devices i.e., (i) conventional TG transistor (ii) junctionless TG transistor (iii) conventional GAA and (iv) junctionless GAA transistor. The current values of all the four devices are calibrated against the published experimental results by tuning the Silicon parameter library file (C.W. Lee *et al*., 2010c; M.H. Chiang *et al*., 2008; ITRS, 2010). After calibration, the device dimensions are brought to the requirements as given in Tables 1 and 2. Figure-5 shows the simulated $I_d$-$V_g$ characteristics for triple gate (TG) and gate-all-around (GAA) devices as per the dimensions given in Tables 1 and 2.

**Table-1.** Dimensions of the conventional TG and junctionless TG transistors.

| **Process parameters** | **Conventional TG** | **Junctionless TG** |
|---|---|---|
| Gate length ($L_g$) | 30 nm | |
| Fin width (W) | 10 nm | |
| Fin height (H) | 10 nm | |
| Gate oxide thickness ($T_{ox}$) | 1 nm | |
| Channel doping ($N_{ch}$) | 1x15/cm$^3$ | 4x19/cm$^3$ |
| Source/drain doping ($N_{sd}$) | 1x20/cm$^3$ | 8x19/cm$^3$ |
| Gate work function (WF) | 4.31 | 5.33 |
| Supply voltage ($V_{dd}$) | 1 V | |

**Table-2.** Dimensions of the conventional GAA and junctionless GAA transistors.

| **Process parameters** | **Conventional GAA** | **Junctionless GAA** |
|---|---|---|
| Gate length ($L_g$) | 17 nm | |
| Diameter (D) of nanowire | 5 nm | |
| Gate oxide thickness ($T_{ox}$) | 0.77 nm | |
| Channel doping ($N_{ch}$) | 1x16/cm$^3$ | 6x19/cm$^3$ |
| Source/drain doping ($N_{sd}$) | 1x20/cm$^3$ | 6x19/cm$^3$ |
| Gate work function (WF) | 4.27 | 4.63 |
| Supply voltage ($V_{dd}$) | 0.8 V | |

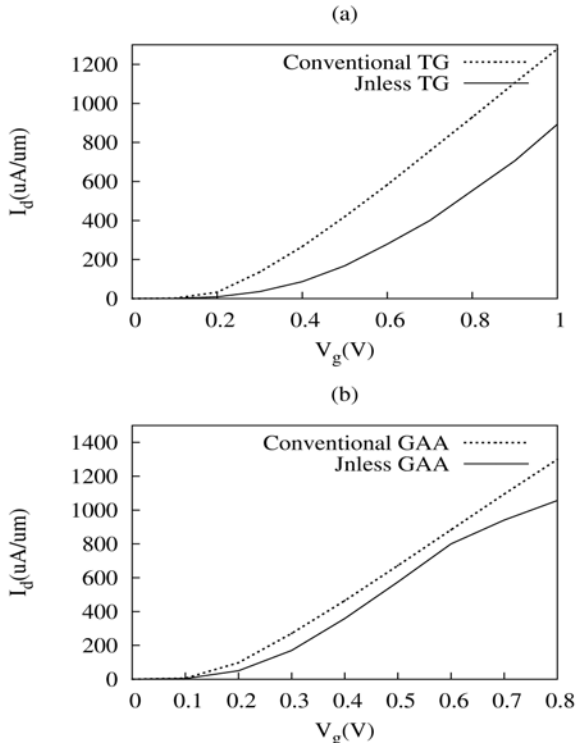


**Figure-5.** Simulated $I_d$-$V_g$ characteristics of (a) TG of gate length 30 nm with matched $I_{off}$ =43 nA/ µm and (b) GAA devices of gate length 17 nm with matched $I_{off}$ 100nA/ µm.

### 2.4 $f_t$ and NQS delay simulation methodology

Standard AC simulations are done in device simulator and $f_t$ is extracted when $|Y_{21}/Y_{11}|$ equals one, and it strongly depends on the gate bias. At various gate biases $f_t$ is calculated and the maximum of them is taken as $f_t$.

The RF non-quasi-static delay in the devices is studied using transient simulation. To evaluate the small signal response, a small time varying ac signal along with a DC bias is applied to the gate. The delay between the applied gate signal drain current is measured to get the NQS delay.

## 3. RESULTS AND DISCUSSIONS

### 3.1 Effect of gate length scaling on $f_t$

#### 3.1.1 Tri-gate devices

The effect of channel length scaling on conventional TG and junctionless TG has been analyzed with and without $I_{OFF}$ matching. The gate length is varied from 20 nm to 40 nm. Figure-6a shows the variation of $f_t$ with respect to gate length for conventional TG and junctionless TG transistor with and without $I_{OFF}$ matching. $I_{OFF}$ is varied from 0.1 nA to 10 nA. It can be seen that $f_t$ of conventional TG is larger than $f_t$ of junctionless TG. It has been predicted in (R.T. Doria *et al*., 2011) that junctionless devices would show lesser $f_t$ compared to conventional devices due to lower on current. The simulations also show the same behavior. An interesting observation is that $f_t$ does not show any dependency on $I_{OFF}$ in conventional device whereas junctionless shows $I_{OFF}$ dependency. Specified $I_{OFF}$ values were achieved by adjusting the gate work function. Conventional devices do not show any high frequency dependency on work function due to screening effect (C.H. Hwang *et al*., 2009) But the junctionless devices do not show any such screening effect i.e., $f_t$ of junctionless devices vary with work function. It can be also observed that the rate of increase in $f_t$ when channel length is decreased is slightly more for conventional trigate device compared to junctionless device. The popular $1/L^m_g$ is used to model $f_t$ versus $L_g$ plot. Modeled 'm' value is given in Figure-7 for various $I_{OFF}$s.

#### 3.1.2 Gate-all-around (GAA) devices

Cho *et al*., studied $f_t$ of conventional and junctionless GAA devices at 30 nm and reported lower $f_t$ values for junctionless GAA devices. In this study, the effect of scaling on $f_t$ for GAA devices has been analyzed for gate lengths ranging from 20 nm to 40 nm and Figure-6b depicts the $f_t$ versus $L_g$ plot for GAA devices. It can be observed that junctionless devices show smaller $f_t$ compared to conventional devices for all the gate lengths.

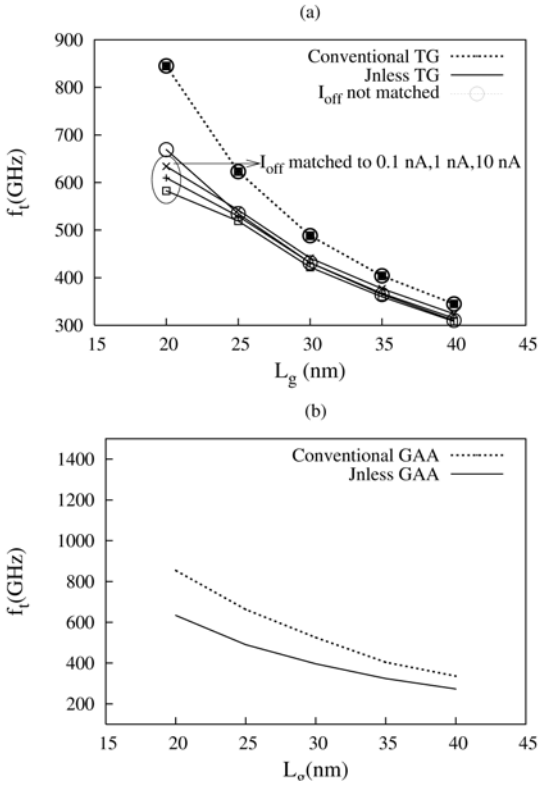


**Figure-6.** Variation of $f_t$ w.r.t $L_g$ for (a) Conventional TG (dotted lines), junctionless TG (solid lines) for $I_{off}$ = 0.1nA, 1nA and 10nA and (b) Conventional GAA (dotted lines), junctionless GAA (solid lines).

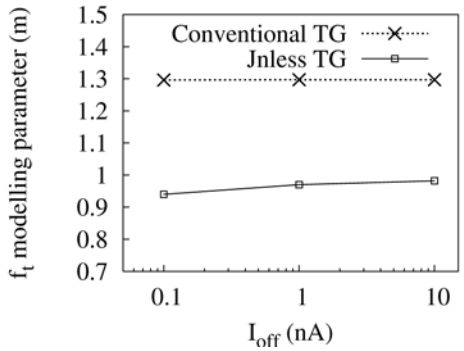


**Figure-7.** Plot between $f_t$ modeling parameter and off current.

### 3.2 Effect of scaling on non-quasi static (NQS) delay

It is known that non-quasi static (NQS) effect i.e., delay plays an important role in RF circuits. In this paper, NQS delay effect is analyzed for tri-gate and GAA devices as they undergo scaling.

#### 3.2.1 Tri-gate devices

Figure-8a shows NQS delay as a function of frequency for two different gate length TG devices. For the given frequency, junctionless devices show higher NQS delay compared to conventional devices. This is expected because of the lower gate over drive in junctionless devices compared to conventional devices. With $I_{OFF}$ matching the NQS performance of junctionless devices degrades further where as conventional devices are insensitive to work function as discussed previously and thereby their NQS performance does not degrade. The simulation results plotted in Figure-8a depicts this.

#### 3.2.2 GAA devices

Figure-8b depicts NQS delay as a function of frequency for three different gate length GAA devices. It can be seen that junctionless devices once again show more delay compared to that of conventional GAA devices.

### 4. CONCLUSIONS

A comparative study between conventional and junctionless multi-gate transistors was made with respect to unity gain cut-off frequency ($f_t$) and non-quasi static (NQS) delay. The comparison was done with and without leakage current ($I_{OFF}$) matching. Two structures, FinFET like trigate structure and gate all around structure with circular cross section, were studied here. It was found that compared to junctionless transistor, conventional devices show better $f_t$ and lesser NQS delay in both trigate and GAA transistors. When the $I_{OFF}$ matching constraint was met by adjusting the gate electrode work function, the conventional devices show no or weak $I_{OFF}$ dependency due to screening effect whereas junctionless devices show strong dependency on $I_{OFF}$, with respect to $f_t$ and NQS delay.

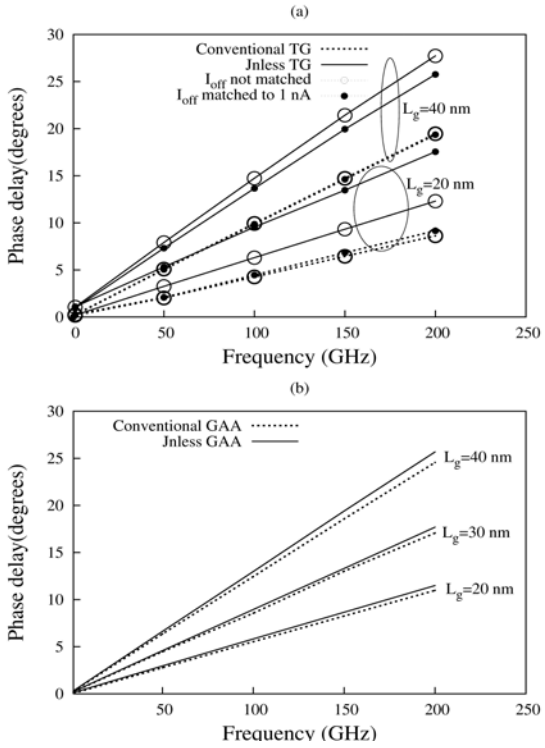


**Figure-8.** Variation of phase delay w.r.t frequency for (a) Conventional TG (dotted lines), junctionless TG (solid lines) for with and without $I_{off}$ matching (b) Conventional GAA and junctionless GAA.

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