VOL. 7, NO. 9, SEPTEMBER 2012 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences


www.arpnjournals.com

COMPARATIVE STUDY ON VARIOUS BIPOLAR PWM STRATEGIES FOR THREE PHASE FIVE LEVEL CASCADED INVERTER

Balamurugan C. R.[1], Natarajan S. P.[2] and Padmathilagam V.[3]
[1]Department of Electrical Engineering, Arunai Engineering College,Tiruvannamalai, Tamilnadu, India
[2]Department of Instrumentation Engineering, Annamalai University, Annamalainagar, Tamilnadu, India
[3]Department of Electrical Engineering, Annamalai University, Annamalainagar, Tamilnadu, India
E-Mail: spn_annamalai@rediffmail.com

ABSTRACT

This paper presents the different types of bipolar Pulse Width Modulation (PWM) strategies for the chosen Cascaded Multi Level Inverter (CMLI). The main purpose of multilevel inverter is to produce approximate sinusoidal wave voltage output using the method of superimposing multiple voltage steps. Due to their ability to synthesize a higher output voltage than the voltage rating of each switching device without a transformer, multilevel inverters are suitable topologies due to low Total Harmonic Distortion (THD) and low voltage stress (dv/dt) which minimize Electro Magnetic Interference (EMI) and also switching losses compared to traditional inverters. In this paper, a cascaded multilevel inverter is controlled with Sinusoidal PWM (SPWM) technique, Third Harmonic Injection (THI) PWM technique and Sixty degree PWM technique with Sub harmonic PWM (SHPWM), Phase Shift (PS), Variable Frequency (VF), Carrier Overlapping (CO), Phase Opposition and Disposition (POD) and Alternative Phase Opposition and Disposition (APOD) modulation strategies. The variation of THD in the output voltage is observed for various modulation indices. Simulations are performed using MATLAB-SIMULINK. It is observed that SHPWM provides output with relatively low distortion for THIPWM and 60 degree PWM references where as PSPWM performs better for sine reference. It is also seen that COPWM is found to perform better since it provides relatively higher fundamental RMS output voltage for all references.

Keywords: THD, CMLI, SHPWM, THIPWM, 60 degree PWM, PD, PS, VF, CO.

INTRODUCTION

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled AC drives in the megawatt range are usually connected to the medium voltage network. Recently, multilevel inverters have been drawing growing attention due to its high voltage operating capability, possible suitability for high power application and advantages in EMI problems. Donald Grahame Holmes and McGrath [1] proposed opportunities for harmonic cancellation with carrier based PWM for two level and multilevel cascaded inverters. Loh *et al*., in [2] introduced synchronization of distributed PWM cascaded multilevel inverter with minimal harmonic distortion and common mode voltage. Mariethoz and Rufer [3] analysed resolution and efficiency improvements for three phase cascaded multilevel inverters. Xianglian Xu *et al*., in [4] proposed phase shift SPWM technique for cascaded multilevel inverter. Azli and Choong [5] analyzed the performance of a three phase cascaded H-bridge multilevel inverter. Shanthi and Natarajan proposed carrier overlapping PWM methods for single phase cascaded five level inverter [6]. Roozbeh Naderi and Rahomati [7] proposed phase shifted carrier PWM technique for general cascaded inverters. Gierri Waltrich and Barbi [8] introduced three phase cascaded multilevel inverter using power cells. Urmila and Subbarayudu [9] analyzed comparative study of various pulse width modulation techniques. Gierri Waltrich and Barbi [10] introduced also three phase cascaded multilevel inverter with commutation sub-cells. Konstantinou *et al*., [11] proposed harmonic elimination control of a five level DC-AC cascaded H-bridge hybrid inverter. Farid Khoucha *et al*., [12] proposed comparison of symmetrical and asymmetrical three phase H-bridge multilevel inverter for direct torque control induction motor drives. This literature survey reveals few papers only on various PWM techniques and hence this work presents a novel approach for controlling the harmonics of output voltage of chosen MLI employing Sinusoidal, THI and 60 degree references for different PWM switching strategies. Simulations are performed using MATLAB-SIMULINK. Harmonics analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

MULTILEVEL INVERTER

Multilevel power converter is a generic term applied to power converters with topologies capable of synthesizing multi-tier voltage waveforms and processing high voltage by means of series connection of active devices to three or more discrete DC voltage sources. Ingenious interconnection of power devices to split DC rail increases the voltage handling capability of these converters for given power devices. Multi-tier voltages synthesized by these converters show improved spectral quality of voltage at the output of multilevel inverters. Figure-1 shows a configuration of the three phase five level cascaded type multilevel inverter. The CMLI is unique when compared to other types of multilevel inverter in the sense that it consists of several modules that are require separate DC sources. Compared to other types of multilevel inverters, the CMLI requires less number of components with no extra clamping diodes or voltage balancing capacitors that only further complicate the

overall inverter operation. The simpler modular structure not only allows practically unlimited number of levels for the CMLI by stacking up the modules but also facilitates its packaging.

The operation of the CMLI can be easily understood. The load voltage is equal to the summation of the output voltage of the respective modules that are connected in series. The number of modules (M) which is equal to the number of DC sources required depends on the total number of positive, negative and zero levels (m) of the CMLI. It is usually assumed that m is odd as this would give an integer valued M. In this work, load voltage consists of five levels which include $+2V_{DC}$, $+V_{DC}$, 0, $-V_{DC}$ and $-2V_{DC}$ and the number of modules needed is 2. The following equation gives the relation between M and m is M = (m-1)/2.

The gate signals for chosen five level cascaded inverter are simulated using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index m_a and for various PWM strategies. Figure-2 shows a sample SIMULINK model developed for SHPWM method. The simulation results presented in this work in the form of the outputs of the chosen multilevel inverter are compared and evaluated.

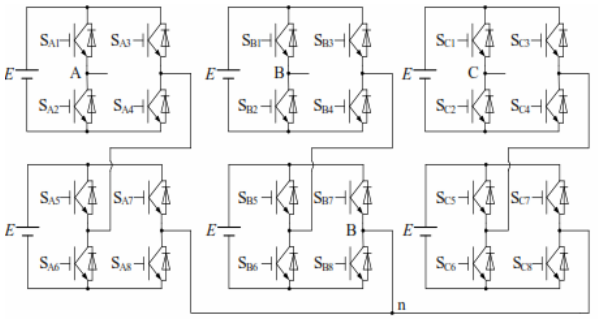

Figure-1. A three phase five level cascaded multilevel inverter

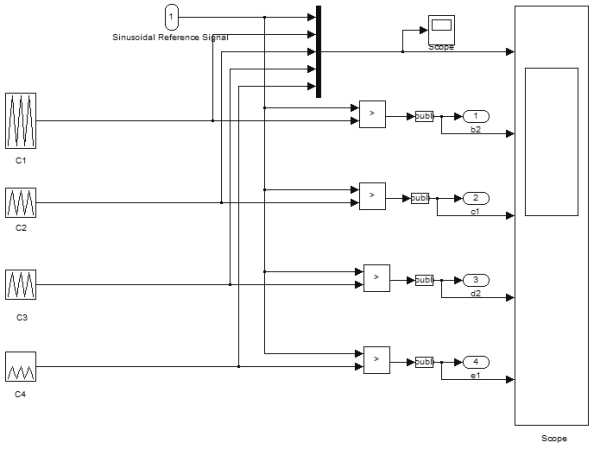

Figure-2. Sample PWM generation logic using SIMULINK model developed for SHPWM technique.

MODULATION STRATEGIES

Development of PWM control strategies concerns the development of techniques to reduce the THD of the output. It is generally recognized that increasing the switching frequency of the PWM pattern reduces the lower frequency harmonics by moving the switching frequency carrier harmonics and associated sideband harmonics further away from the fundamental frequency component. The modulating/reference wave of multilevel carrier based PWM strategies can be sinusoidal or third harmonic injection or 60 degree PWM signal. As far as the particular reference wave is concerned, there is also multiple CFD including frequency, amplitude, phase angle of the reference wave. This paper focuses on multicarrier based sinusoidal PWM strategies; third harmonic injection PWM strategies and sixty degree PWM strategies which have been used in chosen three phase cascaded MLI. The following strategies are employed in this study.

Sub harmonic PWM (SHPWM) technique

In SHPWM all the carriers are in phase. For an m-level inverter using bipolar multicarrier technique, (m-1) carriers with the same frequency f_c and same peak-to-peak amplitude A_c are used. The reference waveform has amplitude A_m and frequency f_m and it is cantered about the zero level. The reference wave is continuously compared with each of the carrier signal. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices switch off. The frequency ratio m_f is defined in the bipolar PWM strategies as follows: $m_f = f_c/f_m$. The amplitude modulation index m_a is defined for this method as: $m_a = 2A_m/(m-1)Ac$. The SHPWM method yields only odd harmonics for odd m_f and yields odd and even harmonics for even m_f, Figure-3 shows the multicarrier arrangement for SHPWM method for $m_a = 0.8$ and $m_f = 40$.

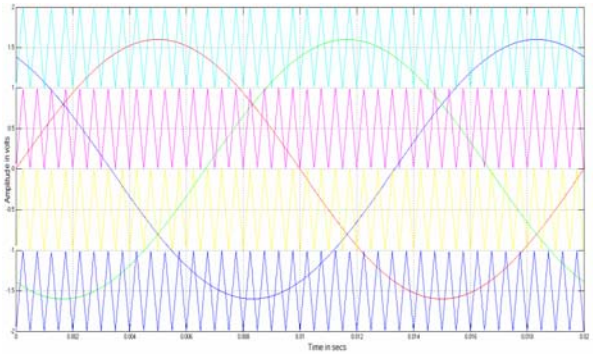

Figure-3. Multicarrier arrangement for SHPWM technique.

Phase shift PWM (PSPWM) technique

The phase shift multi-carrier PWM technique used in this work four carrier signals of the same amplitude and frequency which are shifted by 90 degrees to one another to generate the five level inverter output voltage. The gate signal for the cascaded inverter can be derived directly from the PWM signals. There is a certain degree of freedom in the allocation of the carriers to the

inverter switches. In the case of sinusoidal reference (i) for odd m_f the waveforms have odd symmetry resulting in even and odd harmonics and (ii) for even m_f PSPWM waves have quarter wave symmetry resulting in odd harmonics only. But in the case of 60 degree reference, the waveforms have odd symmetry resulting in only odd harmonics. Figure-4 shows the multicarrier arrangement for PSPWM method for m_a = 0.8 and m_f = 40. The amplitude modulation index is defined for this strategy as: $m_a = A_m/ (A_c/2)$.

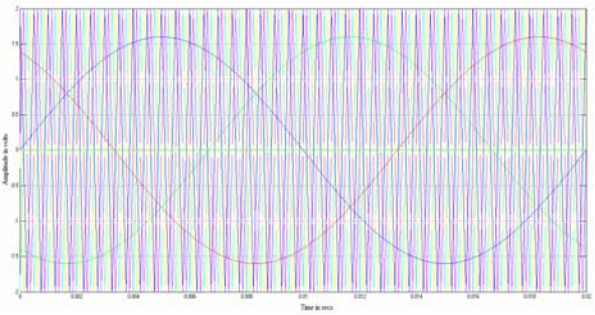

Figure-4. Multicarrier arrangement for PSPWM technique.

Variable frequency PWM (VFPWM) technique

The number of switching for upper and lower devices of chosen MLI is much more than that of intermediate switches in SHPWM using constant frequency carriers. In order to equalize the number of switching for all the switches, variable frequency PWM strategy is used as illustrated in Figure-5, in which the carrier frequency of the intermediate switches is properly increased to balance the numbers of switching for all the switches. The amplitude modulation index $m_a = 2A_m/ (m-1) Ac$. Figure-5 shows the multicarrier arrangement for VFPWM method for m_a = 0.8, m_f = 40 (upper and lower switches), m_f = 80 for intermediate switches.

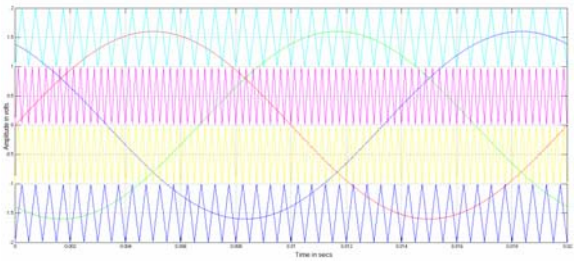

Figure-5. Multicarrier arrangement for VFPWM technique.

Carrier overlapping PWM (COPWM) technique

The COPWM method utilizes the CFD of vertical offsets among carriers. The principle of COPWM is to use several overlapping carriers with single modulating signal. For an m level inverter, m-1 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlap each other. The overlapping vertical distance between each carrier is $A_c/2$ in this work. The reference wave has the amplitude A_m and frequency f_m and it is centered in the middle of the carrier signal. The amplitude modulation index $m_a = A_m/ (m/4) Ac$. The vertical offset of carriers for chosen five level inverter can be as illustrated in Figure-6. It can be seen that the four carriers are overlapped with other and the reference sinusoidal wave is placed at the middle of the four carriers. Figure-6 shows the multicarrier arrangement for COPWM strategy for m_a = 0.8 and m_f=40.

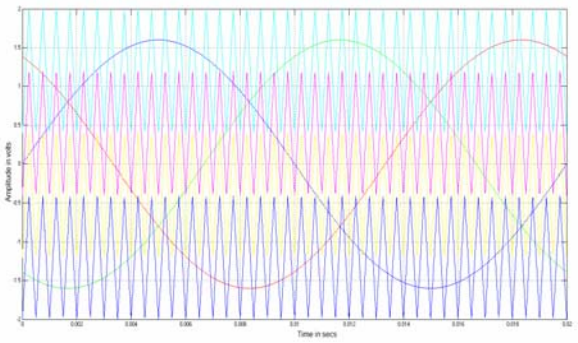

Figure-6. Multicarrier arrangement for COPWM technique.

In this paper, m_f = 40 and m_a is varied from 0.6 to 1. m_f is chosen as 40 as a trade off in view of the following reasons:

a) to reduce switching losses (which may be high at large m_f)
b) to reduce the size of the filter needed for the closed loop control, the filter size being moderate at moderate frequencies
c) to effectively utilize the available dSPACE system for hardware implementation

Third harmonic injection reference PWM

In this technique, a third harmonic component is superimposed on the fundamental. The addition of third harmonic makes its possible to increase the maximum amplitude of fundamental in the reference and in the output voltages. Third harmonic technique is preferred in three phase applications since cancellation of third harmonic component and better utilization of DC supply can be achieved. Harmonic elimination techniques, which are suitable for fixed output voltage, increase the order of harmonics and reduce the size of output filter. But these advantages should be weighed against increase in switching losses of power devices and iron losses in transformer due to high harmonic frequencies. It is not always necessary to eliminate triplen harmonics which are not normally present in three phase connections. So in three phase inverters, it is preferable to eliminate fifth, seventh and eleventh harmonics of output voltages so that the lowest order harmonics will be thirteen. Carrier arrangement with third harmonic injection reference PWM strategy is as shown in Figures 7-11.

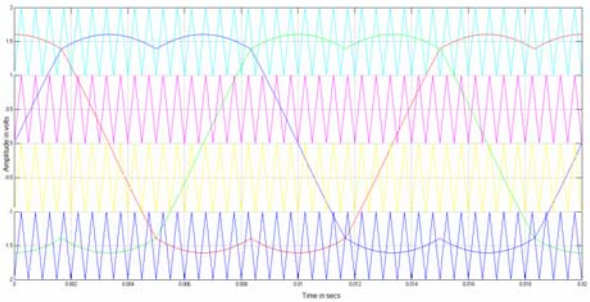

Figure-7. Multicarrier arrangement for SHPWM technique.

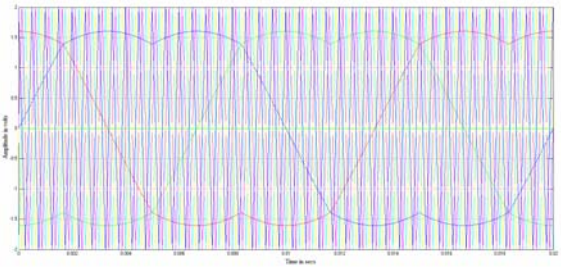

Figure-8. Multicarrier arrangement for PSPWM technique.

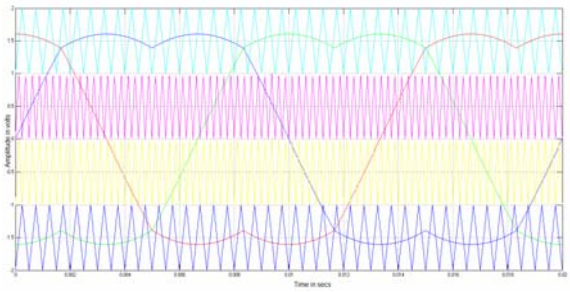

Figure-9. Multicarrier arrangement for VFPWM technique.

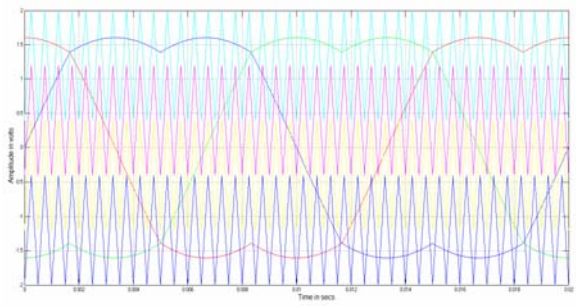

Figure-10. Multicarrier arrangement for COPWM technique.

60 degree reference PWM technique

This PWM strategy is almost similar to sinusoidal PWM except that the modulating sine wave is flat topped for a period of 60 degrees in each half cycle and is as shown in Figures 11-14.

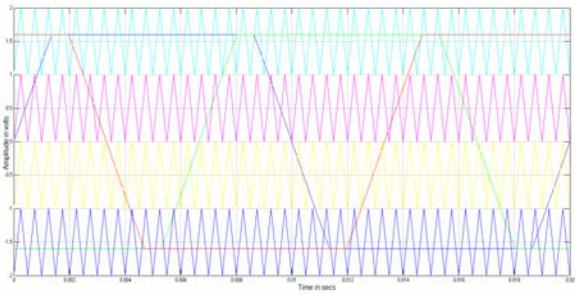

Figure-11. Multicarrier arrangement for SHPWM technique.

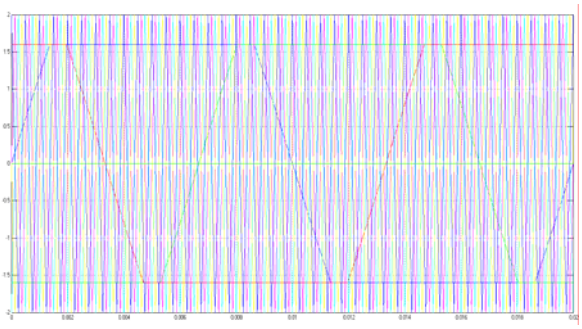

Figure-12. Multicarrier arrangement for PSPWM technique.

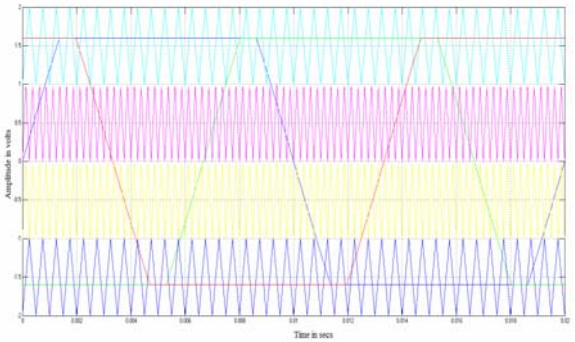

Figure-13. Multicarrier arrangement for VFPWM technique.

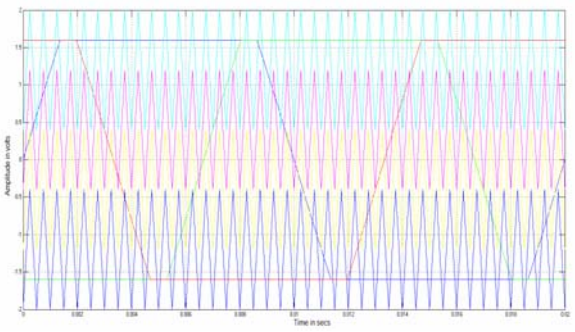

Figure-14. Multicarrier arrangement for COPWM technique.

SIMULATION RESULTS

The cascaded five level inverter is modelled in SIMULINK using power system block set. Switching signals for CMLI are developed using bipolar PWM techniques discussed previously. Simulation is performed for different values of m_a ranging from 0.6-1. The corresponding % THD values are measured using FFT block and they are shown in Tables 1, 3 and 5. Tables 2, 4 and 6 display the V_{rms} of fundamental of inverter output for same modulation indices. Figures 15-38 show the simulated output voltage of CMLI and corresponding FFT plots with above strategies but for only one sample value of m_a = 0.8. Figure-15 shows the five level output voltage generated by SHPWM strategy and its FFT plot is shown in Figure-16. From Figure-16 it is observed that the SHPWM strategy produces significant 30th, 32nd, 36th and 38th harmonic energy. Figure-17 shows the five level output voltage generated by PSPWM strategy and its FFT plot is shown in Figure-18. From Figure-18 It is seen that PSPWM strategy is not having any significant amount of harmonic energy. Figure-19 shows the five level output voltage generated by VFPWM strategy and its FFT plot is shown in Figure-20. From Figure-20 it is seen that the VFPWM strategy produces significant 34th and 38th harmonic energy. Figure-21 shows the five level output voltage generated by COPWM strategy and its FFT plot is shown in Figure-22. From Figure-22 it is noticed that the COPWM strategy produces significant 3rd and 38th harmonic energy.

Figure-23 shows the five level output voltage generated by SHPWM (THI) strategy and its FFT plot is shown in Figure-24. From Figure-24 it is seen that the SHPWM (THI) strategy produces significant 3rd and 38th harmonic energy. Figure-25 shows the five level output voltage generated by PSPWM (THI) strategy and its FFT plot is shown in Figure-26. From Figure-26 it is noticed that the PSPWM (THI) strategy produces significant 3rd harmonic energy only. Figure-27 shows the five level output voltage generated by VFPWM (THI) strategy and its FFT plot is shown in Figure-28. From Figure-28 it is observed that the VFPWM (THI) strategy produces significant 3rd, 36th and 38th harmonic energy. Figure-29 shows the five level output voltage generated by COPWM (THI) strategy and its FFT plot is shown in Figure-30. From Figure-30 it is observed that the COPWM (THI) strategy produces significant 3rd, 5th and 38th harmonic energy.

Figure-31 shows the five level output voltage generated by SHPWM (60 degree) strategy and its FFT plot is shown in Figure-32. From Figure-32 it is observed that the SHPWM (60 degree) strategy produces significant 3rd, 5th, 28thand 38th harmonic energy. Figure-33 shows the five level output voltage generated by PSPWM (60 degree) strategy and its FFT plot is shown in Figure-34. From Figure-34 it is seen that the PSPWM (60 degree) strategy produces significant 3rd harmonic energy. Figure-35 shows the five level output voltage generated by VFPWM (60 degree) strategy and its FFT plot is shown in Figure-36. From Figure-36 it is observed that the VFPWM (60 degree) strategy produces significant 3rd, 36th and 38th harmonic energy. Figure-37 shows the five level output voltage generated by COPWM (60 degree) strategy and its FFT plot is shown in Figure-38. From Figure-38 it is noticed that the COPWM (60 degree) strategy produces significant 3rd and 38th harmonic energy. The following parameter values are used for simulation: V_{DC} = 220V and R (load) = 100 ohms.

Simulation results for sinusoidal reference PWM

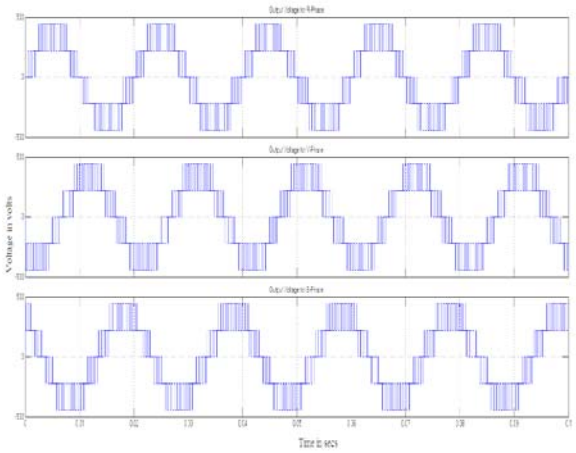

Figure-15. Output voltage generated by SHPWM technique.

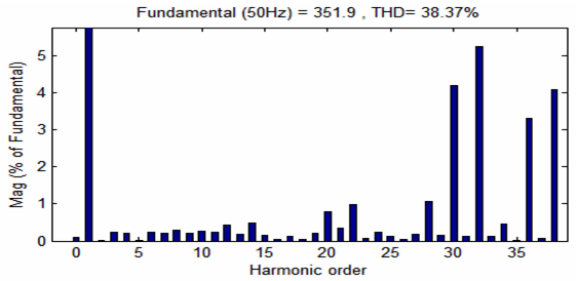

Figure-16. FFT plot for output voltage of SHPWM technique.

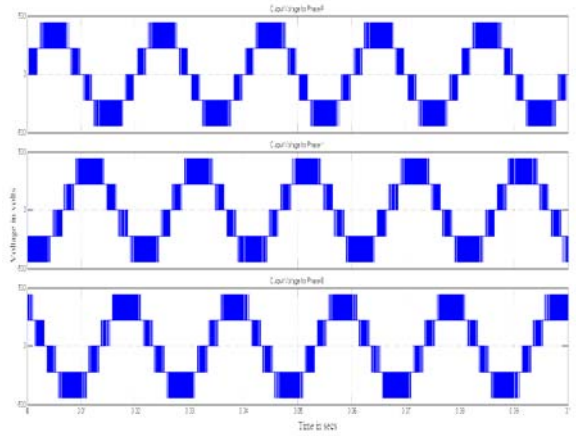

Figure-17. Output voltage generated by PSPWM technique.

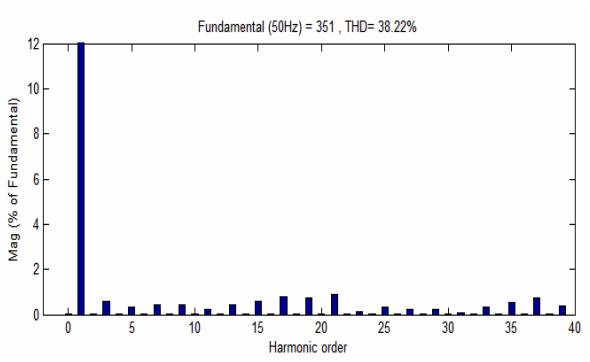

Figure-18. FFT plot for output voltage of PSPWM technique.

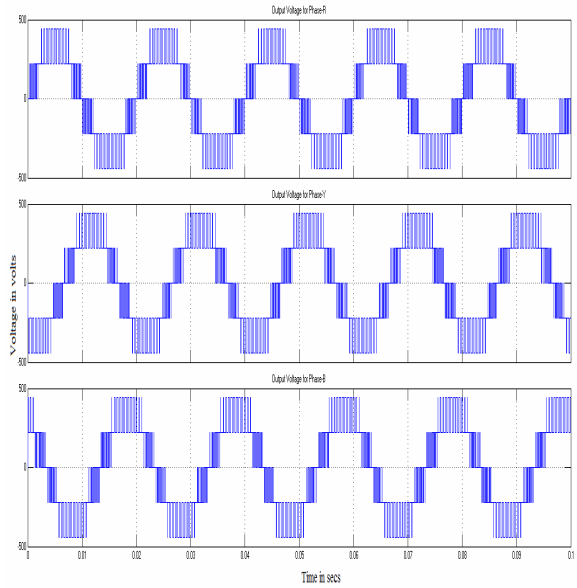

Figure-19. Output voltage generated by VFPWM technique.

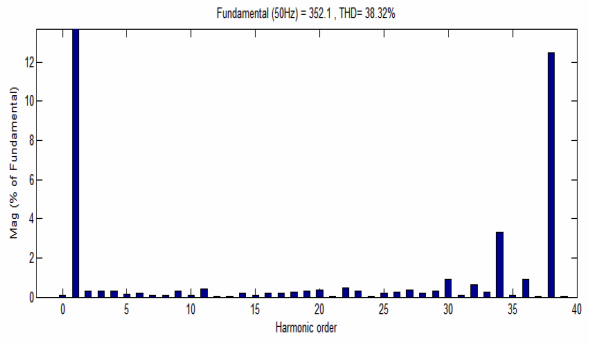

Figure-20. FFT plot for output voltage of VFPWM technique.

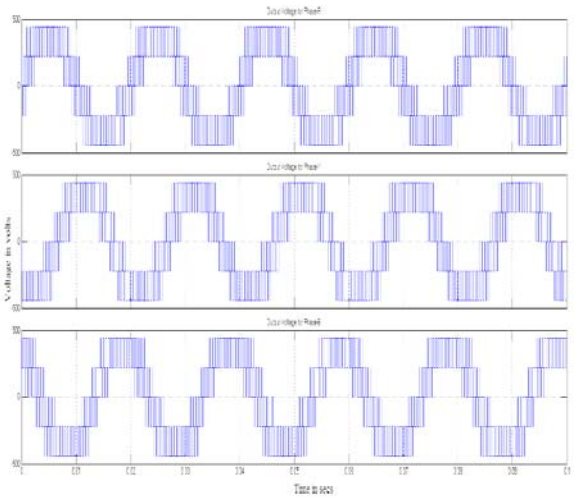

Figure-21. Output voltage generated by COPWM technique.

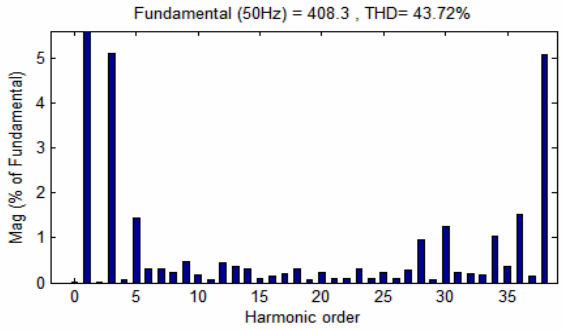

Figure-22. FFT plot for output voltage of COPWM technique.

Simulation results for third harmonic injection reference PWM technique

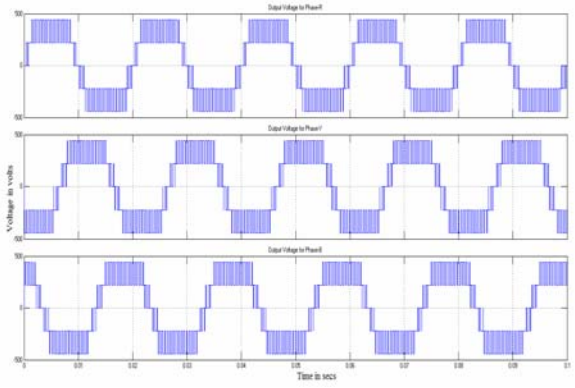

Figure-23. Output voltage generated by SHPWM technique.

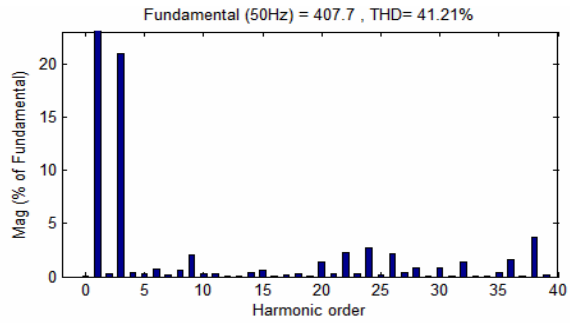

Figure-24. FFT plot for output voltage of SHPWM technique.

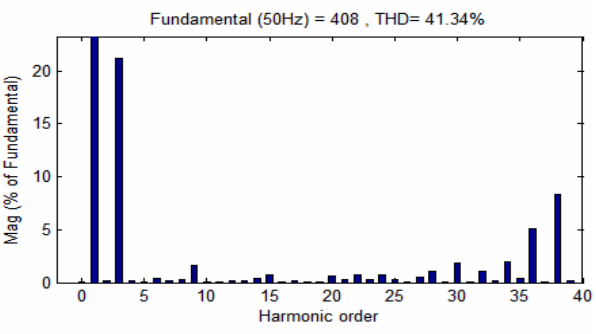

Figure-28. FFT plot for output voltage of VFPWM technique.

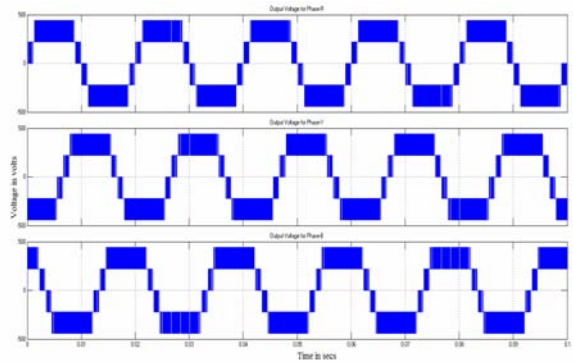

Figure-25. Output voltage generated by PSPWM technique.

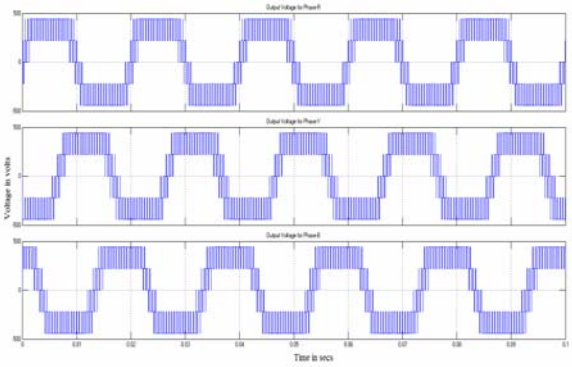

Figure-29. Output voltage generated by COPWM technique.

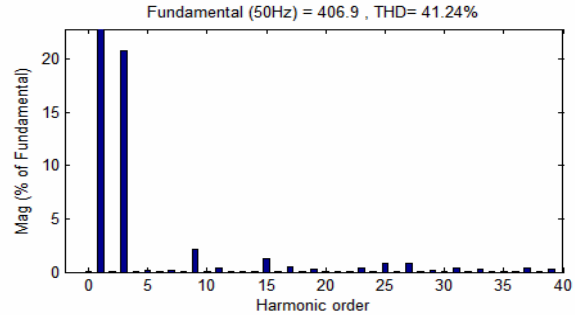

Figure-26. FFT plot for output voltage of PSPWM technique.

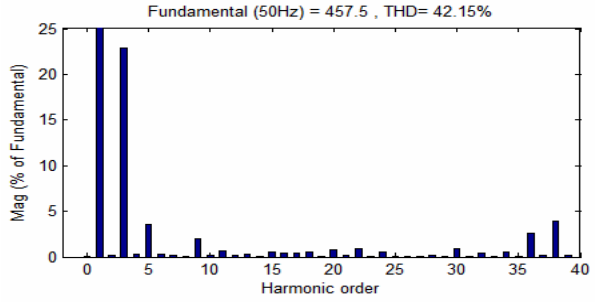

Figure-30. FFT plot for output voltage of COPWM technique.

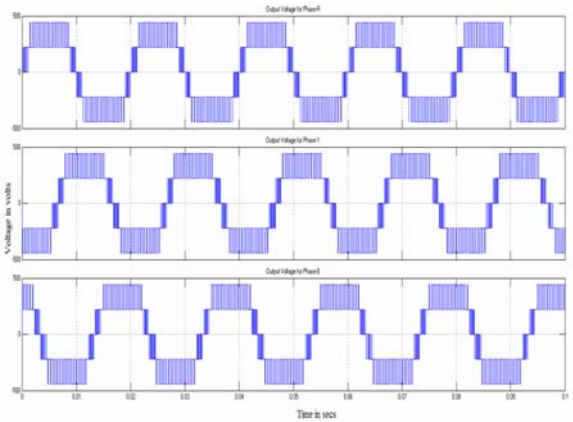

Figure-27. Output voltage generated by VFPWM technique.

Simulation results for 60 degree reference PWM technique

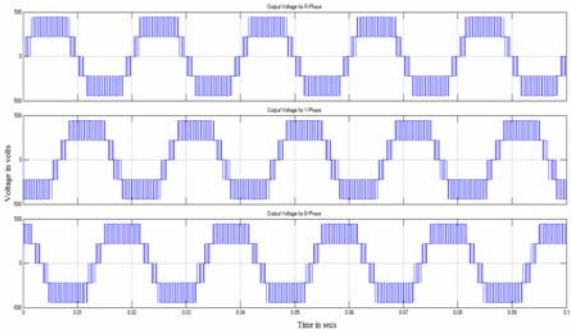

Figure-31. Output voltage generated by SHPWM technique.

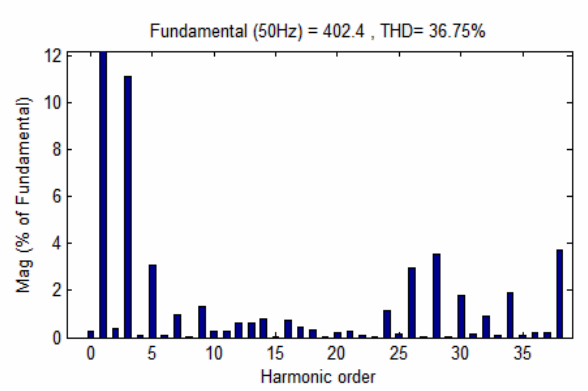

Figure-32. FFT plot for output voltage of SHPWM technique.

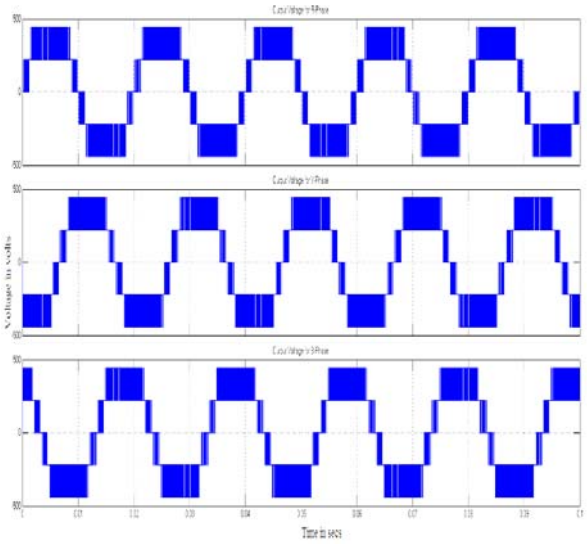

Figure-33. Output voltage generated by PSPWM technique.

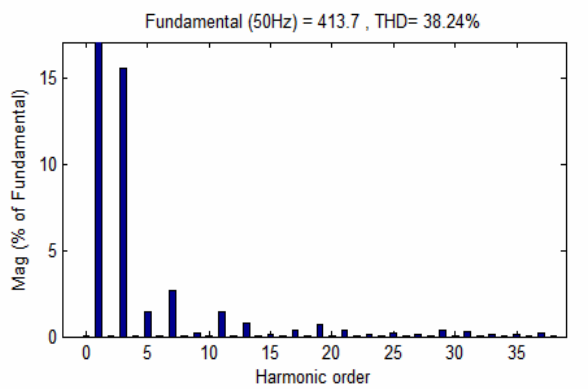

Figure-34. FFT plot for output voltage of PSPWM technique.

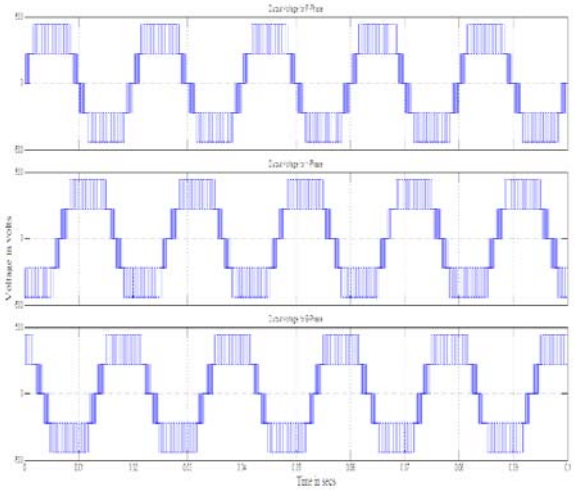

Figure-35. Output voltage generated by VFPWM technique.

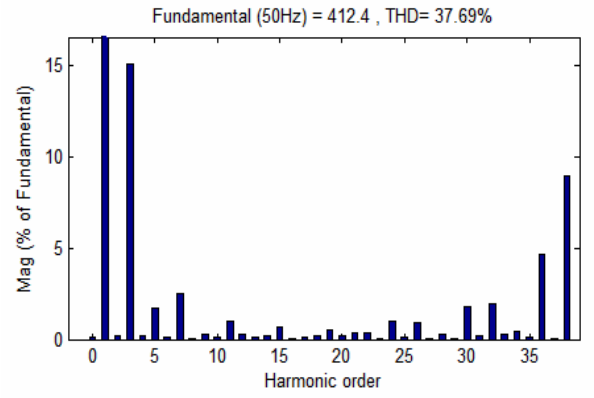

Figure-36. FFT plot for output voltage of VFPWM technique.

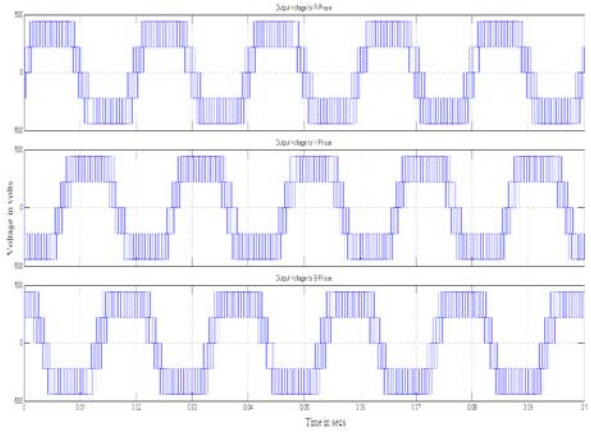

Figure-37. Output voltage generated by COPWM technique.

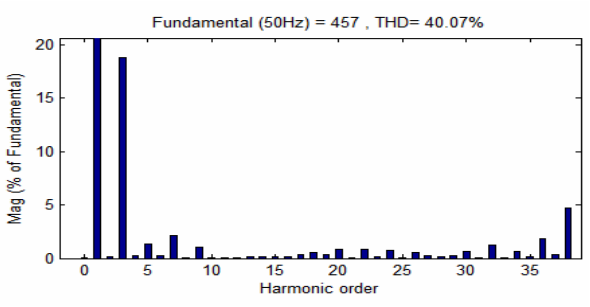

Figure-38. FFT plot for output voltage of COPWM technique.

Table-1. % THD for different modulation indices with sinusoidal reference.

m_a	SHPWM	PS	CO	VF
1	27.04	26.61	33.57	27.09
0.9	33.62	33.22	38.51	33.47
0.8	38.37	38.22	43.72	38.32
0.7	42.07	41.39	50.27	42.49
0.6	44.47	42.95	43.72	44.53

Table-2. V_{RMS} (fundamental) for different modulation indices with sinusoidal reference.

m_a	SHPWM	PS	CO	VF
1	310.7	311.4	333.1	310.8
0.9	280	280.6	311.8	279.9
0.8	248.8	248.6	288.7	248.9
0.7	217.3	218.4	261.9	216.8
0.6	186.1	187.5	288.7	186.5

Table-3. % THD for different modulation indices with THI PWM reference.

m_a	SHPWM	PS	CO	VF
1	28.90	29	33.37	28.94
0.9	35.91	35.80	38.25	35.97
0.8	41.21	41.24	42.15	41.34
0.7	44.05	44.25	45.62	44.04
0.6	42.89	42.91	52.86	42.90

Table-4. V_{RMS} (fundamental) for different modulation indices with THI PWM reference.

m_a	SHPWM	PS	CO	VF
1	359.9	359.1	370.3	359.7
0.9	324.4	325.1	346.5	324.3
0.8	288.3	287.7	323.5	288.5
0.7	252.5	253.3	300	252.9
0.6	216.3	216.1	269.4	216.5

Table-5. % THD for different modulation indices with. 60 degree PWM reference.

m_a	SHPWM	PS	CO	VF
1	21.67	22.69	29.75	22.79
0.9	30.70	31.62	35.73	31.39
0.8	36.75	38.24	40.07	37.69
0.7	41.10	41.83	44.39	41.81
0.6	42.17	41.78	48.58	42.43

Table-6. V_{RMS} (fundamental) for different modulation indices with 60 degree PWM reference.

m_a	SHPWM	PS	CO	VF
1	356.1	364.2	372.5	364.3
0.9	320.3	328.5	346.4	327.7
0.8	284.5	292.5	323.1	291.6
0.7	249	255.2	298.6	255.2
0.6	213.6	218.4	273.5	218.7

Table-7. Crest factor for different modulation indices with sinusoidal reference.

m_a	SHPWM	PS	CO	VF
1	1.414	1.4141	1.4143	1.4142
0.9	1.4143	1.4141	1.4145	1.4145
0.8	1.4143	1.4141	1.4142	1.4139
0.7	1.4141	1.4145	1.4142	1.4140
0.6	1.4137	1.4136	1.4140	1.4140

Table-8. Crest factor for different modulation indices with THI PWM reference.

m_a	SHPWM	PS	CO	VF
1	1.4142	1.4143	1.4141	1.4141
0.9	1.4143	1.4140	1.4141	1.4139
0.8	1.4139	1.4145	1.4140	1.4143
0.7	1.4142	1.4142	1.413	1.4141
0.6	1.4142	1.4143	1.4142	1.4137

Table-9. Crest factor for different modulation indices with 60 degree PWM reference.

m_a	SHPWM	PS	CO	VF
1	1.4140	1.4142	1.4141	1.4143
0.9	1.4141	1.4140	1.4142	1.4142
0.8	1.4144	1.4140	1.4140	1.4140
0.7	1.4141	1.4141	1.4141	1.4142
0.6	1.4139	1.4143	1.4141	1.4142

Table-10. Form factor for different modulation indices with sinusoidal reference.

m_a	SHPWM	PS	CO	VF
1	6214	INF	16655	3108
0.9	3500	INF	3118	3498
0.8	2764	4143	INF	2765
0.7	869	INF	INF	1970
0.6	886	INF	INF	4662

Table-11. Form factor for different modulation indices with THI PWM reference.

m_a	SHPWM	PS	CO	VF
1	1499	INF	9257	3270
0.9	1247	INF	INF	4632
0.8	9610	INF	6470	3606
0.7	1683	INF	1875	8430
0.6	865	INF	2993	866

Table-12. Form factor for different modulation indices with 60 degree PWM reference.

m_a	SHPWM	PS	CO	VF
1	8902	INF	6208	4047
0.9	6406	INF	1924	INF
0.8	1138	INF	INF	3645
0.7	8300	INF	INF	1215
0.6	3051	INF	2486	3124

Table-13. Distortion factor for different modulation indices with sinusoidal reference.

m_a	SHPWM	PS	CO	VF
1	0.035	0.020	0.085	0.073
0.9	0.048	0.043	0.742	0.036
0.8	0.038	0.066	0.571	0.085
0.7	0.094	0.021	0.248	0.063
0.6	0.043	0.049	0.053	0.086

Table-14. Distortion factor for different modulation indices with THI PWM reference.

m_a	SHPWM	PS	CO	VF
1	2.321	2.286	2.634	2.301
0.9	2.316	2.296	2.603	2.305
0.8	2.328	2.304	2.545	2.349
0.7	2.280	2.305	2.431	2.313
0.6	2.292	2.305	2.294	2.311

Table-15. Distortion factor for different modulation indices with 60 degree PWM reference.

m_a	SHPWM	PS	CO	VF
1	0.739	1.666	2.175	1.662
0.9	0.716	1.695	2.162	1.651
0.8	0.746	1.731	2.083	1.671
0.7	0.747	1.671	1.909	1.680
0.6	0.756	1.647	1.680	1.674

CONCLUSIONS

It is observed from Tables 1, 3 and 5 that PSPWM strategy provides output with relative low distortion for the four PWM strategies developed with sine ref where as SHPWM creates least harmonic distortion with other two references. COPWM is found to perform better since it provides relatively higher fundamental RMS output voltage (Tables 2, 4 and 6). Tables 7, 8 and 9 provide crest factor, Tables 10, 11 and 12 provide form factor and Tables 13, 14 and 15 provide distortion factor for all modulating indices.

REFERENCES

[1] Donald Grahame Holmes and Brendam P. Mcgrath. 2001. Opportunities for harmonic Cancellation with carrier based PWM for two-level and multilevel cascaded inverters. In: IEEE Trans. Industry Applications. 37(2): 574-582.

[2] P.C. Loh, D.G. Holme and T.A. Lipo. 2003. Synchronisation of distributed PWM cascaded multilevel inverter with minimal harmonic distortion and common mode voltage. In: IEEE Conf. Rec. 0-7803-7754-0/03. pp. 177-182.

[3] S. Mariethoz and A. Rufer. 2004. Resolution and efficiency improvements for three phase cascaded multilevel inverters. In: IEEE Conf. Rec: 0-7803-8399-0/04. pp. 4441-4446.

[4] Xianglian Xu, Yunping Zou, Kai Ding and Feiliu. 2004. Cascaded multilevel inverter with phase-shift SPWM and its application in STATCOM. In: IEEE Conf. Rec. 0-7803-8730-9/04. pp. 1139-1143.

[5] N. A. Azhi and Y.C. Choong. 2006. Analysis on the performance of a three phase cascaded H-Bridge multilevel Inverter. In: IEEE Conf. Rec. 1-4244-0273-5/06. pp. 405-410.

[6] B. Shanthi and S.P. Natarajan. 2008. Carrier overlapping PWM methods for single phase cascaded five level inverter. International Journal of Science and Technology of Automatic Control and Computer engineering (IJ-STA, Tunisia), Special issue on Control of Electrical Machines. pp. 590-601.

[7] Roozbeh Naderi and Abdolreza Rahmati. 2008. Phase-shifted carrier PWM technique for general cascaded inverters. In: IEEE Trans. Power Electronics. 23(3): 1257-1269.

[8] Gierri Waltrich and Ivo Barbi. 2010. Three-phase cascaded multilevel inverter using power cell switch with two inverter legs in series. In: IEEE Trans. Industrial Electronics. 57(8): 2605-2612.

[9] B. Urmila and D. Subbarayudu. 2010. Multilevel Inverters: A comparative study of pulse width modulation techniques. Journal of Scientific and Engineering Research. 1(3): 1-5.

[10] Gierri waltrich and Ivo Barbi. 2010. Three-phase cascaded multilevel inverter using commutation sub-cells. In: IEEE Conf. Rec. 978-1-4244-3370-4/09. pp. 362-368.

[11] Georgious S. Konstantinou, Sridhar R. Pulikanti and Vassilios G. Agalidis. 2010. Harmonic elimination control of a five level DC-AC cascaded H-bridge hybrid inverter. In: 2nd IEEE International Symposium on Power Electronics for Distributed Generation Systems. Rec. 978-1-4244-5670-3. pp. 352-357.

[12] Farid khoucha, Mouna Soumia Lagoun, Adelaziz Kheloui and Mohamed EI Hachemi Benbouzid. 2011. A comparison of symmetrical and asymmetrical Three-phase H-Bridge multilevel inverter for DTC Induction motor drives. IEEE Trans. Energy Conversion. 26(1): 64-72.