VOL. 7, NO. 11, NOVEMBER 2012 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences


www.arpnjournals.com

STABILITY ANALYSIS OF PARALLELED SINGLE ENDED PRIMARY INDUCTANCE CONVERTERS

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ABSTRACT

The small signal model offers an encouraging scope to examine the steady state stability and there from establish a viable operating range for power converters. The theory of Eigen value analysis facilitates to predict the stable operation and introduce appropriate measures to regain its equilibrium in the event of an exigency. The paper attempts to develop a methodology through the use of compensators to ensure that the Eigen values of the characteristic equation of the converter lie in the left half of the S plane. It includes the philosophy of a master slave current sharing mechanism in the scheme to arrive at satisfactory servo and regulatory results. The performance of the parallel connected SEPIC (Single Ended Primary Inductance Converters) system is evaluated using time and frequency domain plots on a MATLAB platform to project the suitability of the proposed approach in practical applications.

Keywords: compensator, stability, current sharing, master slave control.

INTRODUCTION

There is an increasing demand of higher current rated reliable power supplies owing allegiance to extensive automation in domestic utilities. The high current requirement is best met by connecting converters in parallel in light of the view that parallel operation of dc-dc converters is widely used in many applications.

It inherits a host of advantages over a single converter and caters to the incessant growing demand. The problem of limited component tolerances and asymmetric layout of the converters required to be addressed effectively using suitable techniques. Though a wide variety of approaches with different complexity and current sharing performances are in existence still a good bit of innovation may evince a better use of such converters.

A system remains in a particular state unless affected by an external action and if it returns to the same state when the external action is removed can be considered to be stable. The stability of the system is extremely relevant in the present day environment where frequent changes in load and supply are imminent. It relates to its post disturbance responses and augurs the need for predictive measures to guarantee the desired performance. It is measured more realistically in the time-domain where it is usually more difficult to determine analytically especially for a higher order system.

The small signal model of a buck/boost converter has been developed in the current controlled mode and used to investigate its stability [1]. The average state space model of the dc-dc buck converter has been derived in order to predict its frequency response characteristics [2]. A systematic procedure for analyzing the stability of dc-dc converters using Lyapunov function has been proposed [3]. The successive module has been found to trace the current of its previous module in the form of circular chain [4].

The simplest current sharing open loop (droop) method has been found to rely on the output resistance of paralleled modules to maintain relatively even current distribution among the modules [5]. It has been shown to yield poor output voltage regulation as a result of droop output characteristics and requires individual converter voltages to be trimmed to closely match each other. Each module has been found to track the average current to accomplish an equal current distribution among the multiple connected units [6]. A common reference in an internal loop of each module has been found to eclipse average current mode control [7].

A damping network has been suggested to arrive at the desired phase margin in a particular operating state in a buck converter [8]. A stability criterion for testing the robustness of a power converter system with uncertainties in the frequency domain has been proposed and found to offer satisfactory results [9]. A strategy for assessing the steady state stability of a buck/boost SEPIC has been formulated and ensures the desired performance through the entire operating range [10].

The paralleled converters with non-identical component characteristics and input voltage variation may lead to instability and subsequent performance degradation. Therefore a new methodology that incorporates equal current sharing ensures load voltage regulation and guarantees a stable operating horizon is important in the present context.

PROBLEM FORMULATION

The basic philosophy echoes to insert a suitable feedback compensator in the small signal model of a paralleled SEPIC with a view to facilitate its steady state stability through the loadability range. The algorithm forges the role of a master slave action to elicit the current sharing phenomena and extract the stable operation of the converter. It corners around the construction of a transfer function expressed as a ratio of its output to duty cycle using which the stability is assessed both in time and frequency domains. The strategy includes MATLAB based simulation to investigate its stable operation, ability

to equally distribute the load current and regulate the output voltage.

PROPOSED STRATEGY

The steady state stability of a power converter appears to be significant in view of the fact that it is required to perform satisfactorily over a viable operating range. The circuits parasitic forge their influence in governing the stability and may restrict the operational limit. Besides there is a strong need that the converter enjoys a stable state even in the event of either a source or a load disturbance. The scheme orients to formulate a control strategy, through which the ratio of the output to duty cycle can be altered to regulate the output voltage, equally distribute the load current among the converters and operate the converter in a stable operating state. The approach follows a modelling procedure where from the requisite transfer function is derived.

The power module of two SEPICs connected in parallel shown in Figure-1 offers either to step up or step down the input voltage of the same polarity and serve the needs of higher power rated applications.

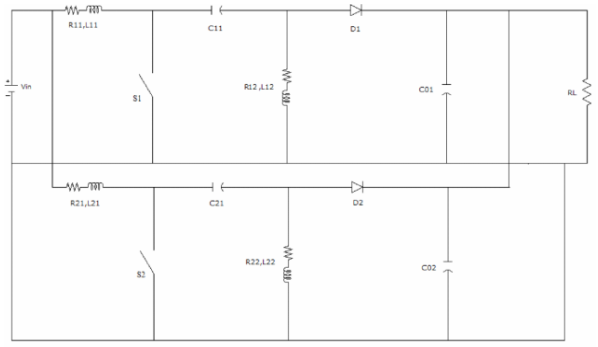

Figure-1. Paralleled SEPICs power stage.

MODELING

A model is basically meant to express the circuit description of the system in a mathematical form. The purpose of a model is to enable the analyst to predict the effect of changes to the system. A good model is a judicious trade-off between realism and simplicity. Small signal models are commonly used where it is preferred to linearized the system about a quiescent operating point. It can be applied to involve relatively simple techniques of linear circuit theory such as Bode plot, root locus and there from design the controller and or evaluate its stable performance.

A host of approaches are in vogue to analyze parallel connected modules among which the Master Slave Current Sharing (MSC) methodology seems to be attractive owing to its hierarchical nature and flexibility of design. It evolves a procedure through which the paralleled converters share the current almost equally, by adjusting the effective voltage reference signals in the voltage loop. The converter with lowest voltage loop gain articulates itself to be the master while the converters automatically become the slave.

It is seen from Figure-2 that a voltage proportional to the output current of the master converter, unaffected by the current sharing circuitry is chosen to the reference of the master converter and the effective voltage reference signals of the slave converters are adjusted so as to increase their output currents to a magnitude almost equaling the masters output current. The parallel connected converters interact in their continuous bid to regulate the output voltage.

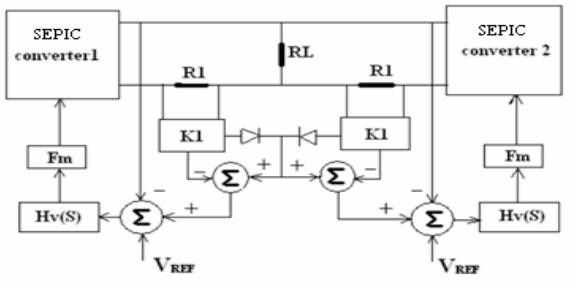

Figure-2. Paralleled SEPIC converters with individual voltage loops and Master Slave Current sharing circuitry.

The transfer function model of a single SEPIC can be written as shown in equation (1)

("V"_"0 " ("S"))/"d" ("S") " = " "1" /"D" ^"□2" ("1-" [["S

Where

$$\omega_{o1} = \frac{1}{\sqrt{L_1\left(C_2\frac{D^2}{D^{\square 2}}+C_1\right)+L_2\,(C_1+C_2)}} \quad (2)$$

$$Q_1 = \frac{R}{\omega_{o1}\left(L_1\frac{D^2}{D^{\square 2}}+L_2\right)} \quad (3)$$

$$\omega_{o2} = \sqrt{\frac{1}{L_2\frac{C_1}{D^2}\square\frac{C_1}{D^{\square 2}}}+\frac{1}{L_1C_1\square C_2}} \quad (4)$$

$$Q_2 = \frac{R}{\omega_{o2}(L_1+L_2)\frac{C_1\omega_{o1}^2}{C_2\omega_{o2}^2}} \quad (5)$$

The dynamic behaviour of the current sharing phenomena can be expressed in equation (6)

$$T_{cs} = A_a(S).A_b(S).H_v(S).F_m.F_1 \quad (6)$$

Where

$$A_a(S) = I.R_s . G_c \quad (7)$$

I is the output current of one converter

R_s is the current sense resistor gain

G_c is the gain of the current amplifier

$A_b(S)$ is the current share compensator

$H_V(S)$ is the voltage feedback compensation. It stabilizes the unstable ω_p in an effort to offer the desired closed loop performance through a pole zero compensation technique.

$$F_1 = \frac{i_{l1}}{d_1} \quad (8)$$

i_{l1} is the input inductor current of SEPIC 1

d_1 is the corresponding duty cycle

The transfer function of the chosen lead lag compensator is expressed in equation (9)

$$= \frac{S+\frac{1}{R_2C_2}}{R_1(C_2+C_3)S(S+\frac{1}{R_2(C_2 \boxtimes C_3)}} \quad (9)$$

$$= K_m \frac{(S+\omega_z)}{(S+\omega_p)} \quad (10)$$

$$K_m = \frac{1}{R_1(C_2+C_3)} \quad (11)$$

$$\omega_z = \frac{1}{C_2} \quad (12)$$

$$\omega_p = \frac{1}{R_2(C_2 \boxtimes C_3)} \quad (13)$$

The change in master reference signal is mathematically seen in equation (14) is determined by the properties of the cross coupling loop gain

$$T_{cC} = A_a(S).A_b(S).H_V(S).F_m.F_2 \quad (14)$$

$$F_2 = \frac{i_{l1}}{d_2} \quad (15)$$

The term I_{lx} / d_y initiates a change in the duty ratio of one converter to influence the inductor current of another converter. The voltage loop gain of the slave converter is appropriately measured and its dynamic response is given by the equation (16)

$$T_{sL} = \frac{T_V}{(1+T_{cs}-T_{cC})} \quad (16)$$

T_V is the voltage loop gain of the individual module

T_{cs} is the current share loop gain

T_{cc} is the cross coupling gain

The voltage loop gain of the master module along with the voltage loop gain of individual module prior to paralleling is expressed in equation (17)

$$T_{ML} = T_V + 2*F_2*(T_{cs}-T_{cC}) \quad (17)$$

Where F_2 is the output to duty ratio transfer function. Therefore the overall system loop gain (master and slave in parallel) is represented by equation (18)

$$T_{overall} = T_{ML} + T_{sL} \quad (18)$$

SIMULATION RESULTS

The small signal model of the parallel buck/boost SEPIC along with lead lag compensator is simulated on a MATLAB - SIMULINK platform. The specifications of the converter system include the following parameters R_1 = 0.1Ω, L_1 = 100 µH, R_2 = 0.2, L_2 = 100 µH, R_1 = 3m Ω C_1 = 680 µF, R_0 = 1mΩ, C_0 = 2200 µF. The objective is to acquire a stable output of 230 V from an input of 350 V for buck converter and 350 V for boost converter from an available input of 230 V. The performance of the model is investigated through a preferred load horizon in the range up to 5 KW when the power switches are fired at 50 KHz.

The steady state output voltage, individual converter currents and the load current corresponding to a load of 3 KW for both buck and boost converters are displayed in Figures 3 and 4. The model is subjected to instantaneous increases of load and supply at t = 0.5 sec and 1 sec, respectively in order to establish the ability of the compensator to function as a controller. Though the load current experiences a sudden increase and the load voltage fall on account of the increased load, the new steady state values of the current and the regulated voltage however are reached almost immediately. The same corrective action is noticed even in the increase of an input voltage where both the output current and voltage settle at the earlier values.

STABILITY ANALYSIS

An important alternative approach to the analysis and design is the frequency response method using which the stability of a system can be determined. The root-locus plots are used to depict the roots of the system over the range of a variable in order to determine if the system becomes unstable. The roots of the characteristic equation play a pivotal role in the assessment and calls for the procedure to estimate the gain in ensuring its position in the left half of the S plane. The transfer function expressed as a ratio of the output to duty cycle gains strength in predicting the maximum loadable level of the converter.

The plot obtained in Figures 5 and 7 exhibit the unstable nature of the buck and boost SEPICS respectively for an operating point of 3 Kw on account of the decline in voltage at that instant of time. However the action of the chosen compensator pushes the pole to the left half in both cases as noticed from Figures 6 and 8.

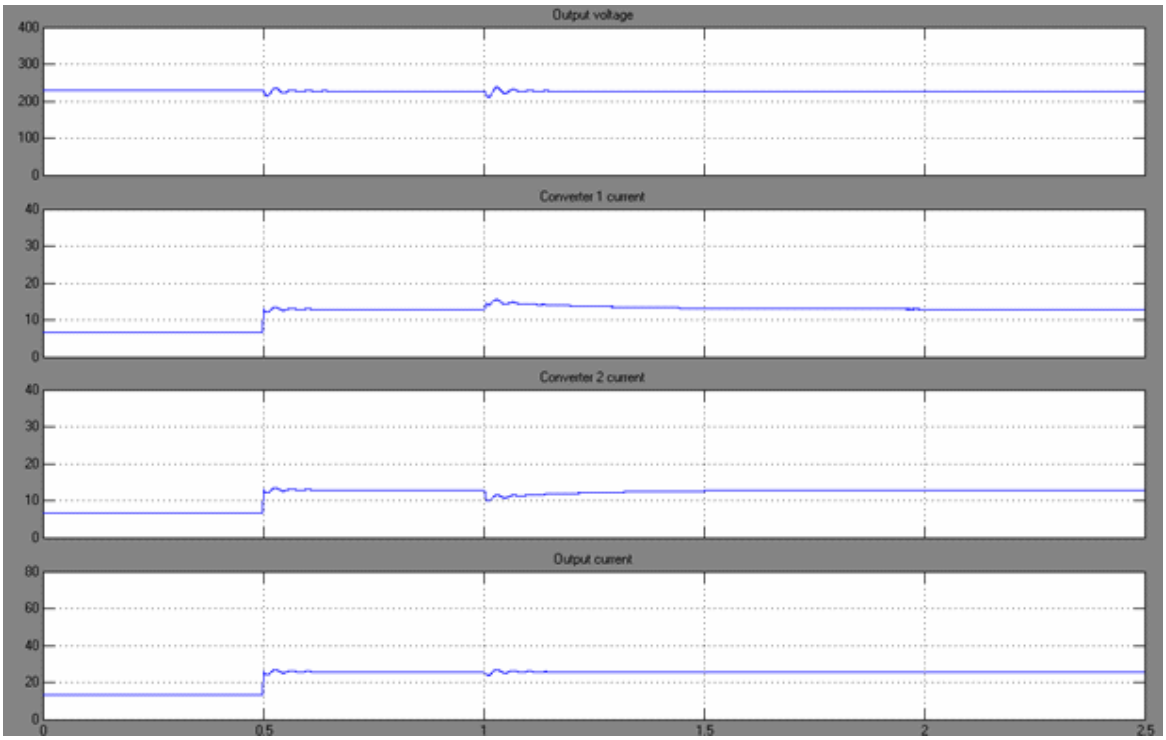

Figure-3. Steady state and transient response of buck mode.

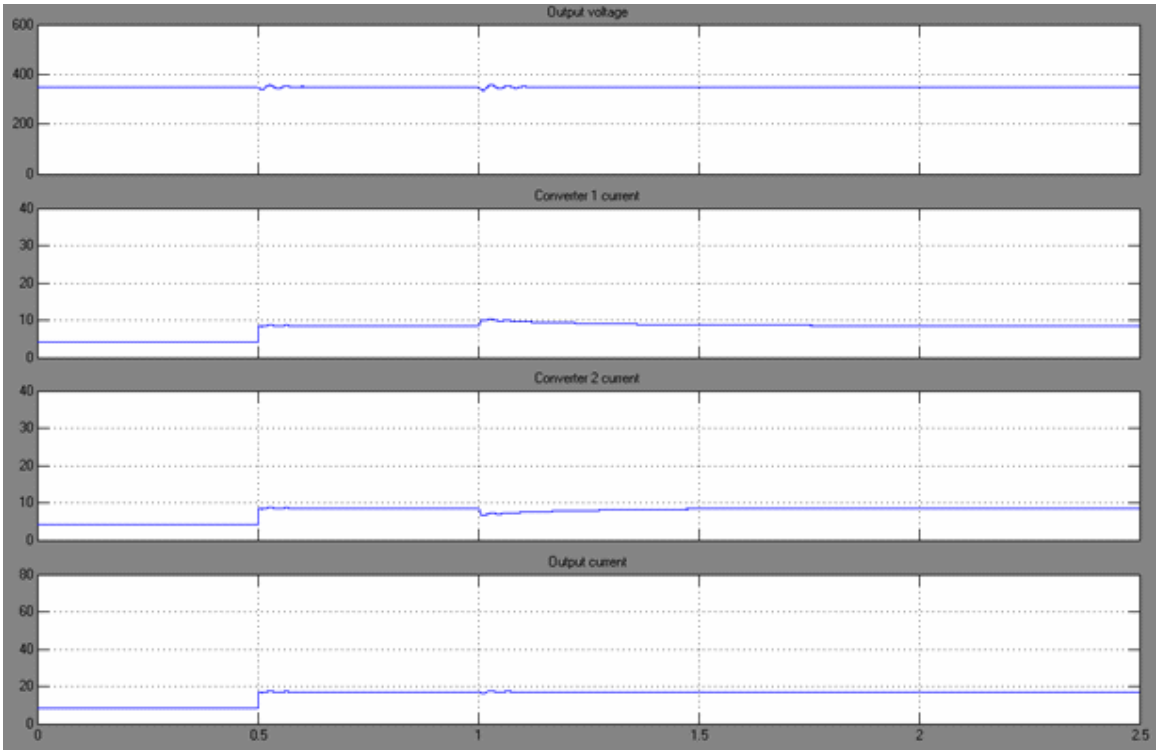

Figure-4. Steady state and transient response of boost mode.

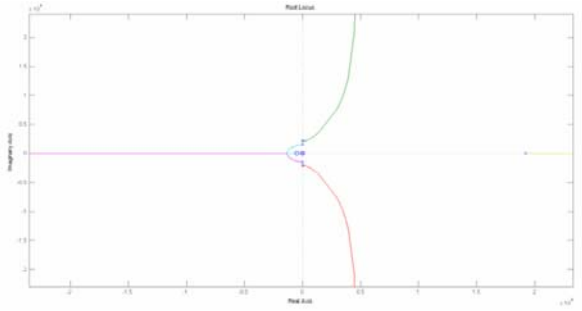

Figure-5. Root locus of buck mode (unstable).

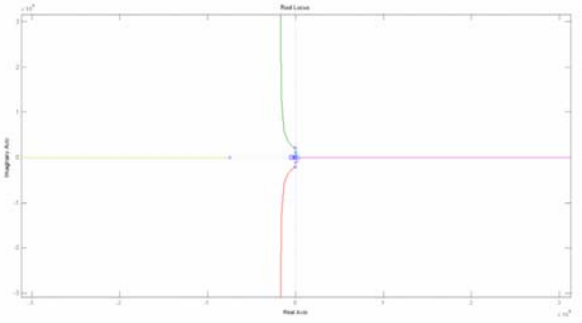

Figure-6. Root locus of buck mode (stable).

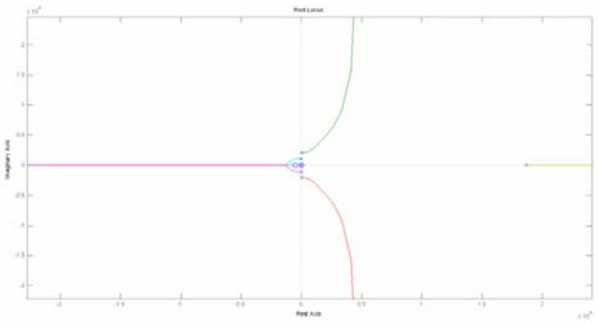

Figure-7. Root locus of boost mode (unstable).

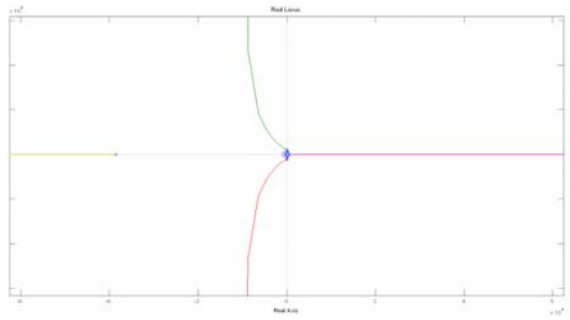

Figure-8. Root locus of boost mode (stable).

The Bode plot is an important tool for stability analysis of closed-loop systems. It is a pictorial representation of the frequency response characteristics of the system and involves a graph of the system transfer function on a log-frequency axis. The stability is assessed by calculating the amplitude and phase angle for the transfer function and expressed as a measure of the gain and phase margins. The Figures 9 through 12 describe the Bode plots of the SEPIC buck and boost at the same operating point and follows from Figures 10 and 12 that the converter is able to deliver the required power to the load with safe stability limits. The lead- lag compensator serves to extract positive values for the phase and gain margins thus elucidating its stability in the frequency domain.

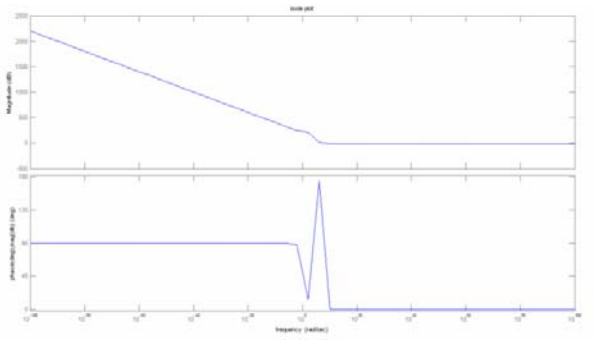

Figure-9. Bode plot response of buck mode (unstable).

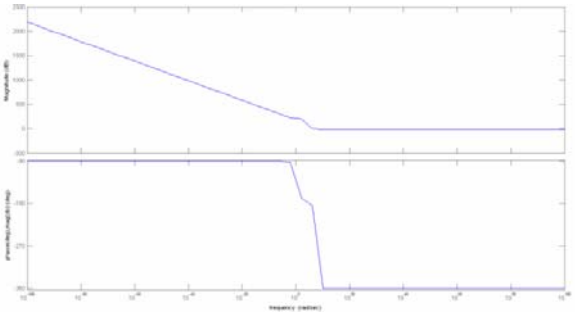

Figure-10. Bode plot response of buck mode (stable).

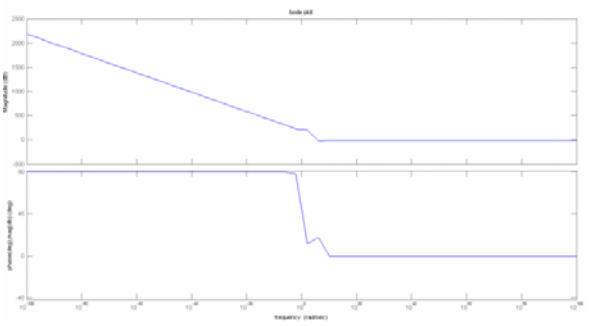

Figure-11. Bode plot response of boost mode (unstable).

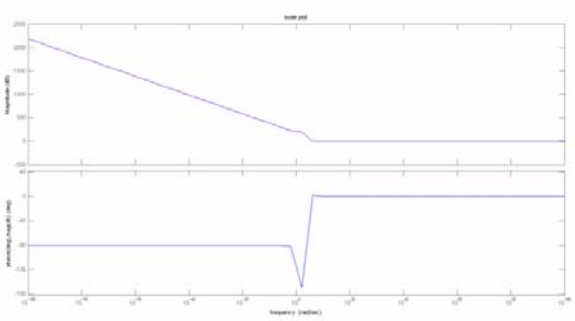

Figure-12. Bode plot response of boost mode (stable).

Table-1. Sepic buck.

Power (KW)	**Load current** (A)		**Converter 1 current** (A)		**Converter 2 current** (A)		**Output voltage** (V)	
	Open loop	**Closed loop**	**Open loop**	**Closed loop**	**Open loop**	**Closed loop**	**Open loop**	**Closed loop**
1	2.87	4.37	1.42	2.185	1.45	2.185	350.39	231.20
2	5.96	8.71	2.99	4.355	2.97	4.355	337.16	230.35
3	9.28	13.02	4.56	6.512	4.72	6.512	323.72	229.65
4	14.35	17.30	7.20	8.652	7.15	8.652	280.70	228.85
5	19.78	21.55	9.87	10.778	9.91	10.778	252.80	228.05

Table-2. Sepic boost.

Power (KW)	**Load current** (A)		**Converter current 1** (A)		**Converter current 2** (A)		**Output voltage** (V)	
	Open loop	**Closed loop**	**Open loop**	**Closed loop**	**Open loop**	**Closed loop**	**Open loop**	**Closed loop**
1	2.13	2.869	1.05	1.434	1.08	1.434	471.40	351.48
2	4.43	5.730	2.22	2.865	2.21	2.865	453.20	350.95
3	6.84	8.582	3.35	4.291	3.49	4.291	439.30	350.45
4	9.85	11.426	4.90	5.713	4.95	5.713	406.70	349.90
5	13.45	14.261	6.72	7.130	6.73	7.130	371.80	349.40

The entries in Tables 1 and 2 relating to SEPIC buck and boost respectively constitute the load current, individual converter currents and output voltage, across a range of load powers. The readings highlight the effective role of the proposed compensating feedback technique through an equal sharing of the load current and ensure tight output voltage regulation over the entire range.

CONCLUSIONS

The role of a compensating network has been sought to ensure the stable operation of two SEPICs connected in parallel. The investigative study unleashed through well accepted procedures has been found to illustrate its performance both in time and frequency domains. The root locus plot has been found to predict the stable nature of the system through the location of the eigen values of the characteristic equation. The influence of the lead lag compensator has been realized through acceptable phase and gain margins. The performance has been obtained over the range of operating loads to translate the viability of the parallel connected SEPIC for present day applications and will go a long way in exploring newer avenues in the emerging variable drive scenario.

ACKNOWLEDGEMENT

The authors thank the authorities of Annamalai University for providing the necessary facilities to accomplish this piece of work.

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