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PRODUCT VISUALIZATION, REALIZATION AND RELIABILITY OF NON-HERMETICALLY ENCAPSULATED INTEGRATED CIRCUIT PACKAGES

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ABSTRACT

The aim of this investigation is to generate 3D models of eight different Thin Dual or Quad Leadless Moulded IC packages and conduct the performance analyses using die shear, thermal experiments and finite element analysis. Reliability plays a major role at every stage in the manufacturing, testing and use of integrated circuit packages. The coupled influence of operating voltages and joule heating on the mechanical reliability of ICs is discussed here. Die shear tests were conducted on the ICs and the shear strength compared with the values obtained from the finite element results. Thermal tests were carried out on the ICs that were later inspected under a Scanning Acoustic Microscope (SAM) for delaminations arising from hygrothermal stresses. Finally the results of the electro-hygrothermo-mechanical analyses were analyzed and presented at the maximum operating temperature (MOT) that highlight the overall static reliability of the ICs with acceptable factors of safety. The main objective of this investigation is the construction of the failure envelopes through determination of the maximum operating temperatures and test temperatures of the ICs that aid in the evaluation of the overall static reliability of the ICs.

Keywords: product visualization, product realization, simulations, design for manufacture, design for reliability, shear tests, scanning acoustic microscopy.

INTRODUCTION

The joint project with SPEL Semiconductor Limited [1] to improve the understanding and exploitation of advanced semiconductor materials and electronic packaging of ICs is unique as it caters to the needs of customers all of whom are from the export market. This project assumes great significance as the entire 3D design and analyses for the ICs developed, are carried out with the facilities available at our academia and SPEL.

Electronic packaging is relatively a new subject compared to super plasticity, composite materials or solid state devices. With the advent of miniaturization and the demonstration of Moore's law (every 18 months the chipmakers double the number of transistors that can be packed on to a silicon wafer), there was a need to package the newer working principles and concepts efficiently and reduce size for a superior performance and manage thermal aspects of the ICs as well. Thus the concept of microsystems and nanosystems packaging came in to being [2]. The role of a package is to shut out environmental influences, enable electrical connectivity, dissipate heat and improve handling and assembly. Some of the popular types of electronic packages are the dual packages, shrink small outline packages, pin grid arrays and plastic leaded chip carriers. The micro Dual Leadless Moulded Packages (µDLMP) and the Thin Quad Leadless Moulded Packages (TQLMP) come with superior function at a small size and are increasingly being used in mobile phones, digital cameras, PDAs and automobile control systems [1]. There is enormous customer curiosity on the reliability of the miniaturized products manufactured with these ICs. Hence there is an imperative need to address the reliability issues, demonstrate the evaluation techniques and conformance of these packages to user requirements. Figure-1 shows the architecture of a simplified plastic IC package. Plastic packages are non-hermetic meaning permeable to heat and moisture, but flexible and cost effective at operating temperatures below 200°C.

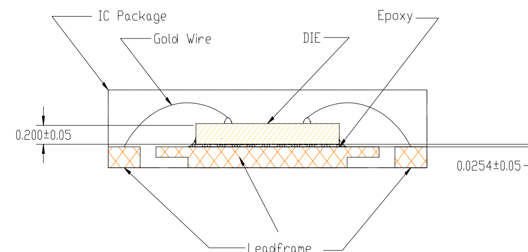

Figure-1. 2D cross section model of an IC package.

Plastic based non-hermetic packages are more popular with the manufacturers of electronic packaging. However, at their maximum operating temperature they may face a hoard of problems that may lead to premature failure. The causes of such failures are mostly by joule heating due to the resistance offered by the material to current flow (I^2 R losses), electrostatic discharge (ESD), hygrothermal fracture, electro-thermo-mechanical fatigue, manufacturing defects like delaminations, soldering defects and material defects.

The present investigation deals with the static reliability of eight IC packages such as the 1.35 x 1.7 mm 8L µDLMP, 1.35 x 2.5 mm 12L µDLMP, 4x4 mm 24L symmetric and asymmetric TQLMP, 5x6 mm 36L TQLMP, 7x7 mm 48L TQLMP, 5x11 mm 56L TQLMP and the 9x9 mm 64L TQLMP. The prefix numbers indicate the number of pins in each IC. Product

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visualization was done using the Pro-Engineer Wildfire software and the products were analyzed for electro-thermo-mechanical static reliability using the ANSYS finite element modelling software [3]. As the IC packages experience joule heating during operation due to the application of voltage difference and current, they cause thermal stresses to be induced in the package. As thermal stresses cause warping, bending, twisting and other type of deflections, the mechanical stresses develop in the package that is fixed to a Printed Circuit Board (PCB) or a Printed Wiring Board (PWB) in the leads and the package as whole [4, 5]. Leadless packages discussed here are more stable than leaded packages, reducing the deflection leverage due to mechanical stresses. However, as it is a new venture involving the manufacture of IC packages through die attach, wire bonding and resin transfer moulding encapsulation, it becomes mandatory to evaluate the packages for reliability and conformance. The results from the simulation studies and calculations based on actual operating conditions are compared with the experimental results from the die shear tests, thermal pre-conditioning tests and delamination observation under the scanning acoustic microscope (SAM). Comparison reveals that the operating stresses are generally lower than the failure stresses with a factor of safety included. The significance of this investigation is in the consideration of electro-hygrothermo-mechanical stresses that are a result of the actual multiple and coupled effects the IC packages go through. The Design for Manufacturing, Assembly and Environment (DFMAE) approach is emphasized here as concurrent design, analysis, manufacturing and testing feedback principles are employed for product realization, keeping cost in mind. The ICs fabricated by SPEL semiconductors are also lead free thereby addressing the issue of environmental impact.

MODELLING AND FINITE ELEMENT ANALYSIS

The 2D and 3 D models of the IC packages were created using the Pro-E wildfire software. For analytical requirements the models were created with and with out the IC plastic encapsulation as the property evaluation had to be done for both the conditions in order to clearly identify the influence of the mould compound. The copper lead frame shown in Figure-2 forms the skeletal frame on which the silicon die is pasted using a conductive silver epoxy paste. Gold wires with a diameter of 25 microns were bonded from the leads on to the silicon die in order to enable the IC to receive and transmit signals. The entire micro assembly is encapsulated with a mould compound consisting of epoxy resin, phenolic resin, carbon black nano powder and fused silica nano powder through the Resin Transfer Moulding (RTM) technique. Here, the 3D models of the ICs with the mould compound encapsulation are shown to be transparent in order to provide visual details keeping the material properties in mind.

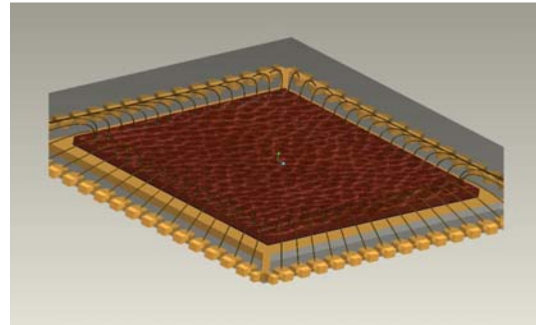

Figure-2. A 3D model of a 64 L TQLMP IC.

The models were imported in to the ANSYS software in the Initial Graphics Exchange Specification (IGES) format. Coupled field electro- thermo-mechanical FE analyses were conducted using the materials properties given in Table-1 for the various materials used in the design. The coupled field analyses were carried out using a solid element with 8 nodes and capable of two degrees of freedom, i.e. temperature and voltage. The element is also capable of three dimensional thermal and electrical conductivity. So it was used for the electrical - thermal coupled field analysis involving joule heating and another solid element was used for the thermal-mechanical coupled field analysis involving the von mises equivalent stresses and shear stresses. The thermal results from the first coupled field analysis were fed in to the next analysis through an `.rth' file and the thermal-structural analysis performed using the solid elements that are used for this coupled field analysis. The results from this analysis were stored as an `.rst' file. Thus it was possible to evaluate the electrical influence on the thermal characteristics and then the thermal influence on the mechanical characteristics of the IC package.

A meshed model of the packages of the ICs without encapsulation is shown here in Figure-3. According to the properties to be derived the models were meshed with and without encapsulation. The models were constrained at the lead lines along the two outer edges of the copper lead frame as it would be during operation. A manufacturer specified potential difference of 3.3 to 6.8 volts was applied at the designated pins for the various ICs investigated here.

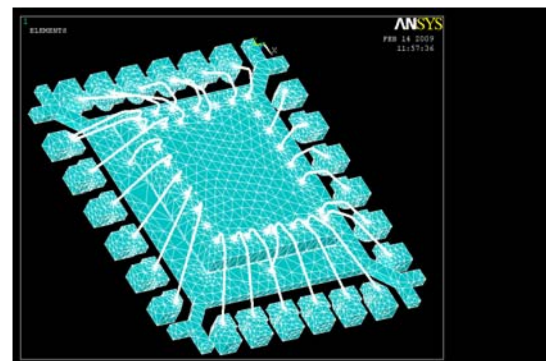

Figure-3. Meshed model of a 24L TQLMP IC.

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The packaging material properties are given in Table-1. In addition to the properties considered for the coupled field analyses, two different mould compounds were used for encapsulation of the ICs. Their required properties were supplied by the manufacturer. The results obtained from the packages by using the coupled field analyses were analyzed and the some of the salient results are shown in Figures 4 and 5. As the IC is supplied with the designated voltage it takes a few minutes to reach a steady state due to joule heating. Hence all the results presented are from steady state electrical- thermal coupled field analysis. No transient analysis is presented here due to the practicality of the approach of this investigation. Forced convection values were used in the model at the surface of the IC encapsulations. Figures 4 and 5 show the maximum temperature achieved in the encapsulated package due to joule heating and the XY shear stress developed in the whole package. A high shear stress is developed at the silicon die and the copper lead frame in-plane interface bonded with a conducting silver epoxy adhesive in the respective packages.

The XY shear stress is of significance as the stresses developed in steady state operation can be compared with the actual shear strength of the interface. The FE evaluated shear stresses developed in all the packages should be at least 1.5 times (factor of safety) lower than the shear strength of the silicon die-copper leadframe interface in order to qualify the IC for reliability. The die-shear test, one of the most recommended tests, conducted to evaluate the shear strength is explained in the experimental details section.

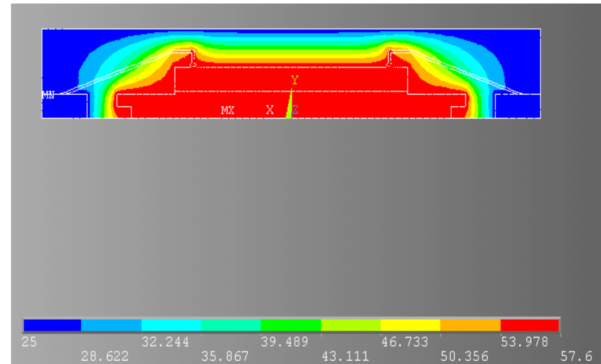

Figure-4. Temperature distribution of 36 TQLMP.

Table-1. Packaging material properties.

Property/Material	Copper	Adhesive epoxy	Silicon	Gold
Youngs Modulus in MPa	1.10E+05	1.15E+04	2.00E+05	8.27E+04
Poissons ratio	0.22	0.35	0.25	0.44
Thermal conductivity in W/mm-K	4.01E-01	2.10E-03	1.30E-01	3.17E-01
Co-efficient of thermal expansion, / ⁰C	1.65E-05	8.50E-05	2.60E-06	1.42E-05
Electrical Resistivity in Ω –mm	1.67E-05	1.00E-04	1	2.35E-05

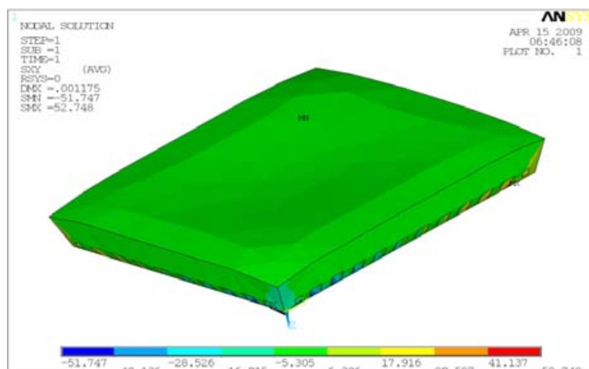

Figure-5. XY shear stress in the 36 TQLMP.

EXPERIMENTAL DETAILS

The die shear test apparatus for the eight different packages is designed to measure the shear strength of the silicon die-copper lead frame interface adhesively bonded with a silver epoxy paste, and is shown schematically in figure 6. Here the silicon die adhesively bonded to the copper lead frame is clamped to the apparatus and a shear beam with a wedge is tightened laterally until the die is sheared from the copper lead frame. The load required to shear the die is noted and the shear strength is calculated based on the surface contact area of the die with the lead frame. For the IC packages, at least about five tests were conducted for every package and the average load taken for evaluation of the shear strength. It should be noted that it is possible to conduct the die shear test only on the ICs without encapsulation. Hence simulation results without encapsulation are relevant for the sake of comparison. Here, temperature rise, the shrinkage pressure due to the encapsulation moulding and the thermal stresses developed in the encapsulation while in operation has a role to play in the origin of the XY shear stress. They are found to affect the magnitude of the XY shear stress for the ICs considered here. The die shear strength evaluated through the experimental setup was found to be higher than the actual stresses developed during operation, by a factor more than 1.5 for all the ICs. The shear stresses developed during

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operation were in the range of 3 to 10 MPa and the actual shear strength of the copper lead frame-silicon die interface was between 10 to 70 MPa depending on the silver-epoxy paste that was used for the bonding. Here, as the die-shear test is done at room temperature and the shear stresses developed in the package are at higher operating temperatures, it was decided to conduct the die shear test for specimens treated at the operating temperatures in an oven. The factor of safety for the various ICs between their shear stresses and shear strengths was found to be at least 5. Hence, for all the packages it was proved that the IC is fail safe at the silicon die- copper lead frame interface at the operating conditions.

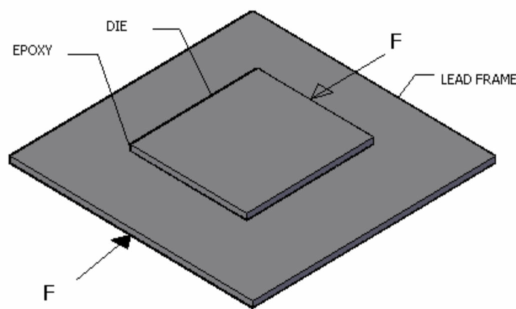

Figure-6. Si- Cu lead frame die shear test.

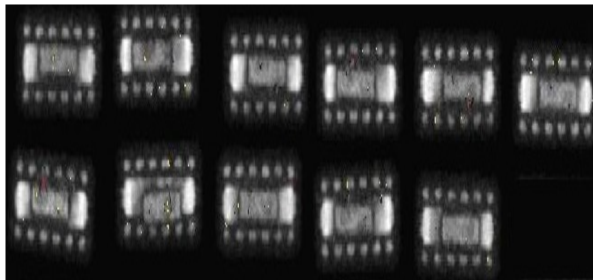

Figure-7(a). 12 L μDLMP SAM image before preconditioning.

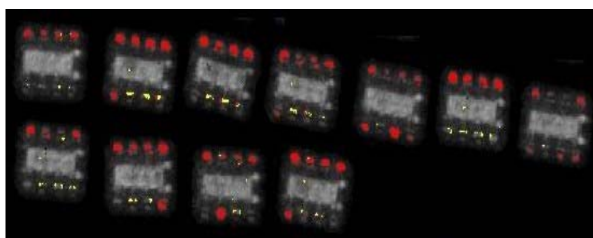

Figure-7(b). 8L μDLMP post conditioning SAM image.

The manufactured ICs are subjected to a preconditioning test involving a few temperature cycles. As the temperature of the ICs is raised beyond 125°C which is above the glass transition temperature of the encapsulant mould compounds and the silver epoxy adhesive, to up to 260°C for lead free products, delaminations were observed in the encapsulated ICs. This was confirmed through Scanning Acoustic Microscope (SAM) observation of the preconditioned specimens through a Sonix, USA, and equipment available at SPEL. Figures 7 (a) and (b) provide the information for two of the IC packages imaged, showing the extent of delaminations prior to and after preconditioning at the aforesaid temperatures for 24 hours or more. The red areas indicate delaminations. As the IC temperature during operation is not expected to go beyond 110.86°C for the 8L μDLMP IC package which was the highest observed among all the packages investigated here and only about 30°C for the 48L and the 56L TQLMP IC packages due to the joule heating analysis it is clear that delaminations occur only when the IC is treated near and above the glass transition temperature of the epoxy for durations as discussed above. As there is a clear margin between the maximum temperature reached during operation and the failure temperature due to the development of thermal stresses, it is found that the IC will not reach its failure limits during operation for all of the ICs considered here except the 8L μDLMP chip. According to the ASTM STP 5229 M rule [6] the MOT (Maximum Operating Temperature) of the material, device/component should be at least 25° Celsius lower than the lowest Tg (normally wet glass transition temperature) of the material. In this case the mould compounds qualify this clause for the 12L μDLMP and the TQLMPs. A mould compound with higher glass transition temperature and good mechanical properties was recommended for the 8L μDLMP as it did not qualify this clause. This was implemented by the manufacturer.
This investigation deals with more reliability analyses based on failure theories and hygrothermal influences. The ensuing sections present the hygrothermal and the failure analyses of all the IC packages.

HYGROTHERMAL ANALYSES

The packages involved in this investigation are polymeric epoxies that are non-hermetic, meaning permeable to moisture and transport of other ingredients. The analytical models for a polymeric material's mechanical behaviour presented are based on the assumption of the environmental conditions. Among the many environmental conditions that may influence polymer mechanical behaviour, changes in temperature and moisture contents are important for discussion. Effects of temperature are usually referred to as "thermal" effects, whereas those of moisture are often referred to as "hygroscopic" effects. The word "hygrothermal" is used to describe the combined effects of temperature and moisture.

There are two principal effects of changes in the hygrothermal environment, on the mechanical behaviour of polymers.

1. Stiffness and strength are altered. Increasing temperature causes a gradual softening of the polymer material up to a point. If the temperature is increased beyond the so called "glass transition" region (indicating a transition from glassy behaviour to rubbery behaviour),

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however, the polymer becomes too soft for use as a structural material. Plasticization of the polymer by absorbed moisture causes a reduction in glass transition temperature (T_g). Thus the wet T_g is always lower than the dry T_g and a corresponding degradation of polymer properties results.

2. Hygrothermal expansion or contractions change the stress and strain distributions in the polymer. Increasing the temperature and moisture content causes swelling of the polymer, whereas reduced temperature and/or moisture content causes contraction. Recent attention is on the hygrothermal reliability aspects of various IC packages [7, 8].

The hygrothermal degradation of the polymer encapsulant strength or stiffness can be estimated by using an empirical Eqn 1 [9], that is

$$F_m = \frac{P}{P_0} = \left[\frac{T_{gw} - T}{T_{go} - T_0} \right]^{1/2}$$

$$T_{gw} = (0.005M_r^2 - 0.1M_r + 1.0)T_{go} \quad (1)$$

Where

F_m = Mechanical property retention ratio,
P = Strength or stiffness after hygrothermal degradation,
P_o = Reference strength or stiffness before degradation,
T = Temperature at which P is to be predicted (^{0}C),
T_{go}= Glass transition temp. for reference dry condition,
T_{gw}=Glass transition temperature for reference wet, condition at moisture content corresponding to property P,
T_o = Test temp. at which Po was measured (25^{0}C),
M_r = Weight percent of moisture at equilibrium.

In our package the encapsulation is made up of a filled epoxy material which absorbs moisture. Two types of encapsulation molding materials were used by the manufacturer. The maximum moisture concentration for the two moulding compounds as determined were 0.23 wt % (Mould compound 1) and 0.3 wt % (Mould compound 2), respectively. The strength or the stiffness retention ratios were calculated for the mould compounds based on the above formula up to the glass transition temperatures. The actual strength of the encapsulant resin is reduced due to the moisture absorption especially at higher temperatures. The strength degradation versus temperature plots for a saturation moisture conditioned mould compound 1 and mould compound 2 are shown in Figures 8 and 9. Shear strength reduction is important.

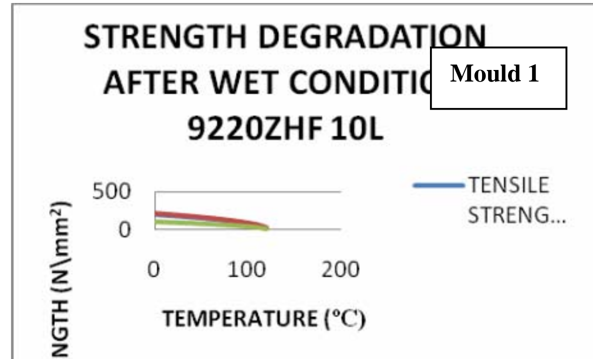

Figure-8. Temp Vs strength plot of mould compound 1.

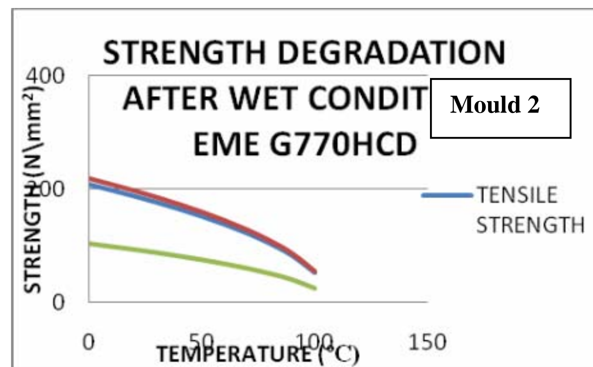

Figure-9. Temp. Vs strength plot of mould compound 2.

FAILURE ANALYSES

FAILURE THEORIES

The failure of composites has been investigated extensively from the micromechanical and the macromechanical points of view. As the encapsulant mould compound is a filled nanocomposite, failure theories for composites are required to describe and predict failure. Failure predictions based on micromechanics, even when they are accurate with regard to failure initiation at critical points, are only approximate with regard to global failure with respect to orthotropy. For these reasons a macromechanical approach to failure analysis is preferred.

Numerous failure theories have been proposed exclusively for composite materials and are available to the composite structural designer. They are classified into three groups, limit or non interactive theories (maximum stress, maximum strain), interactive theories (Tsai-Hill, Tsai-Wu) [10, 11] and partially interactive or failure mode based theories (Hashin-Rotem, Puck). The validity and applicability of the above theories depend on the phenomenological events like interaction between the normal and shear stresses and agreement with experimental results.

AZZI-TSAI HILL THEORY

The Azzi-Tsai-Hill and Tsai-Wu failure theories for composite materials are considered here due to their

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proven accuracy in predicting failure in systems where the normal strengths and the shear strengths interact. According to Azzi-Tsai-Hill theory, in the equation (2), the design is considered to be safe when the left hand side of the equation is less than one.

$$\frac{\sigma_{11}^2}{S_{Lt}^2} + \frac{\sigma_{22}^2}{S_{Tt}^2} - \frac{\sigma_{11}\sigma_{22}}{S_{Lt}^2} + \frac{\tau_{12}^2}{S_{LTs}^2} = 1 \qquad (2)$$

Where

σ_{11} = X (tensile / compressive) stress in MPa
σ_{22} = Y (tensile / compressive) stress in MPa
τ_{12} = Shear stress in MPa
S_{Lt} = Longitudinal tensile strength in MPa
S_{Tt} = Transverse tensile strength in MPa
S_{Lts} = In-plane shear strength in MPa

TSAI-WU FAILURE THEORY

According to Tsai-Wu theory in the equation (3), the design is considered to be safe when the left hand side of the equation is less than one.

$$F_1\,\sigma_{11} + F_2\,\sigma_{22} + F_6\,\tau_{12} + F_{11}\,\sigma_{11}^2 + F_{22}\,\sigma_{22}^2 + F_{66}\,\tau_{12}^2 + 2\,F_{12}\,\sigma_{11}\sigma_{22} = 1 \qquad (3)$$

$$F_1 = \frac{1}{S_{Lt}} - \frac{1}{S_{Lc}} \qquad F_{22} = \frac{1}{S_{Tt}S_{Tc}}$$

$$F_2 = \frac{1}{S_{Tt}} - \frac{1}{S_{Tc}} \qquad F_{66} = \frac{1}{S_{LTs}^2}$$

$$F_{12} = -\tfrac{1}{2}\sqrt{F_{11}F_{22}} \qquad F_{11} = \frac{1}{S_{Lt}S_{Lc}}$$

Where

Other parameters / symbols appear as in equation (2) and
S_{Lc} = Longitudinal compressive strength in MPa
S_{Tc} = Transverse compressive strength in MPa.

FAILURE THEORY VALIDATION

NORMAL CONDITIONING IN 25ºC AMBIENCE

For each of the temperature conditions an ANSYS coupled field analysis was done that provided information about the X, Y and the XY shear stress (which is important for the silver-epoxy sandwich layer between the silicon die and the copper lead frame) developed in the package. Failure theories are applied to check for failure criteria. At normal conditioning i.e. at 25°C ambience as in Figure-10, the following values were obtained for the stresses actually developed and the mean strength of the package.

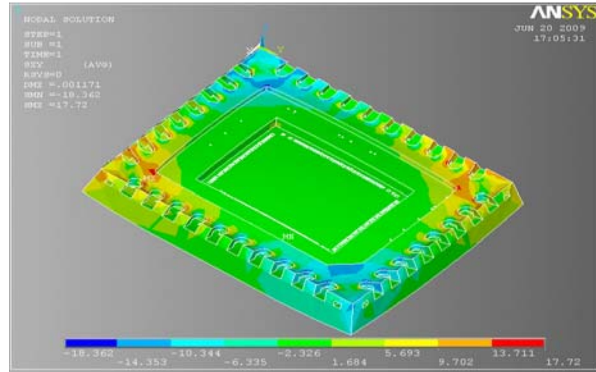

Figure-10. 36L TQLMP - XY shear stress of encapsulation at 25ºC conditioning.

For the 36L TQLMP

X stress in MPa = 42.4
Y stress in MPa = 40.544
XY shear stress in MPa = 17.72
Tensile strength in MPa =185
Compressive strength in MPa = 195
Shear strength in MPa = 92.5

According to Tsai - Wu Failure theory, the LHS is smaller than the RHS, i.e. 0.1093 < 1.

According to Azzi-Tsai-Hill theory, the ratios are 0.0871 (Tensile) / 0.0818(compressive) < 1.

The design is safe for this condition of operation.

AT MAXIMUM OPERATING TEMPERATURE

At the maximum operating temperature as the ambience as in Figure-11, the following values were obtained for the stresses actually developed in the 24L asymmetric TQLMP and the mean strength of the package.

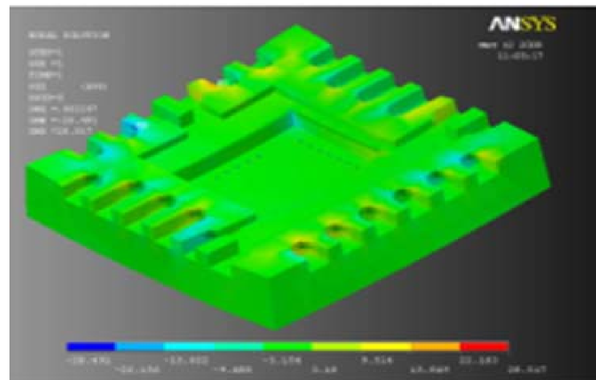

Figure-11. 24L asymmetric TQLMP, Shear stress of encapsulation conditioned at MOT.

For the asymmetric 24L TQLMP at its MOT of 87.5ºC;

X stress = 50.204 MPa
Y Stress = 54.323 MPa

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XY shear stress = 50.793 MPa
Tensile strength= 185 MPa
Compressive strength = 195 MPa
Shear Strength = 92.5 MPa

The Tsai - Wu Failure theory yields a result of 0.401 < 1.

And the Azzi-Tsai-Hill theory yields a result of 0.376 / 0.339 < 1

The IC is thus said to be safe at its MOT. Only the 8L μDLMP was found to be unsafe at its MOT due to a higher operating voltage and the resin wet T_g being almost equal to the MOT. A mould compound with a higher T_g was found to rectify this defect.

AT PEAK CONDITIONING i.e. 125°C FOR 24 HRS

t 125⁰C peak conditioning the following stresses were observed in the symmetric 24L TQLMP encapsulation as shown in Figure-12;

X stress in MPa = 70.509
Y stress in MPa = 98.811
XY shear stress in MPa = 45.793
Tensile strength in MPa = 27.01
Compressive strength in MPa = 28.47
Shear strength in MPa = 13.5

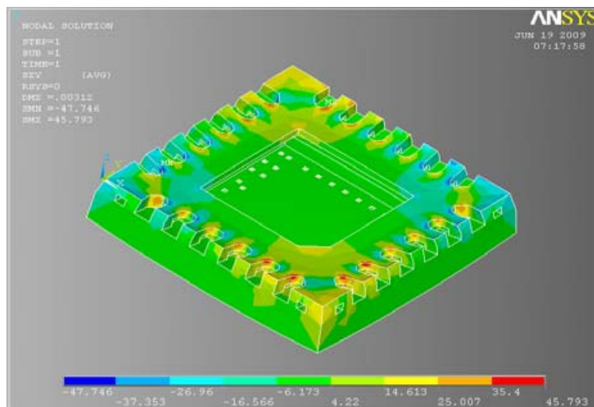

Figure-12. The symmetric 24L TQLMP encapsulation shear stress at 125ºC.

Construction of the failure predictions show that

According to Tsai – Wu Failure theory we get a ratio of 22.29> 1

And according to the Azzi-Tsai-Hill theory we get a ratio of 22.047 (Tensile) / 21.083(compressive) > 1

Thus as the LHS is greater than the RHS, the design is unsafe. The design is completely unsafe after peak conditioning at 125ºC. A reasonable correlation was obtained with that of the preconditioned and post delamination samples of the ICs as imaged with the SAM. As all the products were lead free the appropriate JEDEC standard for conditioning of the ICs was referred to, while hygrothermal reliability studies were conducted [12].

Thus a procedure was developed and implemented in the design and manufacture of μDLMP and TQLMP ICs to visualize and realize the product reliability through modelling, simulation, manufacture and testing. It should be noted that only the static reliability of the products was established here for the customer requirements. Studies on fatigue reliability are on.

CONCLUSIONS

The design and reliability analyses of μDLMP and TQLMP IC packages were discussed in this investigation. The 3 D design was carried out with PRO-E Wildfire 4.0 software and the finite element simulation, with ANSYS FEM software. The simulation results were useful along with the results from the die shear and thermal treatment experiments. The following conclusions could be made from the study.

The joule heating during operation of the IC caused the temperature to rise up in the package. A full transient or a steady state electro-thermal analysis provides this result. Experimental verification was also carried out. The temperature rise due to joule heating caused thermal stresses to build up in the package that caused warping, twisting and bending.

The mechanical stresses thus developed in the package were evaluated employing the electro-thermo-mechanical coupled field analysis using ANSYS software. The silicon die- copper lead frame bonding interface shear stresses (XY shear stresses) could be evaluated for operational conditions. The interfacial stresses developed were lower and an acceptable factor of safety was achieved in the ICs through recommendations for suitable materials selection.

The ICs were found to delaminate when precon ditioned to temperatures in excess of the glass transition temperatures of the mould compound epoxy and the silver epoxy paste. As the maximum test temperatures were in the range of 260°C, the SAM images of the thermally treated ICs revealed the delaminations seen as red areas. However, operational joule heating was not seen to produce any delaminations in all the ICs after the recommendations for mould compound materials were made.

A detailed hygrothermal analysis was carried out on the IC package that provided vital information about the tensile, compressive and shears strengths of the moisture saturated package at elevated temperatures up to the wet glass transition temperature of the mould compounds.

The study establishes the overall static reliability of the ICs with acceptable safety margins at the operating temperatures as substantiated through the application of failure theories.

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