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GAPPED ALTERNATE PHASED OPPOSITE DISPOSITION-PULSE WIDTH MODULATION CONTROL FOR MULTILEVEL INVERTERS

Olusola A. Komolafe and Olufemi I. Olayiwola
Department of Electronic and Electrical Engineering, Obafemi Awolowo University, Ile-Ife, Nigeria
E-Mail: okomolaf@oauife.edu.ng

ABSTRACT

This paper presents a comparative analysis of the harmonics generated in the output waveforms of 3-phase H-bridge cascaded multi-level inverter topology using Sinusoidal Pulse Width Modulation (SPWM) techniques. The Alternate Phased Opposite Disposition- Pulse Width Modulation (APOD-PWM) is one of the best SPWM schemes in achieving reduction in the Total Harmonic Distortion (THD), which is the major parameter often used to assess the suitability of an inverter. However, due to the closely set carrier arrangement, the APOD-PWM produces high THD especially at switching frequencies above 1-kHz. In this paper, a Gapped APOD-PWM is proposed. The switching sequence is similar to the APOD-PWM technique, but it has smaller switching angle. This reduces the switching overlap at boundary positions and hence the THD. The technique was simulated using the MATLAB-SIMULINK toolbox. The output current and voltage signals were evaluated and the THD was computed using SIMULINK-FFT tool. Results show that the proposed technique is able to further reduce THD at all switching frequencies.

Keywords: alternate phased opposite disposition - pulse width modulation, matlab/simulink, GAPOD-PWM, H-bridge, THD.

1. INTRODUCTION

Multi-level inverter topologies have recently attracted more attention due to its high voltage capability, reduced common mode voltages, near sinusoidal outputs, lower switching stress [1] and lower rate of change of voltage with time. Previously, square- and modified square-wave output voltage wave-form inverters were predominant. However, the THD generated by these inverters before filtering is usually above 65%. When the output waveforms from these inverters are not well filtered, the harmonics often results to heat in the system, which leads to lower efficiency and eventual failure of the system [2]. Multilevel inverters are able to reduce harmonics by producing stepped waveform which reduces the voltage stress and therefore THD.

There are various multi-level inverter topologies, which have been extensively discussed in literature, such as the diode clamped cascade (DCC), flying capacitor cascade (FCC), H-bridge cascade [3, 4] and their hybrid topologies [5, 6]. The DCC and FCC are alternate topologies and utilize clamping diodes or capacitors, which makes them more complex to design [7]. The H-bridge cascaded topology has modular layout structure and utilizes lesser number of components when compare with the DCC and FCC. They however require more DC sources depending on the number of bridges in the cascade design.

In order to effectively reduce the harmonic distortion that is closely associated with switch-mode power supply using multilevel inverter topologies, various modulation techniques have been proposed. One of the commonly used multilevel inverter control method is the Sinusoidal Pulse Wave Modulation technique. It requires multiple-carriers (usually triangular carriers) which are usually modulated by a sine wave. The carrier signals can be arranged in different modes to achieve voltage harmonics reduction. The four basic carrier arrangements are discussed by Y. S. Mohammed *et al*., [8]. The number of carriers used depends on the number of line-voltage levels to be produced. To produce n- voltage levels, (n-1) carriers are required. These carriers are then modulated by a sinusoidal wave at the required line frequency. A comparison of the Sinusoidal Pulse Width Modulation multi-carrier techniques for multilevel inverters shows that the effectiveness of each technique is dependent on the modulation technique, switching frequency, and modulation index [9].

Contrary to the operational norm of inverters at low indices (linear range) as discussed by A. M. Gole [10], it has been shown that higher voltages and reduced harmonics can still be obtained at slightly higher modulation indices above m_a=1 [11]. J. R. Uthayakumar *et al*., [12] proposed Carrier Overlap PWM (COPWM) and Varying Frequency PWM (VFPWM) at modulating frequency index (m_f) of 40. These techniques are based on the control freedom degrees for asymmetrical H-bridge topology. Govindaraju *et al*., [13] also proposed a variation of hybrid phase disposition PWM technique and the associated switching losses involved in his technique. He was able to reduce the THD at frequency modulation index of 21, to about 25% in 5-level H-bridge topology. S. A. Bashi *et al*., [14] also used APOD-PWM technique to reduce the THD for 5-level H-cascade inverter to about 17% at switching frequency of 300Hz and amplitude modulation index m_a = 1.

The arrangement of the carrier signals in the APOD-PWM technique is such that, modulation at boundary points by the modulating signal creates multiple switching signals, which deliver additional harmonics at the boundary points. In this paper a Gapped APOD-PWM is proposed which is able to further reduce the observed harmonics by reducing the switching occurrences at the

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boundary points. The GAPOD-PWM technique reduces harmonics of the output-phase voltages significantly at various switching frequencies. Results for symmetrical H-bridge topology at switching frequency range between 300Hz - 45 kHz and modulation index m_a =1 is presented. The THD for 5-level and 7-level H-bridge cascade are presented and compared in this paper.

2. DESIGN AND OPERATION OF THE H-BRIDGE CASCADE MULTILEVEL INVERTER

The three-phase H-bridge cascade inverter is shown in Figure-1. The basic architecture is extensively discussed by M. K. Vijaya and K. K. C. Deekshit [15]. The switching device of choice is the Insulated Gate Bipolar-Junction Transistor (IGBT). This is because of its high power capability and high switching frequency characteristics. The symmetrical H-bridge cascade inverter topology delivers staircase output voltage using several levels of DC voltages on each bridge. If n is the number of required voltage levels, then the number of voltage sources (cascades) is given by $\frac{n-1}{2}$. Increase in the number of cascaded levels reduces the voltage stress at the switches, so that output waveforms tend to be sinusoidal waveforms with reduced harmonic distortion.

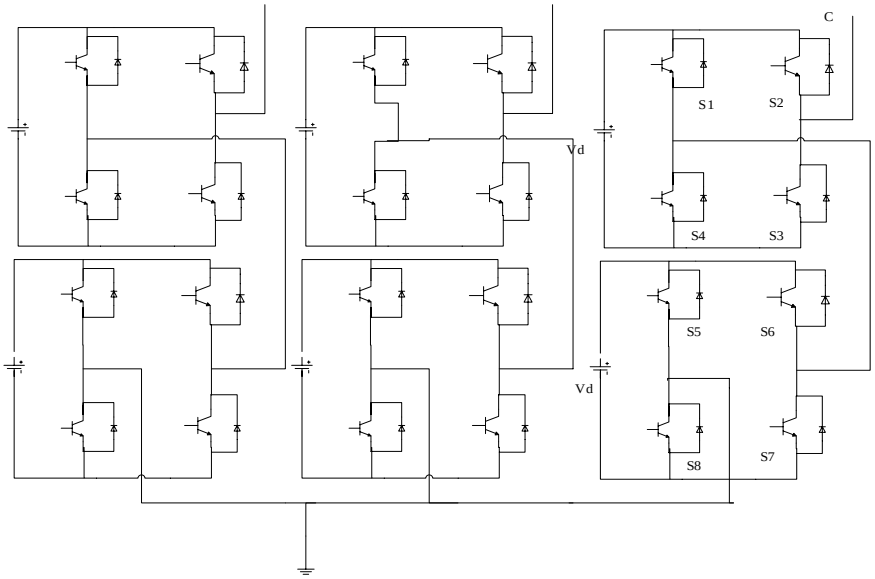

Figure-1. Three Phase 5-level H-bridge cascade.

The signals to the switches of the H-bridge are modulated using the APOD and GAPOD-PWM technique. These modulation techniques involve the natural sampling of several carrier signals typically triangular waveforms which are arranged in vertical/horizontal shifts as defined by the modulation technique used and required number of voltage levels to be produced. All the carriers often have the same frequency and amplitude except in varying frequency-PWM proposed by J. R. Uthayakumar *et al*., [12].

a) H-Bridge signals modulation using alternate phased-opposite disposition - pulse width modulation technique

The APOD-PWM is a simple modulation technique which is achievable without the complex mathematical equations required when using Simple Harmonic Elimination-PWM or Space Vector-PWM. The most important considerations are the modulator - carrier arrangement and logic combination for the comparation of signals. In order to obtain a 5-level voltage output inverter, the carrier signals disposition is electronically measured from the origin (0 volts per division) as shown in Figure-1. Each carrier has amplitude of 1volts per division, such that, when n carriers are used, the peak to peak carrier amplitude $V_c = \pm\frac{n}{2}$. This implies that, at m_a=1, the peak to peak amplitude of the modulating signal $V_m = \pm\frac{n}{2}$. The carrier signals phased arrangement is such, that they are 180^0 out of phase to each other. The switching angle which is measured in degrees (°) and switching sequence are thus obtained as a result of the signals comparison/modulation logic. The switching point occurs at intersection points of both the modulating and carrier signal and it determines the turn on/off of the switches.

$$\theta = 2\pi ft \quad (1)$$

Where, f is the modulating frequency and t is the switching time at the intersection. The modulating and carrier signals arrangement for the APOD-PWM technique is as shown in Figure-2.

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b) H-Bridge signals modulation using gapped alternate phased-opposite disposition-pulse width modulation (GAPOD-PWM) technique

The proposed GAPOD-PWM technique is a variation of the APOD-PWM technique in that, the phased arrangement of the carrier signals are maintained. However, additional reduction in the voltage stress is obtained by increasing the degree of freedom of the carrier disposition.

The amplitude of the carrier signals is retained at 1 volt per division, while the disposition is measured from desired voltage level. In this paper, the carrier disposition is measured from 1volt per division as shown in Figure-2. Also, the 1 volt per division measurement is maintained between each carrier. This implies that to obtain n-level voltage output, where n-1 carriers are required, the peak to peak carrier amplitude $V_c = \pm n$ and peak to peak amplitude of the modulating signal $V_m = \pm n$, when m_a=1.

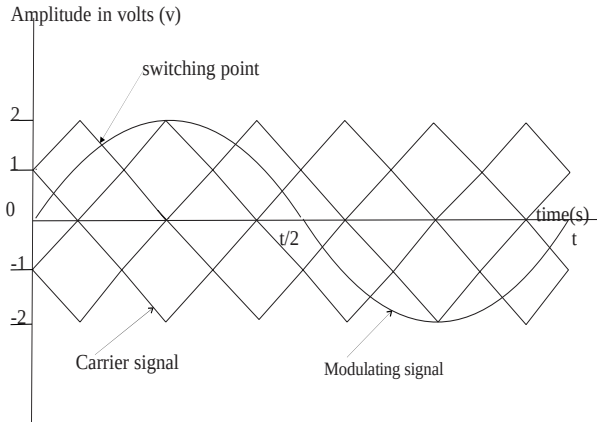

Figure-2. APOD-PWM carrier arrangement.

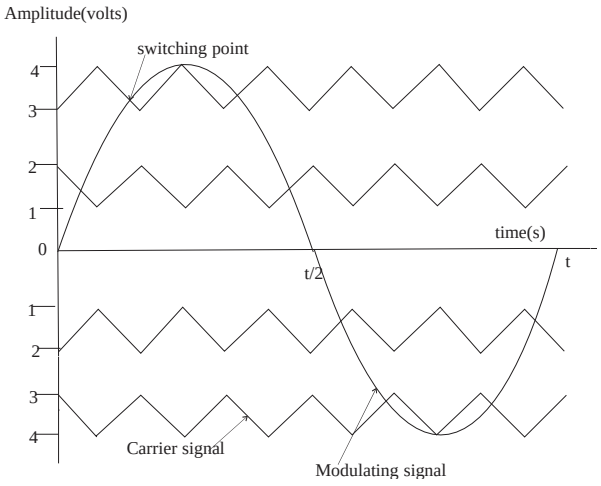

Figure-3. Gapped APOD-PWM carrier arrangement.

It is observed that since the value of V_m for GAPOD-PWM is higher than that of APOD-PWM; the pulses produced upon comparison of GAPOD-PWM signals turns on at an earlier time i.e., has smaller switching angle than when compared to that of APOD-PWM. The switching sequence and switching angle are also obtained as a result of the signals comparison/modulation logic.

The signals arrangement for GAPOD-PWM technique is shown in Figure-3.

c) Basic inverter equations and losses

The design of an inverter is done using various indices. These indices are obtained from the various the parameters that contribute to the efficiency of the inverter.

The switching frequency is estimated using frequency modulation index m_f which is given by:

$$m_f = \frac{f_c}{f_m} \tag{2}$$

Where, f_m is the modulating frequency and f_c is the carrier wave frequency. While the amplitude modulation index is expressed as:

$$m_a = \frac{V_m}{V_c(n-1)} \tag{3}$$

Where, V_m is the peak to peak value of the modulating wave and V_c is the amplitude of the carrier signal.

The THD is measured as the ratio of all the harmonics in a switching system to the fundamental unit.

$$\text{THD} = \frac{\sqrt{\sum_{i=2}^{n} A}}{A} \tag{4}$$

Where, A_i is the i_{th} voltage/current harmonic value. Pulse width modulated systems are usually characterized with power and harmonic losses which result from the switching and conduction losses of the switches/transistors/thyristors that are used [15, 16]. The losses in the modulation techniques cause the average reduction in phase-phase voltages at each switching frequencies. An estimate of the power loses (P_{loss}) in inverter systems can be evaluated as the sum of the switching loss (P_{sw}) and conduction loss (P_{cond}) [17].

$$P_{loss} = P_{sw} + P_{cond} \tag{5}$$

Where

$$P_{sw} = E_{sw} * f_{sw} \tag{6}$$

E_{sw} is switching energy and f_{sw} is switching frequency. Therefore, higher switching frequencies, result in higher power losses and also, lower current harmonics.

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The losses in the techniques used are estimated using the power loss equations below:

$$P_{cond} = I_c * V_{ce} * D \quad (7)$$

$$V_{ce} = VTO + RCE * I_c \quad (8)$$

$$I_c = \frac{\sqrt{\left[R_{thJC} * VTO^2 + 4 * RCE * \left(T_{j\max} - T_c\right)\right]}}{2 * RCE * \sqrt{R_{thJC}}} - \frac{VTO}{2 * RCE} \quad (9)$$

The switching loss P_{sw} can be similarly evaluated as:

$$P_{sw} = \frac{1}{2\pi}\left(E_{on} + E_{off}\right) * f_{sw} \quad (10)$$

Where

$D = \frac{t_p}{T}$ is the duty cycle, t_p is the pulse length

V_{ce} is the collector-emitter voltage, I_c the continuous collector current,
VTO, RCE, E_{on}, E_{off} are interpolated voltages and resistance parameters from datasheet
R_{thJC} = the IGBT junction-case thermal resistance
V_{ce} (sat) = the collector-emitter saturation voltage, and
T_j, T_c = junction and case temperature of the switch

3. SIMULATION CIRCUITS AND WAVEFORMS

The MATLAB/SIMULINK model for 5-level H-bridge cascaded multilevel inverter is shown in Figure-1. The signals modulation logic used to turn the switches of each phase on the bridge on/off with either the APOD-PWM or Gapped APOD-PWM carrier arrangement is shown in Figure-4.

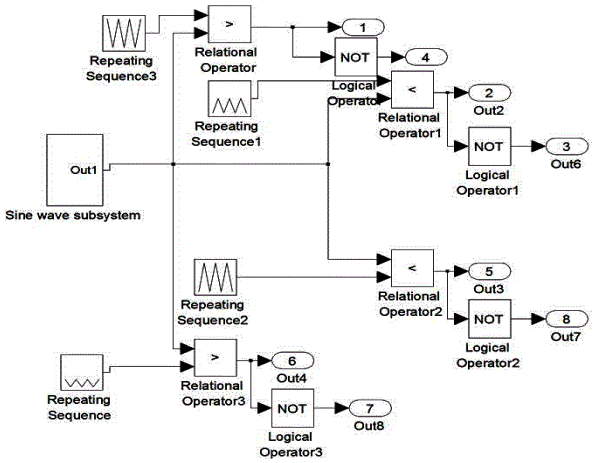

Figure-4. Modulation logic for each phase.

Figure-4 shows how a single phase of the inverter's three phases is modulated. Other phases are switched by the same triggering sequence whose sine waves are out of phase by 120^0.

In MATLAB-SIMULINK, the carrier wave sources are set according to the frequency and amplitude disposition to be used. The amplitude disposition used for each triangular carrier period in the modulation techniques is defined with reference to Figures 2 and 3, as below:

Table-1. Carrier disposition.

	Modulation technique	
Switches	**GAPOD-PWM** (Volts)	**APOD-PWM** (Volts)
S1 and S4	[2,1,2]	[1,0,1]
S2 and S3	[-2,-1,-2]	[-1,0,-1]
S5 and S8	[3,4,3]	[1,2,1]
S6 and S7	[-3,-4,-3]	[-1,-2,-1]

The carrier and modulating signals compared as in Figure-4 above produces modulated signals shown in Figure-5. As shown in Figure-5, the inverted form of signals that is supplied to switches S1, S2, S5 and S6 is supplied to switches S4, S3, S8 and S7, respectively. These signals turn the IGBTs on and off in a sequence, shown by the switching matrix in Table-2.

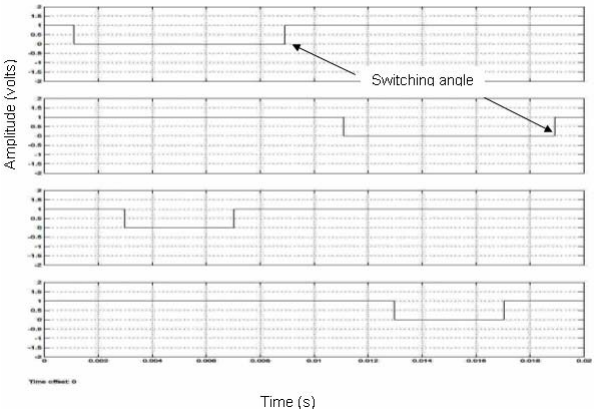

Figure-5. Pulses from modulated signals.

Table-2. H-Cascade switching matrix.

	Switches							
Voltage level	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**
$2V_d$	1	0	0	1	1	0	0	1
V_d	1	0	0	1	1	0	1	0
0	1	0	1	0	1	0	1	0
$-V_d$	0	1	1	0	1	0	1	0
$-2V_d$	0	1	1	0	0	1	1	0

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Figure-6 shows how the stepped voltage waveform determined by the switching matrix of Table-2 in 5-level H-cascaded bridge inverter is obtained with a DC supply voltage V_d of 132-V.

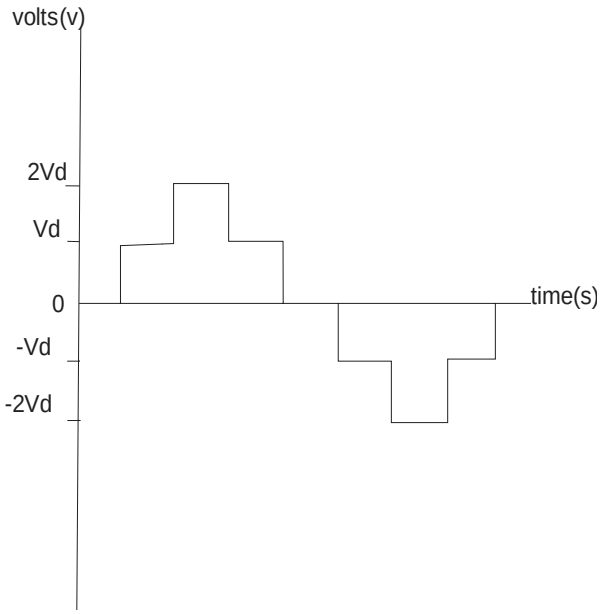

Figure-6. 5- Level Stepped waveform produced using GAPOD-PWM.

4. RESULTS

The terminals of the cascaded H-bridge topology are star connected to a three-phase series load. The nominal phase-phase output voltage is 400-V, nominal frequency is 50Hz, active power is 2kW and inductive reactive power is 500Var.

Figures 7 and 8 shows the obtained line-neutral and line-line voltage waveforms for both APOD-PWM and GAPOD-PWM respectively for m_f =6. It is observed that the resultant line-to-line voltage has seven levels and therefore more sinusoidal as compared with the line-neutral waveform. This implies a reduction in the phase harmonics as compared with the line-neutral voltages.

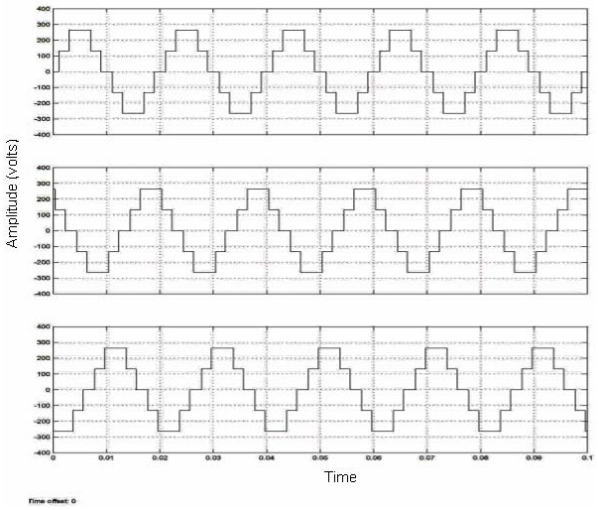

Figure-7. 5-level line voltage wave-form.

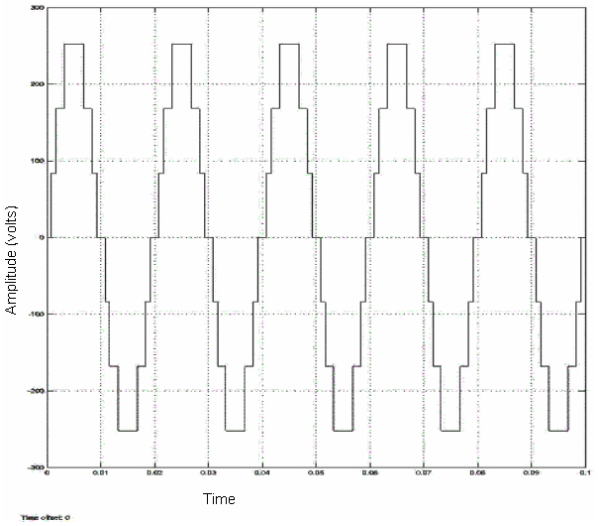

Figure-8. Voltage wave-form for 7-level H-bridge cascade.

The voltage and current THDs measured at different switching frequencies are also shown in Tables 3-6 below.

Table-3. 5-level APOD-PWM.

m_a=1	300 Hz		1.2kHz		15kHz		20.25kHz		45kHz	
	MAG	THD (%)	MAG	THD (%)	MAG	THD (%)	MAG	THD (%)	MAG	THD (%)
V_{ab}(V)	423.5	16.5	401.7	24.21	401.2	25.75	401.2	25.53	402.3	25.12
I_a(A)	3.152	5.62	2.986	3.79	2.985	0.41	2.994	1.96	2.993	0.31

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Table-4. 5-level GAPOD-PWM.

m_a=1	300 Hz		1.2kHz		15kHz		20.25kHz		45kHz	
	MAG	THD (%)	MAG	THD (%)	MAG	THD (%)	MAG	THD (%)	MAG	THD (%)
V_{ab}(V)	447.1	13.66	406.1	20.68	400.8	21.81	400.5	21.76	400.3	21.49
I_a(A)	3.328	3.99	3.022	5.11	2.977	3.38	2.985	3.53	2.992	3.65

Table-5. 7-level APOD-PWM.

m_a=1	300 Hz		1.2kHz		15kHz		20.25kHz		45kHz	
	MAG	THD (%)	MAG	THD (%)	MAG	THD (%)	MAG	THD (%)	MAG	THD (%)
V_{ab}(V)	433.1	11.33	399.9	14.25	400.1	14.91	400	14.84	399.7	14.66
I_a(A)	3.224	6.45	2.974	2.73	2.976	0.40	2.975	1.13	2.979	0.40

Table-6. 7-level GAPOD-PWM.

m_a=1	300 Hz		1.2kHz		15kHz		20.25kHz		45kHz	
	MAG	THD (%)	MAG	THD (%)	MAG	THD (%)	MAG	THD (%)	MAG	THD (%)
V_{ab}(V)	444.1	9.41	408	14.47	402.9	14.65	403.8	14.82	403.9	14.52
I_a(A)	3.305	4.94	3.035	5.03	3	5.96	3.004	6.14	3.003	6.07

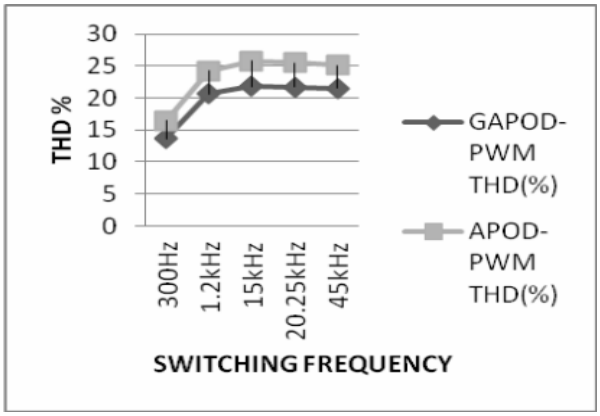

Figure-9. 5-level THD comparison for both techniques.

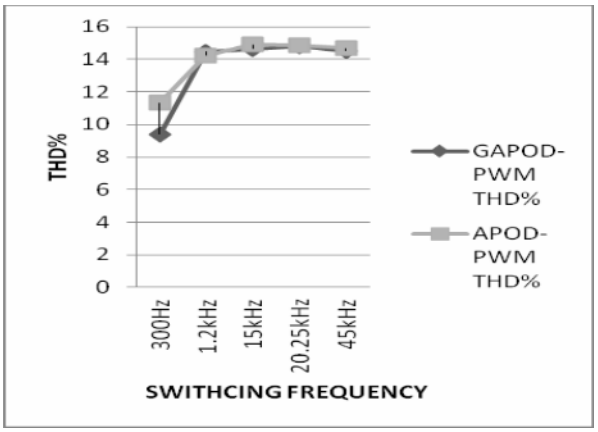

Figure-10. 7-level comparison for both techniques.

It is observed that at linear modulation range ma =1, the output voltage is given by:

$$0.87\frac{V_d\sqrt{3}}{2}(n-1) \le |V_{ab}| = |V_{bc}| = |V_{ca}| < \frac{V_d\sqrt{3}}{2}(n-1) \quad (11)$$

Where

V_d is input voltage and n is number of line-neutral voltage levels.

GAPOD-PWM yields reduced voltage harmonics while APOD-PWM yields slightly preferable current harmonics. Also, that voltage harmonics tend to increase with increasing switching frequency. This can be attributed to the rapid switching that take place at boundary points within the modulating system. When the carrier and modulating signals are compared for both the APOD-PWM and GAPOD-PWM, it is observed that the GAPOD-PWM has shorter boundary comparation period and therefore reduces the harmonics at this boundary points. However, the conduction period (duty cycle) is slightly increased and therefore, more conduction loss is observed.

Infineon SK06N60 (600V, 6A) [18] igbt is used to estimate the power loss using the two techniques. All parameters used with the exception of duty cycle and V_d are derived from the datasheet (T_c and T_j are taken as 100^{o}C) (Infineon Technologies, 2013). Total power loss P_{loss} per switch using both modulation techniques for the 5-level H-bridge cascade is shown in the table below:

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Table-7. Total power loss comparison.

	Upper bridge switch loss (W)		**Lower bridge switch loss** (W)	
Switching frequency	**GAPOD-PWM**	**APOD-PWM**	**GAPOD-WM**	**APOD-PWM**
300Hz	17.79	16.58	22.72	20.99
1.2kHz	23.66	20.37	28.59	24.78
15kHz	113.71	78.61	118.64	83.02
20.25kHz	147.93	100.77	152.86	105.18
45kHz	308.83	205.21	313.76	209.62

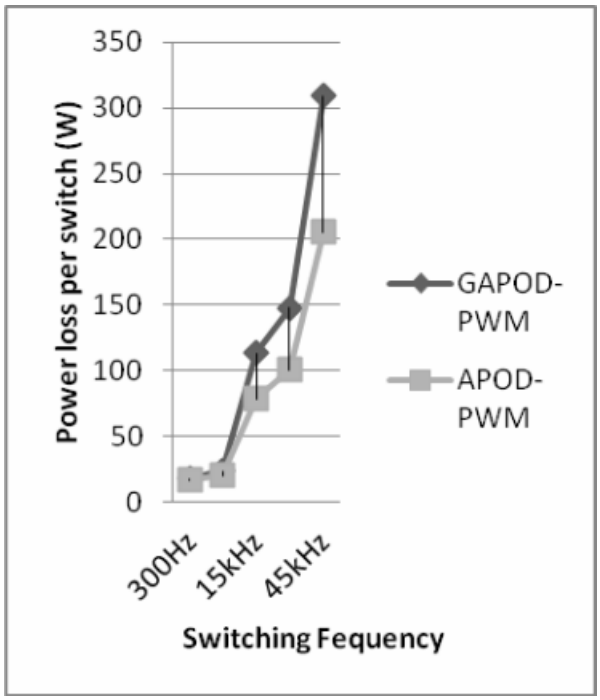

Figure-11. Upper bridge power loss comparison.

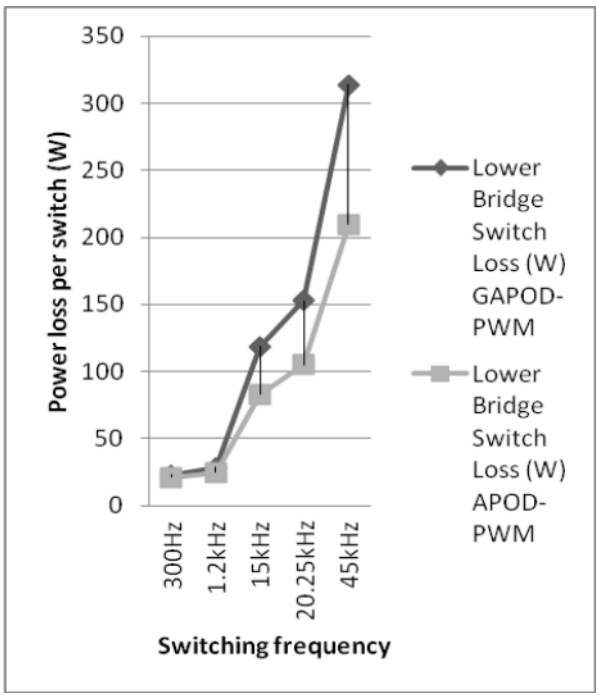

Figure-12. Comparison of lower bridge power loss.

There is therefore need for higher input V_d to produce the same phase output AC voltage.

5. CONCLUSIONS

The results presented above shows reduction in voltage and current THD both at all switching frequencies and when the number of cascade is increased for both modulation techniques. Also, Gapped APOD-PWM tends to yield more voltage THD reduction at lower frequencies. APOD-PWM generally yields better current THD at all frequencies than Gapped APOD-PWM. Therefore, Gapped APOD-PWM can be very effective for voltage-fed systems that do not necessarily require high switching frequencies such as inverters and voltage-fed induction drives. APOD-PWM on the other hand is more effective for current fed systems and drives.

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