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SI IMPATT DIODE OPTIMIZATION FOR PERFORMANCE ANALYSIS: AN OVERVIEW

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ABSTRACT

IMPATT diodes have received much attention in the few years. Based on the previous studies, device performance has been improved from year to year. This paper is focused on the Silicon IMPATT diode because of the reliable and more mature technology. The progress of Si IMPATT diodes based on millimeter-wave applications is reviewed. The development of Si IMPATT which includes the structures, design consideration, fabrication process, techniques for improvement on output power and efficiency is made to review in this paper.

Keywords: IMPATT, silicon, structures, techniques, output power, efficiency.

INTRODUCTION

A proper understanding on IMPATT diodes is important in order to determine the properties of the device. For generating an RF signal, a device such as IMPATT diode is needed. IMPATT diodes are the one of the most powerful millimeter wave sources. IMPATT stands for 'Impact Ionization Avalanche Transit Time'. IMPATT is basically a p+n junction diode; reverse biased to breakdown and can generate microwave or RF power when it is properly embedded in a resonant cavity (Mishra, 2011). It provides the highest output power in the millimeter-wave frequency range among solid-state devices (Ke-Lin Du and Swamy, 2010). The IMPATT diode consists of a reverse-biased pn junction and a drift zone and it may be operated at frequencies from 10 up to 350 GHz, at relatively high powers (Ke-Lin Du and Swamy, 2010).

The two important term of IMPATT diode are negative resistance and impact ionization. These diodes employ impact ionization and transit time properties of semiconductor structures to produce negative resistance at microwave frequencies (Srivastava, 2006). In IMPATT devices, negative resistances arise from two delays which cause to lag behind voltage. These are the avalanche delay caused by finite build-up time of avalanche current and the transit time delay from the finite time taken by the carriers to cross the drift region (Srivastava, 2006). When these two delays add up to 180o, the diode electronic resistance is negative corresponding to that frequency (Srivastava, 2006). Impact ionization is a process that forms additional holes and electrons by knocking them out of the crystal structure when the electrons and holes velocity become so high (Salivahanan, 2008).

The IMPATT diode family includes many different junction and metal semiconductor devices such as Si, GaAs, GaN and so on. The main advantage of IMPATT diode is their high power capability. However these diodes have a major drawback which is high level of phase noise (Băjenescu, 2010). IMPATTs have been used in microwave and millimeter wave (digital and analog) communication system, in radars for civilian purposes and in missiles for defence systems (Roy and Mitra, 2003).

During the initial phase of development of IMPATT devices, Si (Silicon) was mainly used as substrate semiconductor materials for IMPATT fabrication. Then the IMPATT development started with different semiconductor materials like GaAs (Eisele *et al.*, 1992), InP (Chen *et al*., 2996), GaN (Chakrabati, *et al*., 2011), etc. along with Silicon to achieve higher efficiency, power output and frequency range. However, silicon remains the most important material for millimeter-wave IMPATTs because of its advanced technology and stability. Silicon devices more stable and reliable and are based on a more mature technology. From that, the present paper only focuses on the Silicon IMPATT diode and the design consideration in designing the device. The present paper also carries out the type of Silicon IMPATT diode, the optimization techniques in order to improve the performance of Si IMPATT diodes from the previous researches.

STRUCTURES OF IMPATT DIODE

Single drift region (SDR)

The first SDR diode was proposed by Read (Read, 1958) which consists of a single drift region and a single avalanche region with p+nn+ structure. The doping density for p+ and n+ is around 1020 atoms/cm^3. For i region, it is around 1013 atoms/cm^3. The same n and p regions are between 1016 and 1017 atoms/cm^3, and for i region it is around 1013 atoms/cm^3. The structure is shown in Figure-1 (Roy and Mitra, 2003).

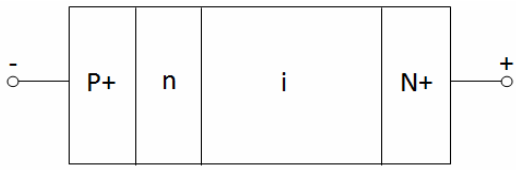

Figure-1. Structure of single drift region of IMPATT diode (SDR).

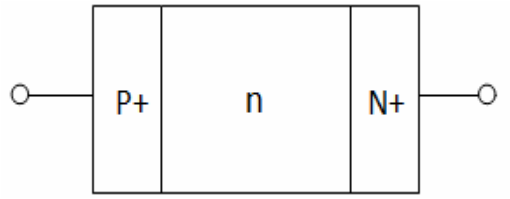

Figure-2. Structure of p+nn+ SDR.

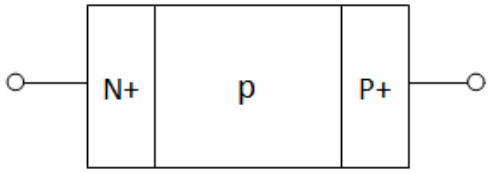

Figure-3. Structure of n+pp+ SDR.

Figures 2 and 3 (Roy and Mitra, 2003) shows the p+-n-n+ and n+-p-p+ structure respectively. Comparisons of n+-p-p+ and p+-n-n+ junction silicon diodes for IMPATT device have been reported using digital-computer program (Udelson and Ward, 1971). The structures of n+-p-p+ may result higher efficiency of operation for IMPATTs. The performance is predicted to improve on the basis of an expected narrower effective avalanche region for the n+-p-p+ structure. For p+-n-n+ structure, the simulated IMPATT-oscillator performance utilizing a 3.6 µm-wide n region doped to 6 × 1015 cm-3 had been investigated (Udelson and Ward, 1971). A maximum theoretical efficiency of 13.9% at a frequency of about 11 GHz was calculated. The maximum efficiency for n+-p-p+ structure was 20.1% and this improvement of efficiency is primarily due to increase of the phase angle (Udelson and Ward, 1971). Afterward, comparison of efficiency, power output and other important operating characteristic of both n+-p-p+ and p+-n-n+ have been employed (Udelson and Ward, 1971). By comparing the p+-n-n+ (n-type) and p+-p-n+ (p-type), the n-type Si IMPATT diode has the higher output power. The p-type structure also can get the similar output power same as n-type output power if when it used the technique of punch-through factor.

Several studies have been developed to determining the properties of single drift region IMPATT diode. The earlier study was reported by Read which proposed high frequency of negative-resistance diode (Read, 1958). New method to reduce the resistance of millimeter-wave IMPATT diodes by employing ion-implantation techniques has been proposed (Hirashi, 1975). From the report, it assumed that if the series resistance of SDR diodes is fully reduced, SDR diodes might have the same properties as DDR diodes. The contact resistance of the ohmic-contact metal (PtSi) can be reduce by implanting arsenic ions into n+ substrate and etching off the surface by about 500 A (Hirashi, 1975).

The use of a lateral IMPATT diode built in 0.25µm CMOS technology was investigated (Al-Attar, 2004). They have proposed a SDR structure, which consists of p+, n and n+ regions that are implemented using standard source/drain, n-well and ohmic contact diffusion region. The dimension of the diode is 0.5µm × 100µm and Figure-4 shows the lateral IMPATT diode structure (Al-Attar, 2004).

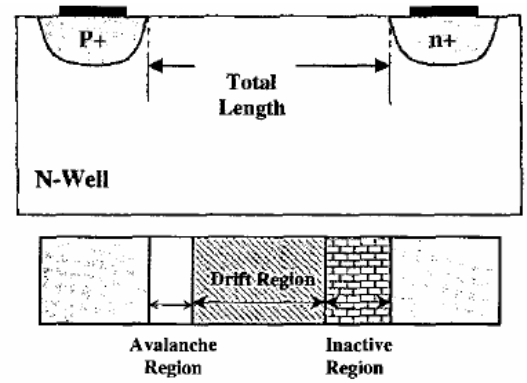

Figure-4. Lateral IMPATT diode structure, showing the avalanche region, drift region and the inactive region.

Monolithic integrated IMPATTs were fabricated in 0.18µm standard complementary metal-oxide-semiconductor technology (CMOS) (Al-Attar and Lee, 2005). This type of device may be suited to use in millimeter-wave systems for various applications because of the cost efficiency and the robustness of standard CMOS manufacturing (Al-Attar and Lee, 2005).

P-type single-drift IMPATT diodes for Y-band frequencies were fabricated with a single diffusion process (Leistner, 1981). This design has used doping concentration of about 7 to 9 × 1016 cm^{-3} which corresponds to a resistivity of active layer of 0.3 to 0.35 Ωcm (Leistner, 1981). This paper has compared with the n-type diode with the similar designed as p-type and p-type diodes deliver more output power and higher maximum efficiency (Leistner, 1981).

P+nn+ SDR IMPATT diode profile has been used in this work with layer n-layer doping concentration of 3.0 × 1017 cm^{-3} (Wenger, 1983). High conductivity arsenic doped n+ layer is applied to minimize both the series resistance in the substrate and the contact resistance of the substrate metallization. This work has developed for D-band frequencies, which in range 140 GHz (Wenger, 1983).

SDR IMPATT diodes have been developed over the 300 GHz bands by several authors (Ino, 1976 - Ishibashi, 1976). T. Ishibashi *et al*. have reported results on the performance of ion-implanted single drift region IMPATT diode with p+-p-n+ structure (Ino, 1976). The highest frequency measured to date is 394 GHz, which was obtained with the 17 µm-diameter diode (Ino, 1976). In another report, they also have reported SDR IMPATT diodes with p+-n-n+ structure that operated continuously in 200 GHz and 300 GHz bands (Ino, 1976). In order to maintain the high value of transfer resistance, it is important to reduce the diode series resistance, Rs. A p+ - n junction structure was formed by thermal diffusion of

boron and ion implantation of phosphorus ions. From this technique, the original n- epitaxial layer of 0.4 µm has been reduced to 0.14 µm and the series resistance was 0.27 Ω for a diode 23 µm diameter (Ino, 1976).

Double drift region (DDR)

A DDR diode has p+-p-n-n+ structure. The different DDR compared to SDR is that consist of two-drift region, one for electrons and other for holes on either side of central avalanche zone (Roy and Mitra, 2003). Electrons and holes emerge from the central avalanche zone and more respectively toward the positive and negative terminals of the device with saturated drift velocity (Roy and Mitra, 2003). The DDR diode produced more high frequency power than the SDR, as each type of carriers in the corresponding drift zone makes the contribution to the power (Roy and Mitra, 2003). Figure-5 shows the structure of DDR IMPATT diode (Roy and Mitra, 2003).

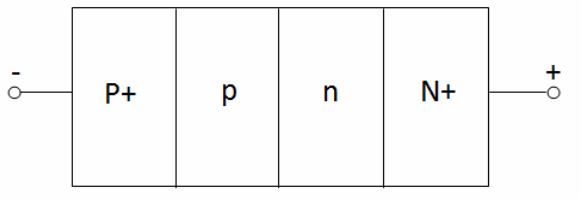

Figure-5. Structure of double drift region of IMPATT diode (DDR).

DDR have many advantages compared to SDR IMPATTs. Since DDR has two drift regions, the double-drift region unit can have essentially double the area of the corresponding (in frequency) single-drift region unit and maintain the same microwave impedance level [19]. Series resistance associated with the contacting n+ and p+ regions will correspondingly be reduced by increase in area. Since only one avalanche region is required for both drift region, increased is also expected (Scharfetter, 1970).

DDR IMPATT diodes (p+pnn+) that employed ion implantation also have been proposed (Seidel, 1970). By referring the fabrication techniques that have been used, the n layer was selected with 6 × 1016/cm^{-3} with the thickness of 1.4µm. Boron implantation were done with 0.6µm and 6 × 1016/cm^{-3}. P+ contact was form with thickness of 0.15 µm and anneals the implanted boron (Seidel, 1970). This condition of the structure has been fabricated and the result of power, 640 mW at 50 GHz was obtained.

In the previous paper (Seidel, 1970), it shows that the higher efficiencies and higher output powers have been obtained from the DDR IMPATTs compared to SDR IMPATTs. This observation is tested for the frequency range from 50 GHz to 100 GHz.

Properties of single-drift abrupt junction IMPATT diodes have been reported (Seddik, 1974) with different punch-through factors (PTF) and compared to the symmetrical and asymmetrical double-drift diode structures. For SDR, the p+-n-n+ and n+-p-p+ has been designed with depletion layer width of 1 µm and different PTFs are considered (Seddik, 1974). The low negative Q is desirable in those devices which can be achieved when the decreasing of PTF. The low negative Q also can be achieved by increasing the peak negative conductance as well as the peak of frequency (Seddik, 1974). The symmetrical p+-p-n-n+ diode is structures using depletion layer width of 1.76 µm while two types of asymmetrical DDR structures are considered which is equal and unequal depletion region layer width.

DDR structures is superior to the original p+-n-n+ SDR IMPATT structure because of the increase power generating capability due to two drift zones and because the junction area of a DDR diode can be larger than a SDR diode for a given impedance level (Midford, 1979). DDR diode is greater by a factor of approximately 2.7 than for a corresponding SDR device because of the differences in the silicon electron and hole ionization rates and saturated drift velocities, the profile should be asymmetric with the p-layer somewhat narrower (Midford, 1979). In designing structures, the doping levels and thickness of p- or n-type region should be chosen. If either the p or n -type region is too wide for the doping level, some of the high resistivity material will remain undepleted and will contribute to parasitic series resistance with reduced RF power and efficiency (Midford, 1979). Table-1 show the design values for doping level and active region widths appropriate to symmetric DDR CW IMPATTs for frequencies ranging from 40 to 225 GHz that are based on the theoretical analyses and on the experimental results (Midford, 1979).

Table-1. Design parameter for millimeter wave CW.

Approximate frequency (GHz)	**ND = NA**(cm^{-3})	**Active region width** (µm)	**Diode breakdown voltage** (V)
225	5.5 × 1017	0.25	8.5
170	4.5 × 1017	0.32	10.0
94	1.8 × 1017	0.60	16.0
60	1.0 × 1017	0.90	22.0
40	6.0 × 1016	1.20	28.0

By referring to the previous paper (Al-Attar and Lee, 2005), a lateral double-drift region IMPATT structure have been proposed which it can be fabricated in standard complementary metal oxide (CMOS) technology (Acharyya, 2012). The p+-p-n-n+ structure is designed to operate at 94 GHz window frequency in standard 0.18 µm CMOS technology. Figure-6 shows the lateral DDR IMPATT structure which contact layers (p+ and n+ layers) and drift layers (p and n epitaxial layers) are adjacent to the substrate surface. Figure-6 shows that the n-well process can be used to fabricate p+-p-n-n+ structured lateral IMPATT device in standard CMOS technology. For 94 GHz diode, the n and p epitaxial layer thickness that have been used are 0.34 µm and 0.32 µm, respectively. This planar structure of lateral DDR IMPATT devices monolithic integration and combining devices in series will be much easier compared to the conventional vertically oriented IMPATTs (Acharyya, 2012).

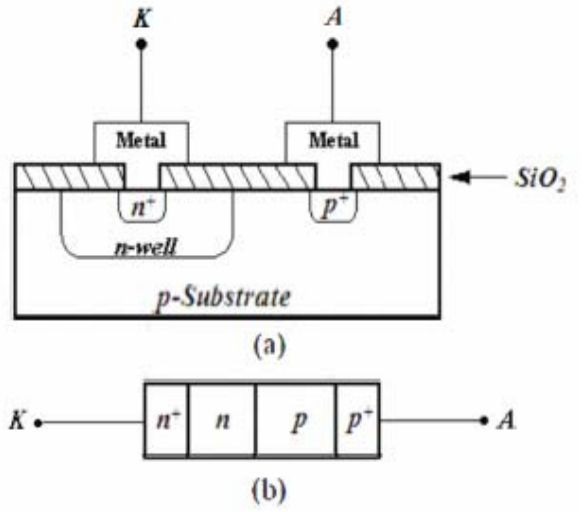

Figure-6. (a) Lateral DDR IMPATT structure, (b) one-dimensional model of DDR IMPATT structure.

Double avalanche region (DAR)

A DAR diode has a p+-n-i-p-n+ structures that consists of one drift zone sandwiched between two avalanche zones (Roy and Mitra, 2003) and it is show in Figure-7. The electrons and holes from the two junctions travel across the central i-region in opposite direction and deliver power. Due to the cancellation of mobile space charge in the central drift region, the DAR has a very little distortion of filed profile in the presence of a large mobile space charge (Roy and Mitra, 2003).

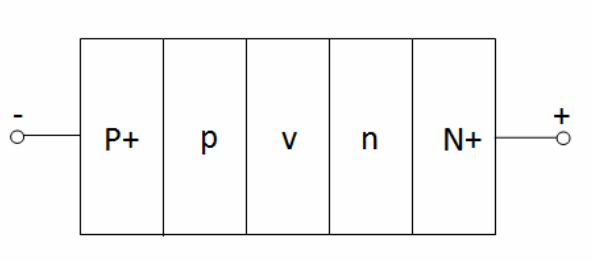

Figure-7. Structure of double avalanche region of IMPATT diode (DAR).

Figure-8 (a) shows the DAR structures which include the two avalanche regions. The charge carriers multiply in the avalanche region and then drift along the drift zone v with the constant speed. These carriers multiply ones again into another avalanche zone (De La Cruz, 200). Those two avalanche regions are located around n+p and np+ junctions and each of them provides the phase delay about π. The electric field distribution can be approximate by the Figure-8 (b). This is sufficiently to produce the negative diode resistance (De La Cruz, 2004).

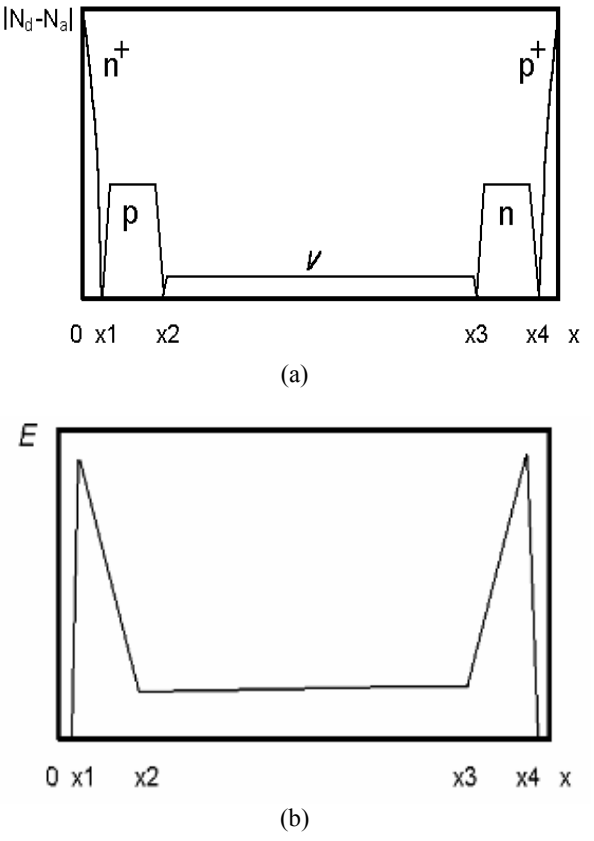

Figure-8. a) Structure of double avalanche region of IMPATT diode (DAR) and b) electric field distribution.

PROPERTIES OF IMPATT DIODE

The frequency of the operation of an IMPATT diode depends on the transit time of charge carriers to cross the depletion region (Deyasi and Swapan, 2011). The operating frequency must consider in designing IMPATTs. The transit time formula shown below is proposed by Sze and Ryder (Deyasi and Swapan, 2011) given by

$$W_{dep} = 0.37\frac{v_s}{f} \quad (1)$$

where Wdep and vs are the total depletion layer width, saturated drift velocity of electrons and design frequency respectively. The transit time frequency in term of junction depth is given by

$$f = \frac{v_s}{2}(W - x_j) \quad (2)$$

where vs = saturated drift electron velocity of Si=107 cm/sec,xj = junction depth and W = length of the n-layer for SDR (Mishra, *et al*., 2011). Several of the previous papers (Chakraborty, 2011) used the realistic value of field, electrons and holes ionization rates, carrier mobility and the saturated drift velocities of electrons and holes in Si for the profiles of electric field from (Mishra *et al*., 2011).

The DC to millimeter-wave conversion efficiency is calculated from semi-empirical formula (Scharfetter and Gummel, 1969).

$$\eta(\%) = \frac{(V_D \times 100)}{(\pi \times V_B)} \quad (3)$$

where VD and VB are voltage drop across the drift region and breakdown voltage, respectively. Also,

$$V_D = V_B - V_A \quad (4)$$

where VA is voltage drop across the avalanche region. This VA occurs in the junction when the electric field is large enough such that the charge multiplication factors become infinite (Chakraborty *et al*., 2011). It is calculated by integrating the spatial electric field over the total depletion region width

$$V_B = \int_{x1}^{x'_1} E(x)dx \quad (5)$$

where boundaries are defined corresponding to the depletion layer widths of the sides (Deyasi *et al*., 2011) For an uniform avalanche region, the maximum voltage that can be applied across a diode is limited by its breakdown voltage is given by (Mitra *et al*., 2011)

$$V_m = E_m W \quad (6)$$

With the maximum field given by

$$I_m = E_m \varepsilon_s v_s A \quad (7)$$

Therefore, the upper limit on the power output is given by (Mitra *et al*., 2011)

$$P_m = V_m I_m = {E_m}^2 \varepsilon_s v_s A \quad (8)$$

OPTIMIZATION TECHNIQUE FOR IMPATTS HIGH PERFORMANCE

Recently, IMPATT diode has attracted interest among the theoretical researchers due to the higher efficiency and output power in microwave range. In obtaining the higher performance, many improvement techniques that has been done year by year.

Mesa, planar and distributed which is vertical oriented structure diodes has been reported (Midford, Lee and Johnston) and found several disadvantages to this type of orientation. This type of orientation has a contact and drift region to be arrange perpendicular to the surface of the substrate (Stabile, *et al*., 1989). Figures 9 and 10 shows the planar and distributed structures, respectively. As a solution to the disadvantages stated in previous paper, a lateral structure has been developed (Stabile, *et al*., 1989). The unique of design is location of the contact and the drift region adjacent to the substrate. The authors have designed the lateral IMPATT with the length of 1500 µm to minimize the thermal resistance between the active region and the backside of the substrate. It is also below the quarter-wavelength limit of 1800 µm to minimize any resonance or phasing problems (Stabile, *et al*., 1989). From the paper, there are several techniques that have been done to solve the problem related to low efficiency of the design which is the high capacitance of the initial capacitance and the current spreading into the substrate. Another contributor to the low efficiency is also related to the fabrication run which the drift region needs to be fully depleted at breakdown to avoid resistance (Stabile, *et al*., 1989).

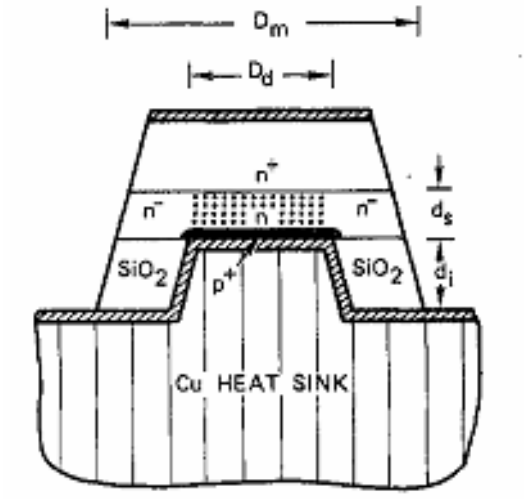

Figure-9. Planar structure IMPATT diode

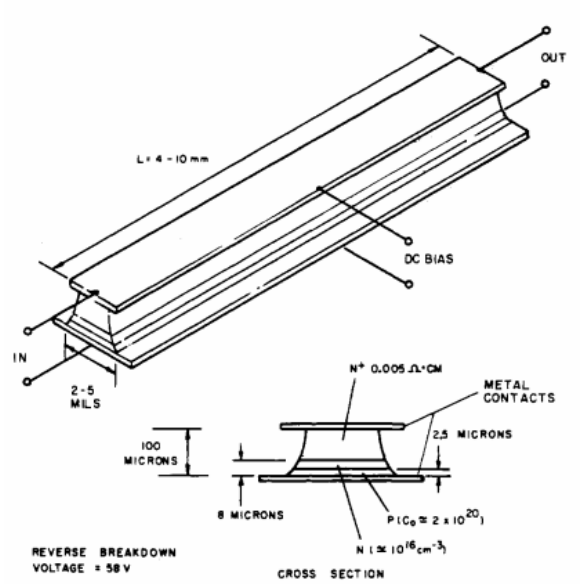

Figure-10. Distributed structure IMPATT diode.

After few years, lateral SDR IMPATT diodes were built as a high frequency power source in Standard CMOS Technology (Al-Attar and Lee, 2005). The unique of the design is consist of n-well, standard source/drain and ohmic contact diffusion region. Similar to the previous paper which this authors use the techniques of reducing the resistance of the inactive region by increasing the diode width while also keeping it below a quarter wavelengths to minimize any resonance or phasing problems (Al-Attar and Lee, 2005). The design structure also needs to reduce the junction area and the junction capacitance to increasing the power efficiency (Al-Attar and Lee, 2005).

Since the SDR IMPATT diode has a low efficiency to the process of input dc power converted into heat, a better heat sinking is needed. So the authors have reported a method of integral heat-sink to solve the problem (Pal and Banerjee, 2010). After e-beam evaporation of CR and Au, the integral heat-sink is formed by electroplating gold to the thickness of 20-30 microns on the p+ side of the structure. To reduce the series resistance, thinning the substrate is the most important step in fabricating the diode. The process can be done by mechanical lapping and chemical etching. Hence, the power and the frequency for the structure could be optimized (Pal and Banerjee, 2010). The optimized fabrication process for realization of SDR IMPATT diode for Ka-band is shown in Figure-11 (Pal and Banerjee, 2010).

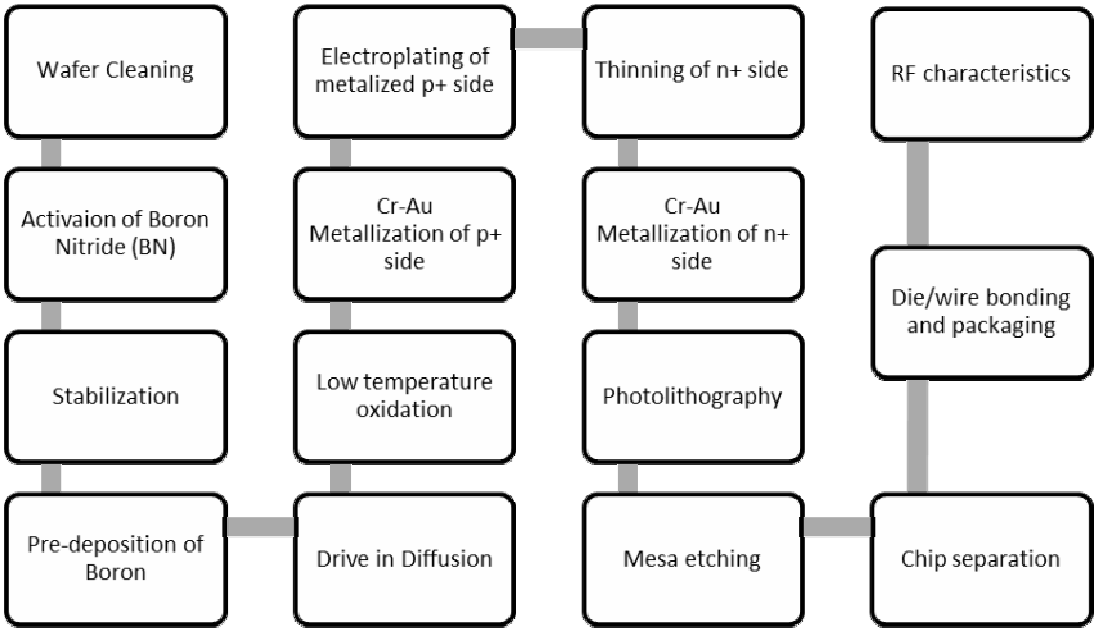

Figure-11. IMPATT diode fabrication process flow.

The junction temperature of Si IMPATT device has been investigated due to the effect of on DC parameters (Deyasi and Swapan, 2011) for optimized the bias current density. The simulation result show that for higher current density, field distorted and perturbation increases with increasing temperature. The electric field becomes less at a specified temperature with increase of current density. The electric field can be increase by increasing junction temperature. The efficiency also may decrease because of higher current density which affects performance of the device (Deyasi and Swapan, 2011).

From previous, it shows that the junction temperature will affect to the parameters of the IMPATT diode. So, each design of IMPATTs has a specific optimum temperature range of operation to achieve a stable and high RF power operation (Mukherjee *et al*., 2011). From the simulation for W-band operation, it has proved that the degradation of RF power output was much more serious beyond 500K. As a precaution, each design of IMPATT diode needs proper heat-sink arrangement to keep the junction temperature at around 500K (Mukherjee *et al*., 2011). Table-2 shows that the peak electric field and the voltage breakdown is increase when the junction temperature increases while the efficiency of the device is found to decrease by 33% (Mukherjee *et al*., 2011). At any temperature, the carrier ionization rates, saturated drift velocities and mobilities of the device can be obtained. Within the lower filed range from $2.4 \times 10^7 - 5.3 \times 10^7 V/m$ (Acharyya and Banerjee, 2012).

$$\alpha_n(\xi, T_j) = 6.2 \times 10^7 \left[exp\left\{ -\frac{(1.08 \times 10^6 + 1.3 \times 10^5 (T_j - 22))}{\xi} \right\} \right]$$

$$\alpha_p(\xi, T_j) = 2.0 \times 10^8 \left[exp\left\{ -\frac{(1.97 \times 10^8 + 1.1 \times 10^6 (T_j - 22))}{\xi} \right\} \right]$$

and within he higher filed range $5.3 \times 10^7 - 7.7 \times 10^7 V/m$,

$$\alpha_n(\xi, T_j) = 5.0 \times 10^5 \left[exp\left\{ -\frac{(9.90 \times 10^7 + 1.3 \times 10^5 (T_j - 22))}{\xi} \right\} \right]$$

$$\alpha_n(\xi, T_j) = 5.6 \times 10^7 \left[exp\left\{ -\frac{(1.32 \times 10^6 + 1.1 \times 10^5 (T_j - 22))}{\xi} \right\} \right]$$

where ξ is the electric field and is the temperature in 0C. The relationship between electron and hole saturated drift velocities with electric field and temperature can be expressed as (Acharyya and Banerjee, 2012)

$$v_{sn} = \frac{1.42 \times 10^7 \times T^{-2.42} \times \xi}{\left(1 + \left(\frac{\xi}{1.01 \times T^{1.55}}\right)^{0.0257 \times T^{0.66}}\right) \times \left(\frac{1}{0.0257 \times T^{0.66}}\right)}$$

$$v_{sp} = \frac{1.31 \times 10^7 \times T^{-2.20} \times \xi}{\left(1 + \left(\frac{\xi}{1.24 \times T^{1.68}}\right)^{0.4600 \times T^{0.17}}\right) \times \left(\frac{1}{0.4600 \times T^{0.17}}\right)}$$

A DDR IMPATT diode is well-known as a better device to produce higher efficiency and RF power. A device has been proposed using standard fabrication of CMOS technology (Acharyya, 2012) which including the n-well process. The device is using the 0.18µm CMOS technology for 94GHz operation frequency. This design structure is improvement from the previous structure which is SDR IMPATT diode (Al-Attar and Lee, 2005) so it could get the higher value of RF power. The same structure is also well suited for optical modulation of RF properties of IMPATT oscillator and optical injection locking (Acharyya, 2012). It has been investigated by a simulation technique which incorporates the dependence of normalized difference of photocurrent density at depletion layer edges (Banerjee and Acharyya, 2012). Figure-12 shows the arrangement for optical illumination on the structure. From the result it shows that the output power of the lateral structure reduces by18.7% and the optimum frequency shifts upwards by 2.48%. By comparing the same condition to the vertical structure, the output power reduces by10.9 and the optimum shifts upwards by 0.75% (Banerjee and Acharyya, 2012).

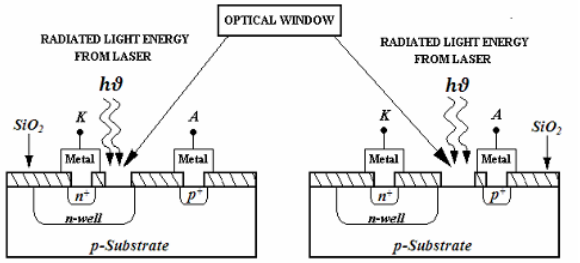

Figure-12. Arrangement for optical illumination on a) n-drift and b) p-drift layers of later DDR IMPATT diode.

A DAR structure which is the optimization structure from DDR gives the possibility to improve the admittance characteristics for higher frequency bands and output power for first and second frequency bands (Alexander Zemliak, 2009). This is because DAR structure has two avalanche regions that can produce an avalanche delay which alone can satisfy conditions necessary to generate microwave power (Alexander Zemliak, 2009).

In overview, series resistance is the main problem that exists in every IMPATT diode and it is difficult to define because it can vary with the doping profile, current density, contact technology used and the chip mounting condition (De and Chakraborty, 2004). In this paper (De and Chakraborty, 2004), the dependence of series resistance on the punch through has been studied due to lower active layer thickness and higher dc current. It found that with increasing of degree of punch through (cause by doping density at lower current density) will increases the value of series resistance and the overall microwave performance. So, the punch through of the depletion layer into the heavily doped substrate needs to be avoided in order to minimize the series resistance and to optimize the microwave performance of IMPATT diode (De and Chakraborty, 2004)

CONCLUSIONS

IMPATT diodes have three basic structures, which has been discussed in previous chapter. Many techniques have been developed which allow in high efficiency and high output power. Those techniques were employed to analyze the properties of the IMPATT diodes either by computer simulation or fabrication. The

development of IMPATT diode also has been reported in higher frequency.

Series resistance is the one of the criteria that should be considered in designing the diode. Furthermore, the doping profiles also must be considered in designing the structure such as depletion region, doping concentration, the thickness of active region and so on.

From the discussion part, the different materials that use as base compound in IMPATT diode give the different result in term of output power, efficiency, reliability, stability and so on. Each of the material has their own reason why it can give the different result. Even though many type of material is used for base material in IMPATTs, silicon still be the mostly used because of the simplicity, low processing cost and easy availability.

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