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LAYOUT DESIGN AND SIMULATION FOR ANALOG NEURAL NETWORK CIRCUIT USING CMOS TECHNOLOGY 0, 35 µM

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ABSTRACT

In this paper, a layout design for analog neural network designed using mentor graphics software based technology will ICFlow 0, 35. By using mentor graphics software ICFlow designing a layout of analog neural network component to a high speed camera and also perform simulations layout. Multiplier designing layouts, Op-amp layout, and Sigmoid layout. To generate the layout design rule check process performed (DRC) and Layout Versus Schematic (LVS). Resulting layout correctly according to the rules of technology.

Keywords: analog neural network, CMOS, layout.

INTRODUCTION

The CMOS circuit design process consists of defining circuit inputs and outputs, hand calculations, circuit simulations, circuit layout, simulations including parasitics, reevaluation of circuit inputs and outputs, fabrication, and testing [4]. In this paper will explain the phase's design and layout simulation. The circuit layout is the phase after the making the circuit and circuit simulation. In addition to following the circuit schematic and simulation results, the making layout should also follow the rules in the design. This rule is also called the Design Rule. Design Rule is a set of rules made by the provider of CMOS technology; the method used for the design rule is DRC. In addition to the making layout design rules also require matching circuit design or layout of the design commonly called the"Matching". Matching is the process of matching and adjustment between circuit designs with design layout. This matching method using LVS. After the DRC and LVS then require layout layout simulation. Simulation layouts aimed trying to test the layout has been created, whether accordance with the schematic circuit simulation.

Therefore in this paper will be designing a layout for the analog neural network. The circuit schematic of an analog neural network has been done by Brahmantyo Heruseto the writing is for the high-speed camera [1]. In the paper it was explain that analog neural network consist of multiplier circuit, OP-AMP circuit and Sigmoid circuit [1]. The goal of this paper in addition layout design also expected can be continuation from design analog neural network who has been done until be a layout already to fabrication. The process to create layout Analog Neural Network using Mentor graphics software version ICFlow 2006.2a and Cmos Technology for 0, 35 µm from AMS (Process C35) with library c35b4c3.

EMBEDDED ANALOG NEURAL NETWORK

Analog neural networks have the following advantages: high speed, low power consumption and compact implementation in comparison with competing digital signal processing approaches [2]. Conception of structures in CMOS technology that demand low power and low siliconarea consumption have been widely investigated in the implementation of analog neural networks in VLSI integrated circuits [1,2]. Hardware implementation of artificial neural networks can be classified into several categories [1]:

1. Neurochips (in the form of digital, analog and mixed signal).
2. Accelerator Boards or additional card that is inserted into the computer (using neurochip or specialized processors such as digital signal processors).
3. Neurocomputer (using neurochip or general purpose processors).

Component of Analog neural network consist of 3 parts that is multiplier circuit, op-amp circuit and sigmoid circuit. The synapses in a neural network can be realized by analog multipliers if the inputs and the weights can be represented by voltages [1] in the previous paper using a multiplier circuit of Barrie Gilbert well known Gilbert multiplier which has been modified. The op-amp circuit is a current voltage converter. The sigmoid is a activation function. Figure-1 shows Analog Network Cell

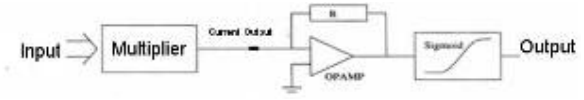

Figure-1. Analog Neural Network Cell [1].

From Figure-1 the input current goes through a multiplier circuit and will then generate output currents. From the results a current output is then passed as an input for the opamp the results of op-amp circuit is a voltage. The voltage resulting from the type of op-amp is a current into a voltage converter. The reason for the output voltage to a able to amplify the current to the desired shape. Then the output of the op-amp circuit will be forwarded become input for sigmoid circuit is used as the activation function. Then the layout can be made follow the design.

MENTOR GRAPHIS ICFLOW AND AMS C35

Many of software for electronic design. one of which is ICFlow of mentor graphics. ICFlow is software for electronic design (schematic and layout). ICFlow can run cross-platform on both linux / unix or windows. However, more and more users use linux version. Until now, the latest version of ICFlow is 2008. In this paper using the 2006 version, but there was no significant difference between 2006 and 2008. ICflow using ”design Architech-ic” for schematic design and ”IC Station” to design the layout.

Many foundries that provide services to design cmos technology. one of which is the AMS (Austria Microsystems). Technology provided a wide variety technologies such as 0, 35 µm. For 0.35 µm there is a wide variety technology such as C35, H35 and S35. The technology is often used C35 for low power consumption.

DESIGN ASPECT

In this paper we are using Mentor Graphics ICFlow 2006.2a and AMS C35 Technology for implementation Analog Neurral Network Circuit. The process of making Analog Neural Network layout consist of three steps, they are:

1. Making / create layout ANN using schematic design (Multiplier, Op-amp and Sigmoid) [1].
2. DRC Layout (Design Rule Check).
3. LVS Layout (Layout versus Schematic).

LAYOUT DESIGN ANALOG NEURAL NETWORK

LAYOUT DESIGN FOR MULTIPLIER CIRCUIT

In this circuit, the multiplier circuit used is a multiplier circuit was created by Barrie Gilbert then modified by Brahmantyo Heruseto. This circuit consist of two input are x and y as input which will multiplied in addition consist of the four input, there input as voltage source drain (VDD), voltage source source(VSS), Ground and Voltage Bias (Vbias). Then output has 1 signal as current. Figure-2 shows as schematic of multiplier circuit with size 44, 25 x 40, and 95 (in µm)

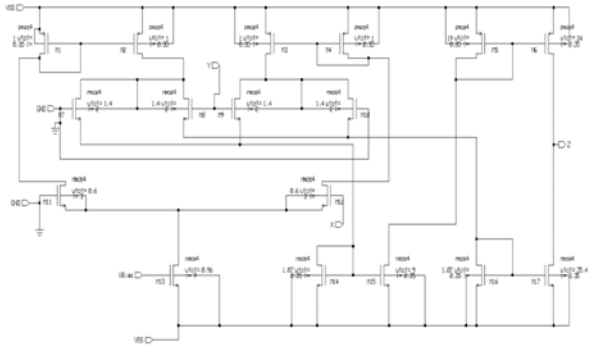

Figure-2. Multiplier schematic [1]

From the circuit consist of 6 Pmos and 11 Nmos, more explained on Table-1. On the schematic multiplier has been designed pmos in one area making it easier to design layout, as well as nmos has been designed also. So by following the circuit layout is generated as shown in Figure-3.

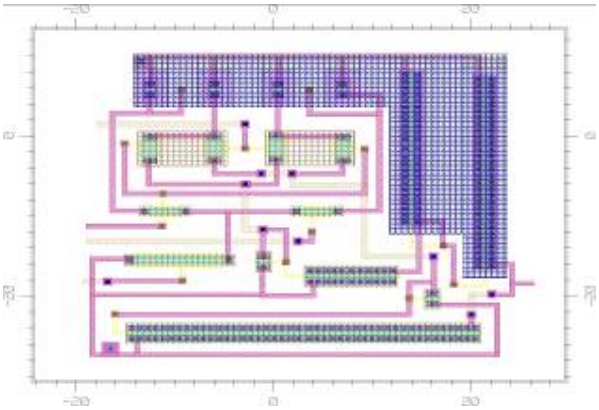

Figure-3. Multiplier layout.

Table-1. W and L transistor value multiplier circuit.

No	Tipe	W (µm)	L (µm)	No	Tipe	W (µm)	L (µm)
M1	Pmos	1	0,35	M10	Nmos	1,4	2
M2	Pmos	1	0,35	M11	Nmos	0,6	3
M3	Pmos	1	0,35	M12	Nmos	0,6	3
M4	Pmos	1	0,35	M13	Nmos	0,96	9
M5	Pmos	19	0,35	M14	Nmos	1,07	0,35
M6	Pmos	24	0,35	M15	Nmos	9	0,35
M7	Nmos	1,4	2	M16	Nmos	1,07	0,35
M8	Nmos	1,4	2	M17	Nmos	35,4	0,35
M9	Nmos	1,4	2				

LAYOUT DESIGN FOR OP-AMP CIRCUIT

In this circuit, the op-amp circuit is used op-amp current into a voltage converter. This circuit consist of one input which the output from multiplier in addition consist of the three input, there input as voltage source drain (VDD), voltage source source (VSS) and Ground. Then output has one signal as voltage. Figure-4 shows as schematic of opamp circuit.

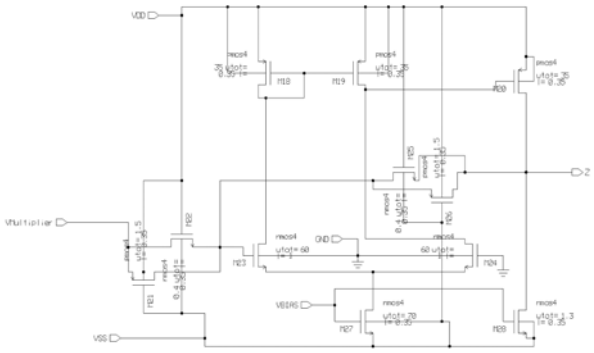

Figure-4. Op-amp schematic [1].

From the schematic circuit consist of 5 Pmos and 6 Nmos, more explained on Table-2. Figure-5 shows as Layout of opamp circuit with size 80, 45 x 67 (in µm).

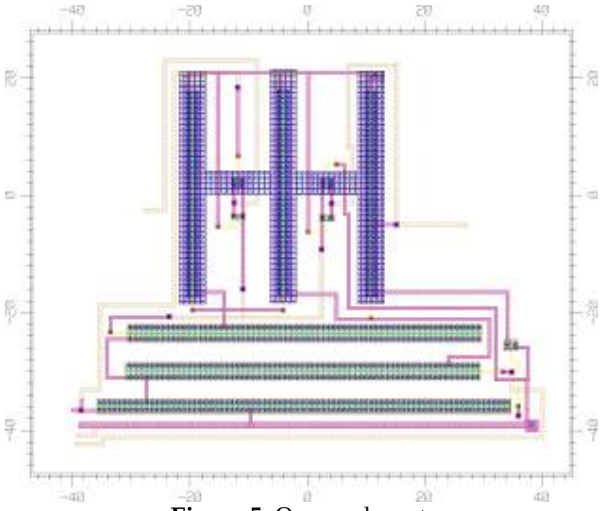

Figure-5. Op-amp layout.

Table-2. W and L transistor value op-amp circuit

No	Tipe	W (µm)	L (µm)	No	Tipe	W (µm)	L (µm)
M18	Pmos	35	0,35	M24	Nmos	60	2
M19	Pmos	35	0,35	M25	Nmos	0,4	3
M20	Pmos	35	0,35	M26	Pmos	1,5	3
M21	Pmos	1,5	0,35	M27	Nmos	70	9
M22	Nmos	0,4	0,35	M28	Nmos	1,3	0,35
M23	Nmos	60	1				

LAYOUT DESIGN FOR SIGMOID CIRCUIT

In this circuit, the sigmoid circuit is used consist of one input which the output from op-amp. in addition consist of the one input as voltage in addition consist of the four input, there input as voltage source drain(VDD), voltage source source(VSS), Ground and Voltage Bias (Vbias). Then output has one signal. Figure-6 shows as schematic of sigmoid circuit.

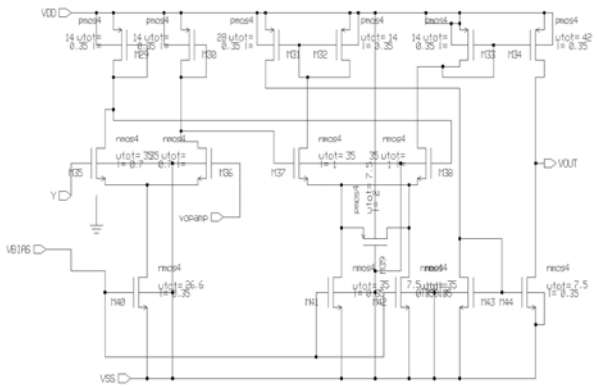

Figure-6. Sigmoid schematic [1].

From the schematic circuit consist of 6 Pmos and 10 Nmos, more explained on Table-3. Figure-7 shows as Layout of sigmoid circuit with size 88 x 91 (in µm).

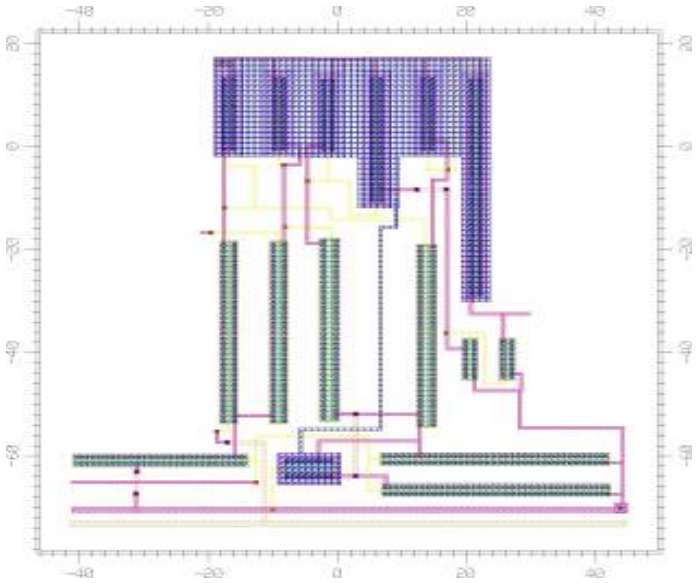

Figure-7. Sigmoid layout.

Table-3. W and L transistor value sigmoid circuit

No	Tipe	W (µm)	L (µm)	No	Tipe	W (µm)	L (µm)
M29	Pmos	14	0,35	M37	Nmos	35	1
M30	Pmos	14	0,35	M38	Nmos	35	1
M31	Pmos	28	0,35	M39	Nmos	7,5	2
M32	Pmos	14	0,35	M40	Nmos	26,6	0,35
M33	Pmos	14	0,35	M41	Nmos	35	0,35
M34	Pmos	42	0,35	M42	Nmos	35	0,35
M35	Nmos	35	0,7	M43	Nmos	7,5	0,35
M36	Nmos	35	0,7	M44	Nmos	7,5	0,35

DESIGN RULE CHECK

Design rule checking is a physical check of the layout or design layouts based on the rule-checking technology used. Layout good according to the rules is a layout that does not have errors. But if there is a warning can be ignored. Which is a lot more mistakes in geometry conditions (such as distance, size, and connection) Metal and Transistors. With using rules C35 for c35b4c3 then the result from DRC process is shown as Figure-8.

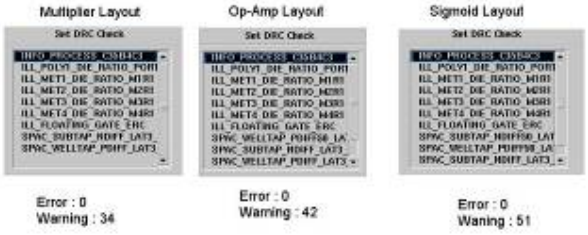

Figure-8. Design rule check result.

From Figure-8 shows that each layout has no errors (geometry) but still have the warning, but the warning can be ignored because it is not a errors.

LAYOUT VERSUS SCHEMATIC

LVS functions as a way to compare the structure (size transistors, transistor type, transistors, the number of transistors and connection lines), with a schematic circuit between layout has been made. For each layout lvs produces conditions as in Figure-9.

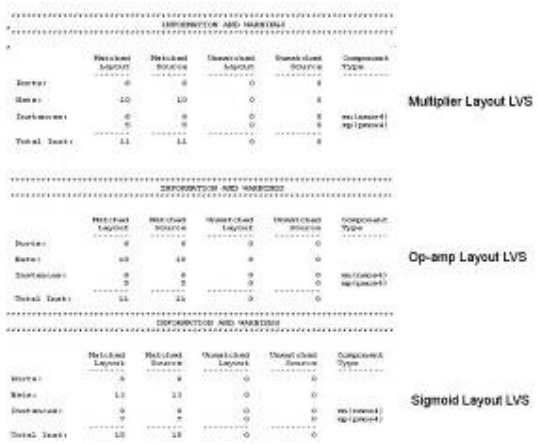

Figure-9. Layout versus schematic result.

Figure-9 shows that each layout has the same value with schematic circuit and has matched then the result all layout has been match with schematic circuit.

SIMULATION RESULT

After each layout has been created, the next step is to perform a simulation on each layout. This simulation aims to test the layout with the schematic simulation by using the file .cir of layout to obtain the same or close to the characteristics of schematic simulation [5]. The following are the results of the simulation of each layout.

MULTIPLIER LAYOUT SIMULATION RESULT

Figure-10 shows multiplier layout in symbol schematic and Figure-11 shows the simulation results of the multiplier layout. Worth the weight values -2, -1, 0, 1, 2 volts with the voltage value at the sweep with a range of -2 Volts to +2 Volts.

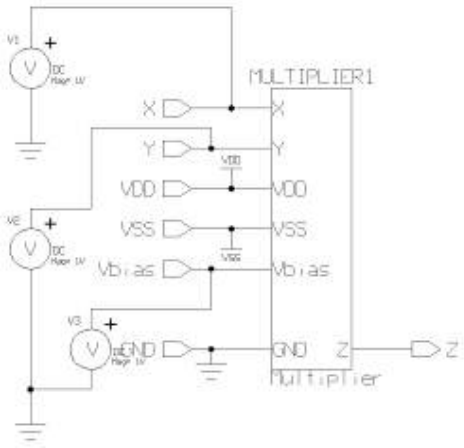

Figure-10. Multiplier layout in symbol schematic.

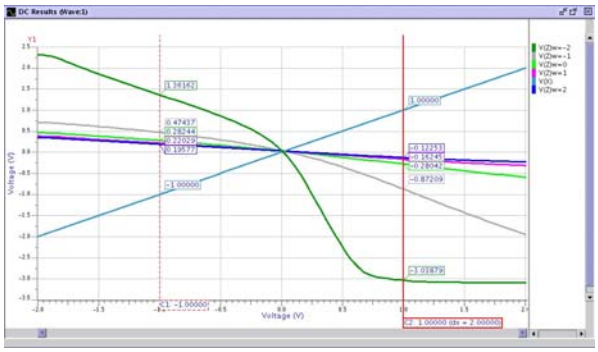

Figure-11. Multiplier layout simulation result.

From Figure-11, multiplier layout generates a graphical form approaching the characteristics of schematic simulation results that have been done on previous research Analog neural network. This happens because the value set for the simulation is slightly different.

OP-AMP LAYOUT SIMULATION RESULT

Figure-12 shows op-amp layout in symbol schematic and Figure-13 shows the simulation results of the op-amp layout.

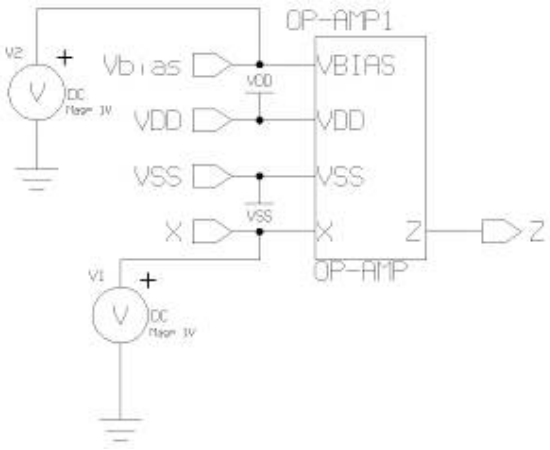

Figure-12. Op-amp layout in symbol schematic.

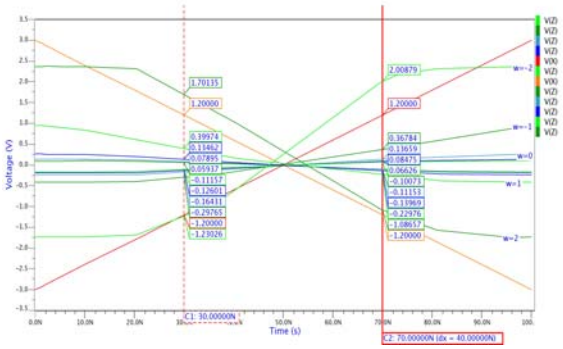

Figure-13. Op-amp layout simulation result.

From Figure-13, multiplier layout generates a graphical form approaching the characteristics of schematic simulation results. The simulation using the weights -2,-1, 0, 1, 2 and insert the voltage set at -3 volts to 3 volts and 3 volts to -3 Volt.

SIGMOID LAYOUT SIMULATION RESULT

Figure-14 shows sigmoid layout in symbol schematic and Figure-15 shows the simulation results of the sigmoid layout. The sweep voltage values between -2 volts to 2 volts.

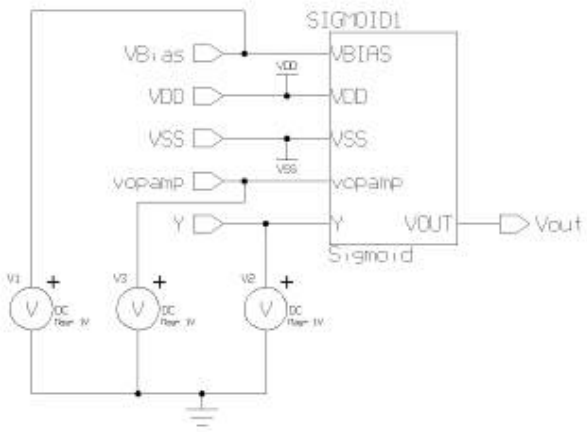

Figure-14. Sigmoid layout in symbol schematic.

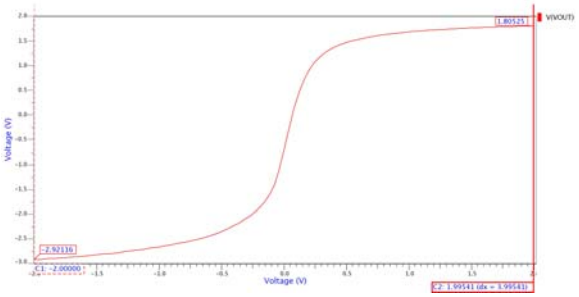

Figure-14. Sigmoid layout simulation result.

From Figure-15, the results showed values between -2 up to 2 is a good value

CONLUSIONS

This paper presented a layout for shape desiain Analog Neural Netwrok with 0, 35 µm technology. Also the continuation and the realization in the form of layout design and implementation of analog neural network for high speed camera to fabrication preparation has been proposed.

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