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EFFICIENT DRIVER DESIGN FOR AMOLED DISPLAYS

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ABSTRACT

The conventional A current feedback driver with double zeros compensation is proposed for medium to large AMOLED displays. The zeros for lead compensation are implemented with switched-capacitor circuits to reduce chip area. The selection rules for compensation Capacitors and zero capacitors are described to obtain wide bandwidth and high speed. The proposed driver has a settling time of 7us for the panel load of 10k/100pF. This work uses high gain and low gain differential amplifiers to provide constant current through pixel and also make sure that voltage induced in capacitor will keep transistor in saturation to make further operation in emission period. Capacitors used for this feedback loop will provide high speed and high bandwidth. Two phases of operation is done to make current through pixel is constant. The feedback system can be analyzed to check performance by parameters like gain margin and phase margin. This current feedback system gain margin and phase margin can be calculated by keeping Data current initially zero and testing output using test voltage. OTRA, high slew rate TRA are used to improve GM, PM with current feedback. In this paper all feedback techniques are compared by checking their performances based on gain margin and phase margin.

Keywords: AMOLED displays, double zeros, fast feedback current driver, OTRA feedback driver, lead compensator, slew rate.

INTRODUCTION

DZ-DFFC Driver is proposed for high speed AMOLED Displays to drive pixels at high speed and clarity. In this Driver Current feedback mechanism makes current flow through pixel exact value equal to the current provided to the driver. DZ-DFFC driver is little modification to DFFC driver by adding two Zeros to improve Bandwidth and Speed.

DFFC Driver will contain compensation mechanism by adding capacitor to compensate the problem with data driven speed of different data currents. Then this compensation capacitor's large area occupation problem can be compensated by Zero added in left half of S-Plane. This resistor large area occupation problem can be avoided by using switching capacitor model instead of resistors.

Operational Trans Resistance Amplifier with current feed-back driver can drive pixels effectively with high bandwidth and phase margin. High slew rate Trans Resistance amplifier can also this job effectively to drive pixel.

AMOLED Display consists of pixels connected in MATRIX form. All these pixels are driven by different drivers connected at back side of the display. All the pixels should be driven at same speed irrespective of data current provided to it. Drivers should do iterations so many times to make current

Active -matrix

An AMOLED display consists of an active matrix of OLED pixels that generate light (luminescence) upon electrical activation that have been deposited or integrated onto a thin-film-transistor (TFT) array, which functions as a series of switches to control the current flowing to each individual pixel. Typically, this continuous current flow is controlled by at least two TFTs at each pixel (to trigger the luminescence), with one TFT

to start and stop the charging of a storage capacitor and the second to provide a voltage source at the level needed to create a constant current to the pixel, thereby eliminating the need for the very high currents required for passive-matrix OLED operation.

Pixel design

Pixel clarity basically depends on current through pixel. So pixel architectures will helps to improve the luminance of Display panel.

a. Source coupled type pixel

Current through pixel cannot be controlled. Scan signal will on the two transistors in scan period and in emission period two transistors are off and no connection between driver and cell.

b. Inverted type pixel

In this pixel current can be controlled by charge stored in capacitor.
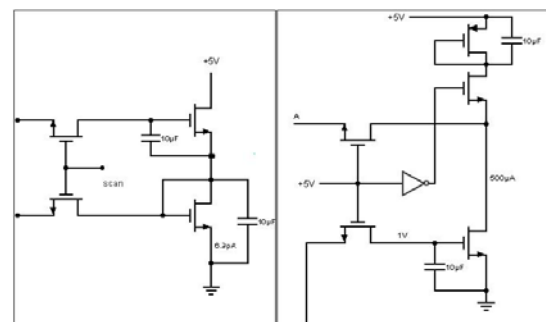
Figure-1. Source coupled and inverted type pixels.

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Current feedback system

Feed-forward methods using the parasitic capacitance of the adjacent data line improve the driving speed in current driving. However, at the beginning of the driving, a pre-charging period is additionally required to equalize the quantity of charges between two data lines. The amount of charge in the parasitic capacitance of one data line is supplied to the parasitic capacitance of the other data line. For large panels, massive parasitic capacitance brings forth a large time constant. As a result, the pre-charging operation requires a long settling time, and programming time of the data current at a predetermined row time should be reduced. Total operation is performed in two phases. First phase is programming phase in which feedback system performs infinite number of iterations and will make sure that current flowing through it is equal to the pixel current. then in second phase driver system and pixel will be separated so that constant amount of data current will flow through pixel for ever.

DESIGN AND ANALYSIS OF PIXEL DRIVERS

DFFC Driver should be designed for large size, high clarity and luminance display panels. Pixel clarity can be improved by transferring constant current (Ipixel) through it. So driver should be designed for that application.

Current mirror driver circuit

We can use current mirror circuit instead of driver circuit. But pixel clarity is not high. Because current through pixel is not constant for given data current (Idata). Due to variations in input resistance of current mirror circuit for different input currents data driven speed will be varied. So different pixels will be driven at different speeds so panel resolution will be less and also causes mismatch errors.

DFFC driver

A DFFC Driver should be designed for large size, high clarity and luminance display panels. Pixel clarity can be improved by transferring constant current (Ipixel) through it. So driver should be designed for that application. DFFC driver consists of feedback loop which is formed by following modules.

The pixel circuit has an inverted type structure in which current flow should be equals to the Data current provided to driver by sensing current in pixel using current follower. The output current of the digital-to-analog converter (DAC) Idata by the digital code D0-D7 is directly compared with IPIXEL through the current follower. The proposed DFFC driver uses an inverting amplifier to make a negative feedback loop between the driver and the pixel circuit. During the programming period (SCAN = High), the DFFC driver and pixel form a feedback loop and make sure both current are equal means error current is zero when the OLED is off.

In this Driver following systems are connected so as to make current feedback to drive pixel at high rate.

a) Current follower
b) Loop compensator.
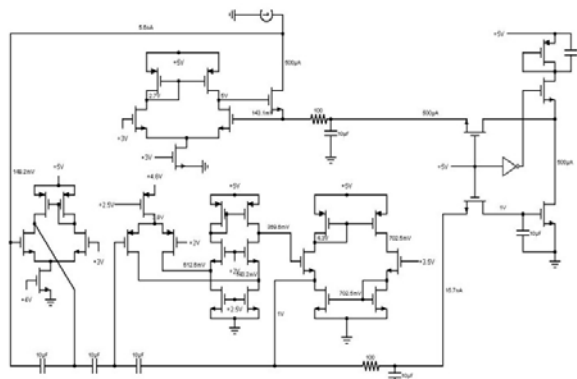c) Error amplifier.
d) Inverting amplifier

Figure-2. DFFC drivers.

DZ-DFFC Driver

Compensation with double zeros

The effect of inserted zeros in the DZ-DFFC driver according to compensation methods when the parasitic line loads between the driver and pixel are 10k/100pF. The AC responses describe the gain and phase of the feedback loop, respectively. When the feedback loop uses only dominant pole compensation, PM of 70.

In this driver first zero is added by placing resistor on loop compensator capacitor and second zero is added by placing another resistor to the capacitor on integrator. Here zero can be adjusted by changing the value of resistor. So large size resistor can be avoided by switching capacitor which has same properties by adjusting the phase of clock signals provided to it. The loop compensator design should be varied according to the data current provided to the current feedback system. For that capacitance should be varied according to the data current.

Double zeros compensation technique used in this system provide high PM, more BW and high speed.
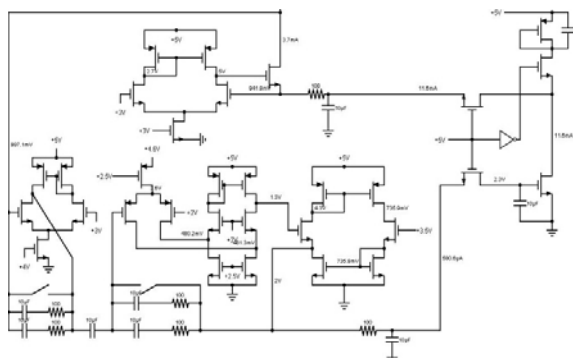

Figure-3. DZ-DFFC driver schematic.

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Current feedback diver using OTRA

In this following driver circuit Operational Transeresistance Amplifier as a driver which drives the pixel. Here OTRA is a class-A cascode current mirror with feedback amplifier to the input stage is less so second stage of current mirror circuit is added to improve slew rate. Output stage consists of source follower is used as voltage shifter to bias outer stage transistors to go into deep saturation for higher transresistance.
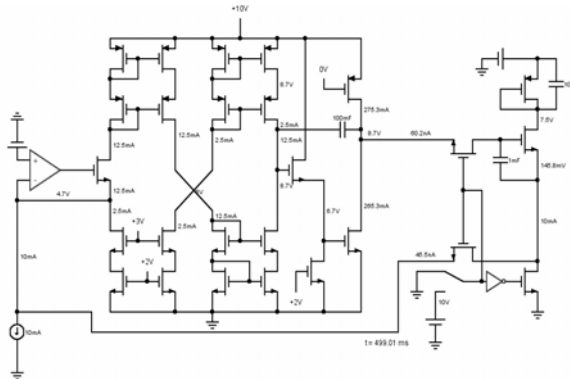
Figure-4. OTRA current feedback driver.

High slew rate Transresiatance amplifier

For the shunt-feedback TIA amplifier, a large feedback resistor is used in order to minimize its contribution to the input referred noise current achieving a good noise performance.
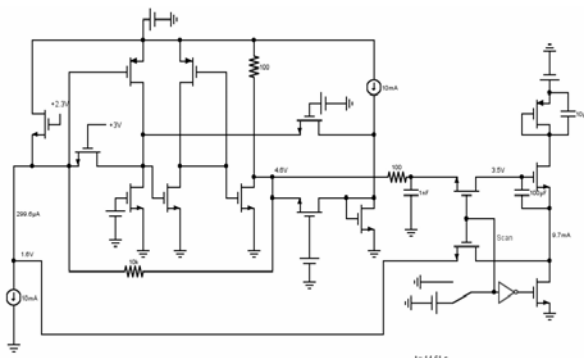
Figure-5. Current feedback driver Transresiatance amplifier.

RESULT AND DISCUSSIONS

Simulation results of DFFC driver

DFFC Driver has four modules connected so as to form negative feedback loop. Here all modules of amplifiers A1, A2, A3 should work properly to get error current minimum.

Driver Amplifiers A1, A3 (One-stage operational transconductance amplifier)
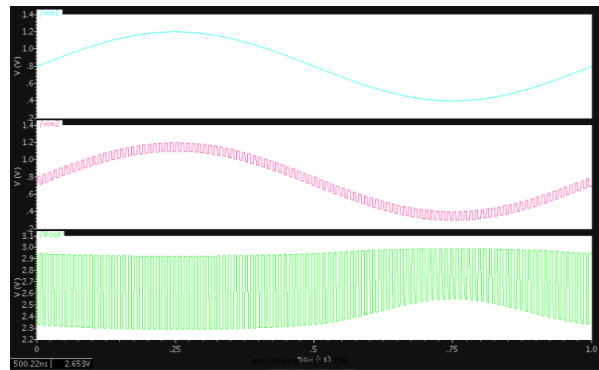Bias Voltage 3V:

For One-stage operational transconductance amplifier all the transistors should in saturation. So bias voltage applied to amplifier should be such that bottom transistor will acts like a current source. If current flow through it is maximum greater than sum of input transistors currents then system will not acts as amplifier.
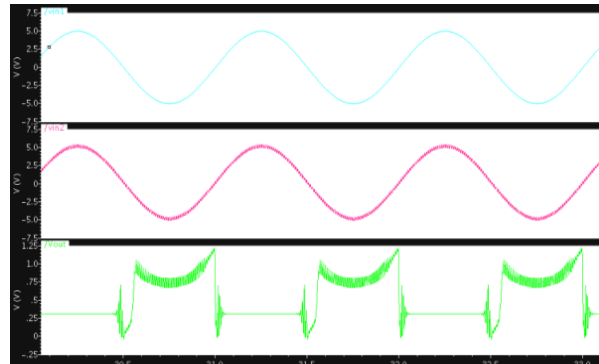
Figure-6. OTC amplifier output for bias voltage=3V.

In this one-stage operational transconductance amplifier bottom transistor will bring other input transistors out of saturation.

Bias voltage applied is maximum so maximum current flown through bottom transistor so it failed to operate as an amplified. Here as a differential amplifier differential signal is not amplified. Bias voltage applied is not maximum so summing current only flown through bottom transistor so it is operated as an amplified. So as a differential amplifier differential signal is amplified.
Bias Voltage 1.4V:

**Figure-7.** OTC Amplifier output for bias voltage=1.4V.

Driver amplifiers A2 (push pull amplifier)

In this amplifier all transistors should be in saturation so as to give differential output. Push pull amplifier first stage should have same currents when same inputs applied and current difference according to the differential input applied.

Here first waveform is generated when bias voltage maximum and second waveform when bias voltages is reduced. So distorted output containing

common signal along with differential input. Here Push Pull amplifier amplified only differential signal. So the from output amplified differential signal at biased level is observed.
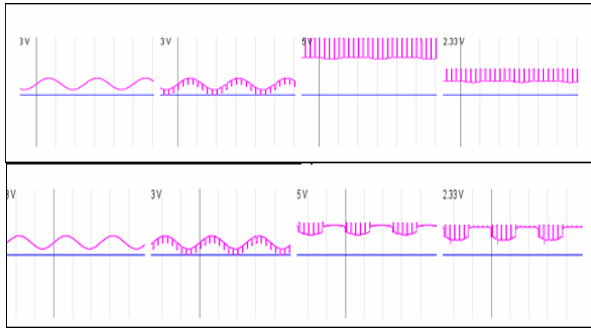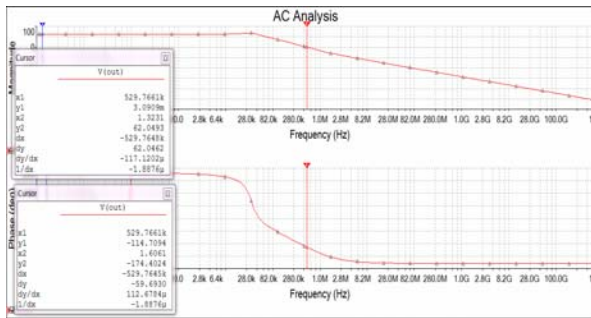

Figure-8. waveform for Class-AB Push pull amplifier for different bias values.

Simulation result of AC analysis of DFFC driver loop

DFFC Driver is design for driving AMOLED Pixel. Before using this driver this driver stability has to be calculated.

So AC analysis is done for feedback loop of driver using test voltage.

Figure-9. Bode plot for feedback driver with basic compensation model.

Feedback loop analysis can be done based on parameters phase margin and gain margin. With phase margin System stability can be decided.

Phase Margin = 180-(gain cross over point)
= 180-114= 66.

Here PM and GM are constant so this feedback system is stable.

### Simulation result of DZ-DFFC driver

DZ-DFFC Driver is design for driving AMOLED Pixel. Before using this driver this driver stability has to be calculated when both cases of adding zeros to the system. So AC analysis is done for feedback loop of driver using test voltage.

AC analysis when first zero is added to the system

By adding positive zero negative zero is cancelled so phase margin is improved. So that stability also improved.

Here expected phase margin for this open loop system with double zeros is increased by 8. So stability of system also improved with compared to previous system.
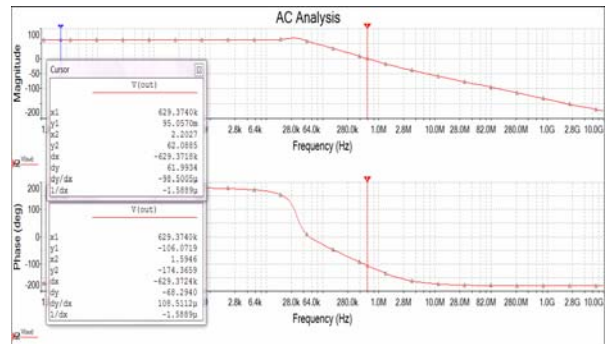
Figure-10. Bode plot for feedback driver with one extra zero added in the system.

Phase Margin = 180-(gain cross over point)
= 180-106 = 74.

AC analysis when first and second zeros are added to the system

By adding positive zero negative zero is cancelled so phase margin is improved. So that stability also improved. Here expected phase margin for this open loop system with double zeros is increased by 15. So stability of system also improved with compared to previous system.
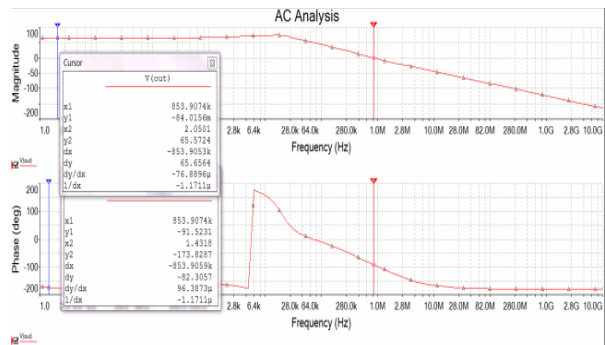

Figure-11. Bode plot for feedback driver with two extra zeros added in the system.

Phase Margin = 180-(gain cross over point)
= 180-91 = 89.

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Simulation results of OTRA driver

Gain response

Operational trans resistance amplifier should be designed with high gain, low input and output resistance. So input current change will not affects the stability.

Phase Margin of OTRA feedback driver = 180-(GP)
                                = 180-80=100.

Here from above plot GM and PM are positive so system is stable. Phase margin is improved with compared to previous drivers.
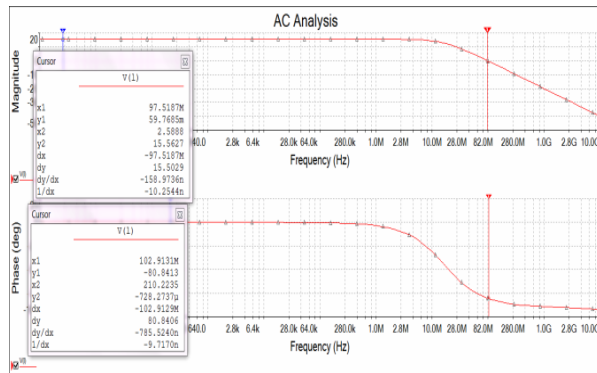

Figure-12. Bode plot for OTRA feedback driver.

Simulation current values of each driver with different settling time
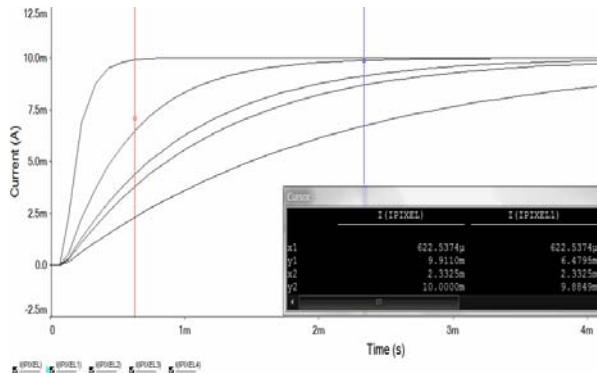

Figure-13. Simulation current values of each driver with different settling time.

Settling time is depends on driver stability. Here from above Figure settling time of DFFC Driver is reduced by DZ-DFFC Driver by increasing stability and data driven speed.

COMPARISONS

Comparison of different driver stability by using phase margin parameter

Table-1. Comparison of different driver by phase margin parameter.

Drivers	DFFC	DZ-DFFC	OTRA	STRA
PM	66	89	100	85

Comparison of normal driver input resistance variation with variations of Idata

Table-2. Comparison of normal driver input resistance.

Data current (Driver input current)	Driver input resistance
5mA	1k
10mA	0.5K
20mA	0.25k
1A	0.005k

variation with variations of Idata

Comparison of potential difference for different supply voltages of pixel

Table-3. Comparison of potential difference for different supply voltages of pixel.

Supply current	0mA	1mA	5mA	7mA	10mA
Potential difference	0V	1.65V	1.78V	1.78V	2.1V

Comparison of settling time for different cases in driver design

Table-4. Comparison of settling time for different cases.

	first zero	2nd zero	zero away from origin
settling time	622 u sec	434 u sec	287 u sec

CONCLUSIONS

Settling times smaller than 0.7 m sec for all the currents as smaller than 12 mA. Limitations of the conventional drivers in terms of driving performance is overcome by different drivers. PM is improved by adding two zeros by value 18. OTRA with high open loop transresistance is used to drive pixel cell with less settling time. Parasitic capacitance of feed-back and data line is reduced by reducing input resistance and output resistance of all drivers for lower the values of data currents below than 10 mA so that compensation circuitry added to compensate these poles easily with less settling time.

REFERENCES

Y.-J. Jeon, J.-Y. Jeon, Y.-S. Son, J. Huh and G.-H. Cho. 2010. A high-speed current-mode data driver with push-

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pull transient current feedforward for full-HD AMOLED displays. IEEE J. Solid-State Circuits. 45(9): 1881-1895.

Y.-S. Son, Y.-J. Jeon, J.-Y. Jeon and G.-H. Cho. 2010. Transient charge feedforward driver for high-speed current mode data driving in active-matrix OLED displays. IEEE Trans. Circuits Syst. I, Reg. Papers. 57(3): 5395-5447.

J.-Y. Jeon, Y.-J. Jeon, Son, K.-C. Lee, H.-M. Lee, K.-H. Cho and G.-H. Lee. 2008. A direct-type fast feedback current driver for medium- to largesize AMOLED displays. In: Proc. IEEE ISSCC Dig. Tech. Papers. pp. 174-604.

S. J. Ashtiani and A. Nathan. 2009. A driving scheme for active-matrix organic light-emitting diode displays based on current feedback. J. Display Technol. 5(7): 257-264.

G.-H. Lee, S.-K. Kim, Y.-S. Son, J.-Y. Jeon, Y.-J. Jeon and G.-H. Cho. 2006. A fast driving circuit for AMOLED displays using current feedback. In: Proc. SID Dig. pp. 363-365.

Kumar A. Nathan and G. E. Jabbour, 2005. Does TFT mobility impact pixel size in AMOLED backplanes? IEEE Trans. lectron Devices. 52(11): 2386-2394.