VOL. 9, NO. 12, DECEMBER 2014 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences


www.arpnjournals.com

A LOW POWER LOW NOISE CMOS AMPLIFIER FOR PORTABLE ECG MONITORING APPLICATION

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ABSTRACT

A low power and low noise front end chopped instrumentation amplifier for portable electrocardiogram recording system is presented. The circuit is based on the chopper technique which is implemented using folded cascode structure that has significant lower power consumption than the predecessor's approaches while keeping the performance unchanged. The chopper switches modulate noise from a low frequency into a higher frequency range, then demodulates back to original signal before filtering the unwanted effect by a low pass filter. The circuit is designed based on SILTERRA 0.18 µm CMOS technology process using VIRTUOSO CADENCE. The simulated results of the amplifier show ultra-low power of 5.51 µW and low noise of 17.2 µV/√Hz at 10 Hz. High differential voltage gain of 54.5 dB and 71 dB in CMRR are achieved.

Keywords: electrocardiogram (ECG); instrumentation amplifier (IA); chopper technique; folded cascode amplifier.

INTRODUCTION

Electrocardiogram (ECG) is extensively used in acquiring vital health information in cardiovascular system. Rapid development in advance technology has led to the realization of portable medical devices for human's health monitoring without restricting their mobility. The trend towards increasingly portable demands low power and reduced size without impacting the recording quality.

Generally, the architecture of instrumentation amplifier (IA) for ECG device includes traditional three operational amplifiers configuration (3OA), current balance IA configuration (CBIA), differential difference amplifier (DDA) and operational transconductance amplifier (OTA). Among this circuit design implementations, OTA approach has benefit in reducing the number of circuit components and consumes lesser power since portable ECG device has tight constraint with power consumption.

Conventionally, the most widely circuit approach for ECG biomedical amplifiers is the three operational amplifier structures. One of its superior advantage is it is able to alter the gain of the amplifier without the need of changing more than one type of resistor. Dobrev then introduced amplifier with bidirectional current sources connected to inputs using negative shunt to shunt feedback. The voltage controlled current sources provide support in controlling the amplifier differential input impedance whereby the polarization potentials' effect is automatically balanced [1]. The downside of the design is it produces low CMRR as the mismatch of the resistance in 3OA will cause CMRR to be degraded. Therefore in order to achieve high CMRR, perfect matching resistance must be obtained.

On the contrary, since ideal matching resistance is not needed in CBIA, high CMRR can be achieved if the transistors of the current mirror are matched perfectly. Nonetheless, the high number of parallel branches of CBIA rises the power dissipation. Yazicioglu proposed the use of coarse-fine servo loop in AC coupled chopper stabilized instrumentation amplifier to reduce the number of parallel branches. However the AC coupled with the use of Gm-C filter limits the output swing [2].

DDA structure is another architecture that can achieve high CMRR without requiring matched resistance. Albeit the present of variations in process parameter it can still produce large CMRR. Yen presented DDA with the new offset cancellation circuitry to improve the equivalent input offset voltage. The major concern of this approach is its poor power consumption. Yen's proposed amplifier consumes high power consumption which is approximately 1525 µW; hence it is not relevant to be implemented in portable system [3].

Thus, three of the mentioned methods are not appropriate for low power and low noise front end instrumentation amplifier design. Last but not least, OTA structure has the advantage over its small chip area whereby it contains lowest total number of transistor. Besides improving the battery life and attaining low power consumption, reduction in total transistor count of the IA also plays a crucial role in enhancing the portability and mobility of the device.

This paper presents a design of low power and low noise chopped stabilized folded cascode instrumentation amplifier using SILTERRA 0.18 µm CMOS technology process. Section II discusses the concept of the selected amplifier and the theory of chopper technique implementation. Section III deals with the detailed explanation on the proposed IA. Results and discussion are described in section IV followed by section V which concludes the overall work.

DESIGN CONCEPT

Amplifier

The folded cascode amplifier topology has been widely used in electroencephalogram (EEG) due to its

upper side characteristics such as low power, low noise, high gain and the ability of providing gain in both DC and AC signals [4, 5]. The previous conventional IA designs in ECG have a disadvantage over the total power consumption owing to the complexity of the circuit. Hence, folded cascode architecture is the perfect IA structure to be chosen for ECG recording front end amplifier seeing that it is a single stage op amp with lowest number of transistors among that traditional design [6].

Chopper technique

Chopper technique is based on a modulation technique where it converts the frequency range of an input signal to the higher frequency range of a chopping frequency, f_c where the dominant noise is a white noise. The bandwidth of the amplifier is approximately ten times larger than the chopping frequency. Thus, in order to chop at high frequencies, a larger amplifier bandwidth compared to chopping frequency is required to decrease $1/f$ noise and to allow the thermal noise unchanged. After the amplification, demodulation is required to demodulate it back to the baseband. The high order low pass filter (LPF) is needed to diminish the demodulated noise within higher frequency range than the chopper frequency and to achieve a low spurious signal [7].

Referring to Figure-1, at V_B, the undesired signal V_n, V_D, which represents sources of noise or distortion, is added to the spectrum. After the second multiplier which refers to the demodulator, the signal is demodulated back to the original one and the undesired signal has been modulated. The spectrum of the undesired signal has been shifted to the odd harmonic frequencies of the chopping square wave. The spectrum of the $v_n + v_D, V_n + V_D(f)$, has been folded back around the chopping frequency. If the chopper frequency is much higher than the signal bandwidth, then the amount of undesired signal in the pass-band of the signal will be greatly reduced. Since the undesired signal will consist of $1/f$ noise and the DC offset of the amplifier, the influence of this source of undesired signal is mixed out of the desired range of operation.

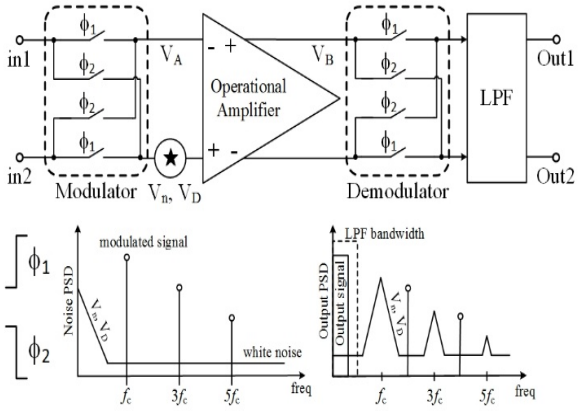

Figure-1. Principle of chopper technique.

PROPOSED CIRCUIT

A MOS folded cascode operational amplifier uses cascoding in the output stage combined with an unusual implementation of the differential amplifier to obtain better input common mode range. The proposed circuit basically consists of common source configuration, common gate configuration, cascaded mirror, constant current source and three sets of chopper. Based on Figure-2, M1 is connected in a common source configuration and M1A is connected in a common gate configuration. Since PMOS has lower flicker noise than NMOS, PMOS has been chosen for the differential input pairs M1 and M2 to reduce the flicker noise of the amplifier. As M11 and M12 act as constant current source, small signal variations in the drain current of M1 and M2 are conducted primarily through M1A and M2A respectively. It is said to be folded as it reverses the direction of the signal flow back towards the current mirror. This reversal has two benefits when differential pair is being applied. One of them is it increases the output swing and so, it increases the common mode input range. The current mirror sends variations in the drain current of M1A to the output where it converts the differential signal into single ended output. Bias is realized by allowing the currents in current sources M11 and M12 larger than $|I_{D5}|/2$. Equation 1 shows the relations between I_{D1A} and I_{D5}.

$$I_{D1A} = I_{D2A} = I_{D11} - (|I_{D5}|/2) = I_{D12} - (|I_{D5}|/2) \quad (1)$$

The small signal voltage gain of folded cascode op amp at low frequencies is

$$A_v = G_m R_o \quad (2)$$

where G_m is the transconductance and R_o is the output resistance (from equation 2). The variation in the drain current of M1 and M2 contribute productively to the transconductance due to the appearance of the current mirror of M3 to M4. Thus, $G_m = g_{m1} = g_{m2}$.

In order to get R_o, both inputs, in1, in2, are connected to AC ground. The sources of M1 and M2 do not operate at AC ground even though the input voltages do not move in this case. The drain current of M1 stays constant when the source of M1 and M2 connecting to AC ground. Besides, as M3 and M3A are diode connected, the Thevenin equivalent resistances at the gates of M4 and M4A are very small. Therefore, the gates of M4 and M4A are assumed to be connected to small signal ground. Thus, the calculation of R_o is shown in equation 3.

$$R_o = (R_{out}|_{M2A}) \parallel (R_{out}|_{M4A}) \quad (3)$$

The first chopper, Ch_1 works as a modulation module whereas the second chopper, Ch_{2a} operates as a demodulation module. The third chopper Ch_{2b} is embedded within the self-biased cascade transistors to up-modulate the errors from transistors M3 and M4. All three chopper modulation modules act as modern switches. The chopper modules are constructed by commutating bridge which consists of 4 transistors each as shown in Figure-3. The unwanted low frequency flicker noise of the front end amplifier is modulated with a high chopping frequency carrier signal and then demodulated back to modulating signal before filter out by the low pass filter (LPF). As the high frequency carrier signal with the residual signal after demodulation still remains, a LPF is needed to eliminate the carrier signal [8]. The cascade transistors are properly biased to sustain operation against variations of process and supply. The single stage high gain folded cascode structure is chosen to achieve lower power consumption with the advantage of using lesser number of transistors compared to the design of [6].

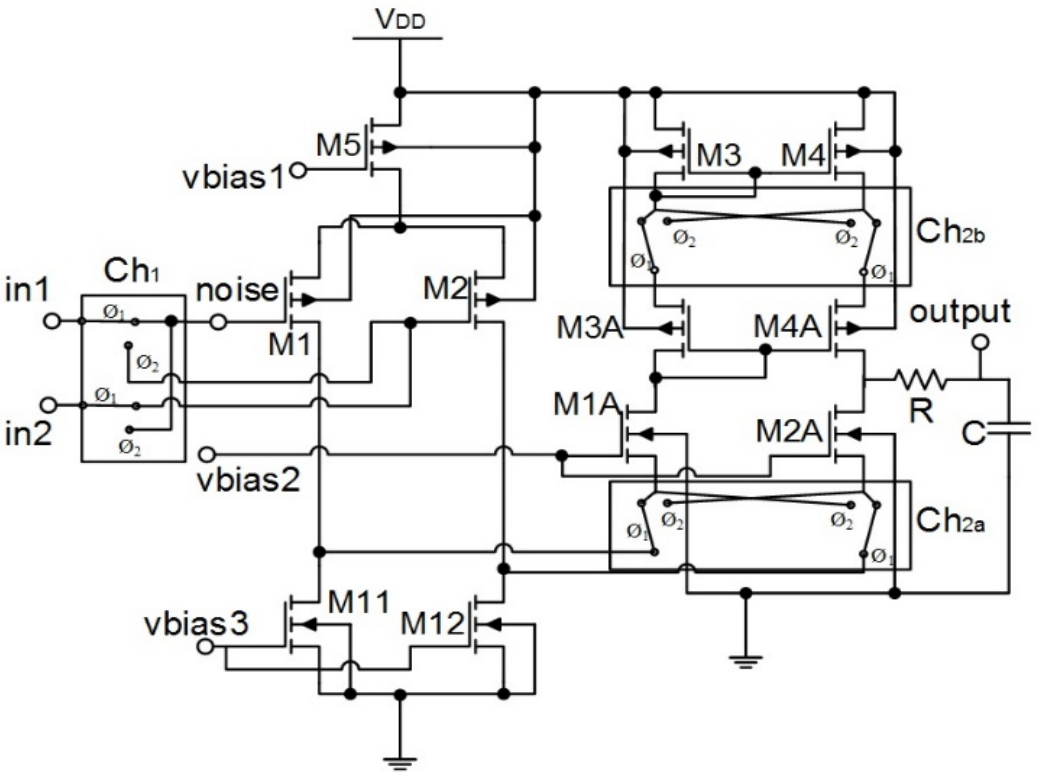

Figure-2. The presented chopper stabilized folded cascode IA.

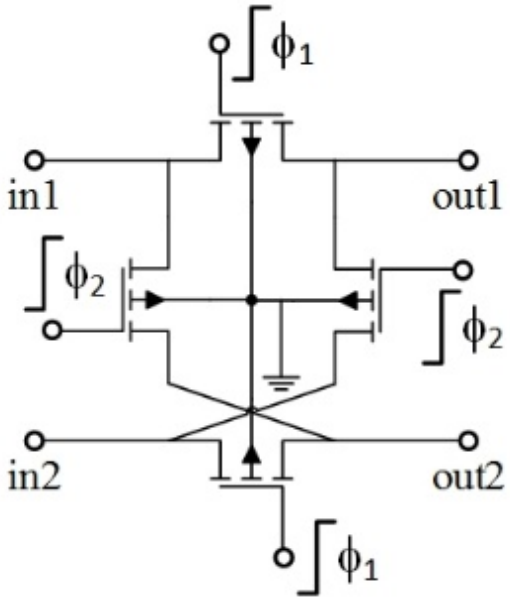

Figure-3. Chopper structure using transistors.

RESULTS AND DISCUSSIONS

The proposed IA is constructed and simulated with SILTERRA 0.18 µm CMOS technology. The supply voltage is 1.8 V, chopping frequency is 20 kHz and the capacitance of the low pass filter is 2 pF. Figure-4 shows the simulated gain of the IA which is approximately 54.5 dB with the limited bandwidth at 200 Hz as the frequency range of the ECG signal is from 0.1 Hz to 200 Hz. Chopping frequency of the circuit can reach as high as 100 kHz as the original gain bandwidth of the IA is around 1 MHz before passing through the low pass filter. The CMRR of the IA is 71 dB indicated in Figure-5 which is the result of differential gain in decibel minus common mode gain in decibel.

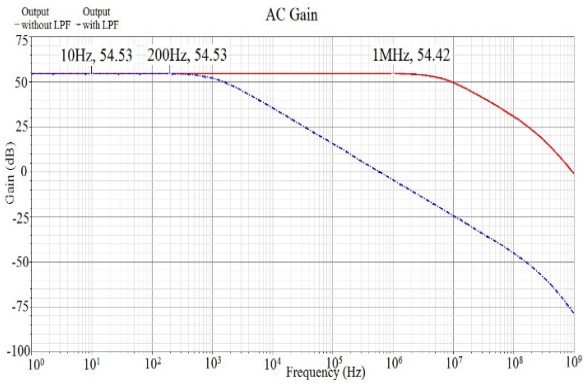

Figure-4. AC gain of the folded cascode IA in decibel.

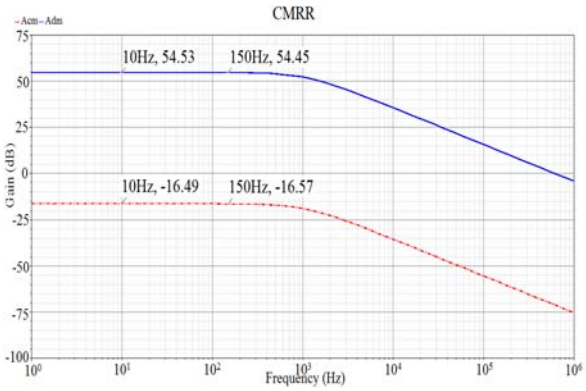

Figure-5. Differential mode gain, Adm and common mode gain, Acm in decibel.

Two simple voltage sources have been generated in the simulation to recognize the process of the chopper technique. In the left electrode, a 10 Hz sinusoidal signal with 1 mV amplitude which represents heartbeat and a 30 Hz sinusoidal signal with 500 µV amplitude which acts as electrode motion artifact are provided, whereas only 30 Hz sinusoidal signal with 500 µV amplitude is given at the right electrode. The third signal of Figure-6 reveals the modulation signal after mixing with the chopper frequency to increase the frequency of the signal together with the flicker noise.

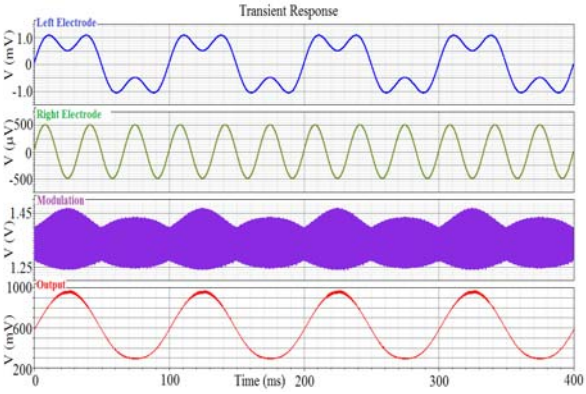

Figure-6. Input and output waveforms with chopper implementation.

A 5 Hz flicker noise with 1 mV is deliberately added to one of the input. The Discrete Fourier Transform (DFT) from Figure-7 proves that the flicker noise gain of the chopper stabilized IA has been decreased. The output signal to noise ratio is S_{output}/N_{output} = 328.800/9.024 = 36.44. Thus, the chopper stabilized technique provides 31.23 dB reductions in the low frequency flicker noise. The magnitude via DFT calculation is collected from a standard sample size of 512 samples from initial 0 s to 200 ms. The reason of setting the DFT calculation until 200 ms is to acquire a period of 5 Hz which is the lowest signal frequency that has been used throughout the simulation

test cases. From Figure-8, the input referred noise is reduced to 17.2 µV/√Hz at 10 Hz with chopper technique. The performance of the proposed low power instrumentation amplifier is compared with several IA architecture approach for ECG recording front end amplifier in Table-1. The result proves that the chopped stabilized folded cascode OTA approach is the best amplifier to be used in portable ECG devices as it consumes the least power consumption without degrading the performance.

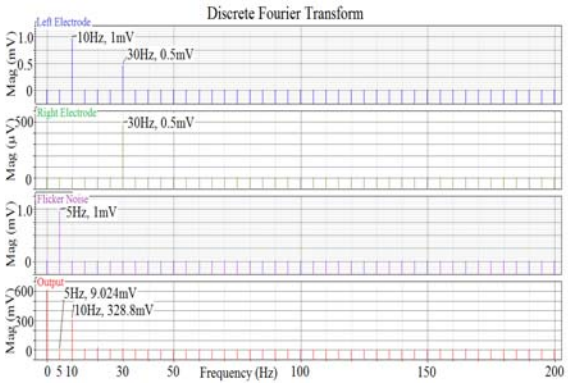

Figure-7. DFT of the input and output signals with chopper implementation.

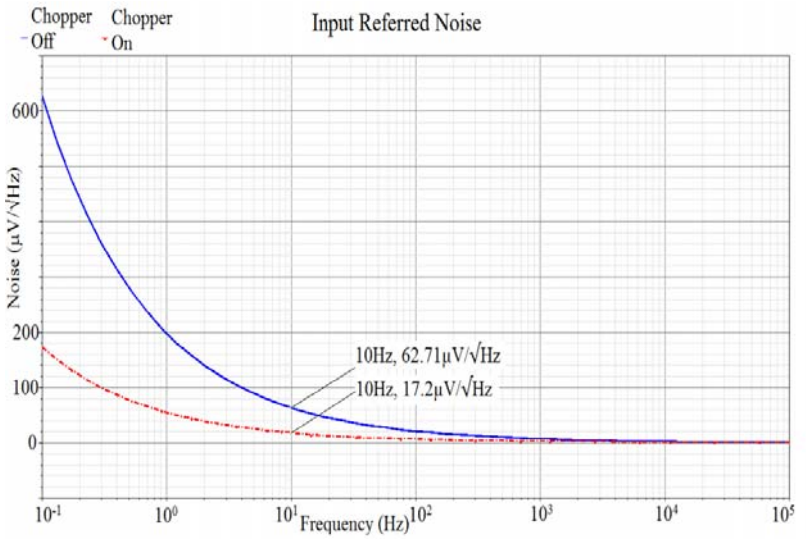

Figure-8. Input referred noise with chopper and without chopper.

Table-1. Comparison of Various ECG Recording Amplifiers.

Parameter	[1]	[2]	[3]	[6]	This work
Approach	3OA	CBIA	DDA	OTA	OTA
Process (µm)	-	0.5	0.5	0.18	0.18
Voltage Supply (V)	3	2	2.5	1	1.8
Current (µA)	150	15.25	61	110	3.06
Power (µW)	450	30	1525	110	5.51
Gain (dB)	46	49.5	19.99	38	54.5
CMRR (dB)	60	105	110	80	71
Input Referred Noise	-	85 nV/√Hz	175 nV/√Hz @20 kHz	1.64 µVrms	17.2 µV/√Hz @10 Hz

CONCLUSIONS

A low noise and low power chopped stabilized instrumentation amplifier for ECG recording applications is demonstrated. The front end amplifier is implemented in SILTERRA 0.18 µm CMOS technology with 1.8 V voltage supply. The complete amplifier consumes 5.51

μW power with 3.06 μA current which has led to the development of portable ECG monitoring system that is more power efficient that its predecessor approaches. Moreover, this approach has advantage in reducing the IC cost due to the lowest total number of transistors being used and may benefit in high volumes of manufacturing.

ACKNOWLEDGEMENT

The authors would like to thank the support of Motorola Solutions Foundation - USM Masters Scholarship Grant and the anonymous reviewers for their insightful comments, which have led to a significantly improved manuscript.

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