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A LOW-POWER DOUBLE BALANCED OSCILLATOR MIXER DESIGN IN 90nm CMOS TECHNOLOGY

Satish Reddy N. and S. Satheesh Kumar
Department of SENSE (VLSI Design), VIT University, Vellore, India
E-Mail: satish.nannuri@gmail.com

ABSTRACT

CMOS Scaling technologies are the main caused for great impact on Analog design. The most severe affect is the reduction in the voltage supply. A double balanced down conversion oscillator mixer using 90 nm CMOS technology is proposed in this work. This oscillator mixer consists of an individual mixer stacked on a voltage-controlled oscillator (VCO). The proposed stacked structure allows entire mixer current to be reused by the VCO cross-coupled pair to reduce the total current consumption of the individual VCO and mixer. Using individual supply voltages and eliminating the tail current source, the stacked topology requires low supply voltage. The DC power consumed by the oscillator is 1.7 mW and mixer is 0.2 mW. The power consumed by discrete structures is high when compared to the proposed stacked structure. At 4.2 GHz a voltage gain of 39 dB and an IIP3 is -12.4 dBm are measured at a supply voltage of 0.9V and with a power consumption of only 1.9 mW.

Keywords: stacked oscillator mixer, self oscillating mixer (SOM), voltage controlled oscillator (VCO), IIP3 point.

INTRODUCTION

The increasing speed and complexity of today's designs implies a significant increase in the power consumption of very-large-scale integration (VLSI) chips. To meet this challenge, researchers have developed many different design techniques to reduce power. One of the key features that led to the success of complementary metal-oxide semiconductor, or CMOS, technology was its intrinsic low-power consumption. This meant that circuit designers and electronic design automation (EDA) tools could afford to concentrate on maximizing circuit performance and minimizing circuit area.

Another interesting feature of CMOS technology is its nice scaling properties, which has permitted a steady decrease in the feature size, allowing for more and more complex systems on a single chip, working at higher clock frequencies. In this market, battery lifetime is a decisive factor for the commercial success of the product. Another fact that became apparent at about the same time was that the increasing integration of more active elements per die area would lead to prohibitively large-energy consumption of an integrated circuit. A high absolute level of power is not only undesirable for economic and environmental reasons, but it also creates the problem of heat dissipation. In order to keep the device working at acceptable temperature levels, excessive heat may require expensive heat removal systems. These factors have contributed to the rise of power as a major design parameter on par with performance and die size. Infact, power consumption is regarded as the limiting factor in the continuing scaling of CMOS technology.

Wireless communication

In radio communications, a radio receiver is an electronic device that receives radio waves and converts the information carried by them to a usable form. It is used with an antenna. The antenna intercepts radio waves (electromagnetic waves) and converts them to tiny alternating currents which are applied to the receiver, and the receiver extracts the desired information.

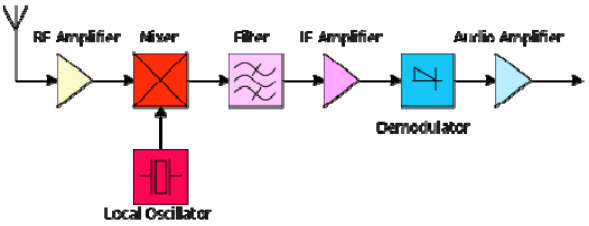

Figure-1. Block diagram of Heterodyne Receiver.

The receiver uses electronic filters to separate the desired radio frequency signal from all the other signals picked up by the antenna, an electronic amplifier to increase the power of the signal for further processing, and finally recovers the desired information through demodulation. The information produced by the receiver may be in the form of sound (an audio signal), images (a video signal) or data (a digital signal). Low voltage, low-power, and highly integrated circuits (ICs) are always the trends for IC design, especially crucial in mobile wireless communication systems due to the limitation of battery capacity. Circuits combining oscillator and mixer using GaAs, BiCMOS, and CMOS processes were designed for the purpose of a high degree of integration and reducing power dissipation. Therefore, an oscillator-mixer design is attractive for highly integrated ICs with low power consumption. This standard commonly requires low cost and low power consumption. To implement low cost chips, direct conversion or low-IF receiver has been widely used because it is essential to increase integration.

$$V_{IF} = A_{RF}[\cos(\omega_{RF}t - \omega_{LO}t)]/\pi = A_{RF}\cos(\omega_{IF}t) \quad (1)$$

Reducing the power consumption is usually realized by two methods: One is lowering the supply voltage and the other is reducing the current. To minimize supply voltage, folded topology is widely used. By dividing current path with low supply voltage and minimizing needless current, the power reduction can be obtained. However, this method may increase chip size because it needs extra inductors. For lowering current consumption, for example, the method to convert cascade circuit to a stacked circuit may be used. The power consumption can be reduced because the current is reused among stacked circuits. However, stacked circuits have potentially linearity problem because it has low voltage headroom.

The mixer or frequency converter is a significant noise contributor in most communication systems. Its function is inherently noisy because noise is transferred from multiple frequency bands to the output. Since the circuit performs frequency translation, it is not linear time-invariant and its noise behavior cannot be analyzed with conventional circuit techniques. This makes the designer almost exclusively dependent on nonlinear noise simulators. Fast estimation of the noise performance is desirable because this capability facilitates design optimization and accelerates the design cycle.

BACKGROUND METHODOLOGY

Self-oscillating mixer design

A self-oscillating mixer (SOM) technique is used to achieve self-oscillation involves merging the mixer and oscillator functions into a single circuit rather than stacking the two circuits upon one another. The merging of the two functions is accomplished by modifying the Gilbert cell mixer to output an LO signal component through an additional port which can be fed back to the LO input port to produce oscillation. The SOM consist a mixer, which performs the task of oscillator without the addition of extra transistors. This merging of functionality is appropriate for any communications system to achieve more compact implementation. By this technique, it is possible to create an LC based PLL with virtually no dedicated VCO transistors. However, this structure operates at a supply voltage of 3.3 V since two NMOS and two resistors are directly stacked. The noise Figure is also limited due to the switching transistor not completely turned on and off.

Double balanced Gilbert cell

Active CMOS mixers, in which a switching pair is used for current-commutation, such as the CMOS Gilbert cell, are commonly used in communication systems. Modern CMOS processes are becoming widely used in the realization of communication circuits because they are capable of achieving high-frequency performance, are inexpensive, and are appropriate for a high level of integration. Active mixers have conversion gain, relaxing the gain requirements of the blocks preceding the mixer and the noise requirements of the blocks following it. In this work, we examine the operation and the noise performance of current-commutating active CMOS mixers, neglecting capacitive effects. The results are applicable when the mixer operates at moderate frequencies used at the intermediate-frequency (IF) stage of a receiver and high bias current, at higher frequencies used at the radio-frequency (RF) front end.

Folded switching mixers

The performance of double-balanced switching mixers is normally sufficient for a majority of applications (typically noise figure (NF) of 10 dB, voltage gain of 10 dB and IIP3 of 1 dBm at power dissipation levels of 6 mW). In the double-balanced switching mixer the transistors in the switching stage are stacked on top of the transistors that comprise the transconductor. Also, the load resistor is placed on top of the switching stage. This way of connecting the transconductor, the switching stage, and the load resistors is conflicting with operation at low supply voltages.

All dc tail current flows through the transconductor, the switching stage and the load resistors. Therefore, at a low voltage supply the voltage drops, across the load resistors, the switching transistors and the transistors in the transconductor become critical. In this particular case it is difficult to keep all the transistors to operate in their saturation region and this causes a significant drop in performance. Hence, it is of interest to find new mixer topologies that can handle successfully low supply voltages. In terms of operation at low supply voltages, the goal is to reduce the voltage drops across the load resistors and the switching transistors. This can be done by designing a switching mixer in which only a part of the dc current from the transconductor flows through the switching stage and the load resistors. In this case the switching stage may be regarded as folded with respect to the transconductor. Therefore, we call this mixer folded-switching mixer.

CIRCUIT DESIGN AND ANALYSIS

VCO and mixer circuits

From Figure-2, Transistor M3 acts as a Current source and M1 and M2 are cross coupled pair. The oscillator produces sinusoidal signal. Two signals are having180^0 phase shift. The oscillating frequency is determined by LC tank circuit. The minimum supply voltage for VCO is

$$V_{vco} = v_{gs1} + (v_{gs3}-v_{th}) \quad (2)$$

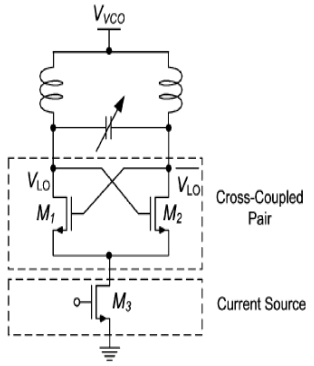

Figure-2. Oscillator schematic.

Figure-2 shows the schematics of a regular down-conversion double-balanced mixer and regular differential VCO [N. Fong *et al*., 2003]. For simplicity in analyzing the minimum supply voltages of the regular mixer, the regular VCO, and this oscillator mixer, the body effect is neglected, all the transistors are assumed identical, and all devices are in the saturation region. The transconductances of the NMOS transistors M5 and M6 are used to convert input RF voltage signals to currents. The NMOS devices (M1-M4) are the time-variant section to mix the RF signals with the LO signals to generate the IF signals.

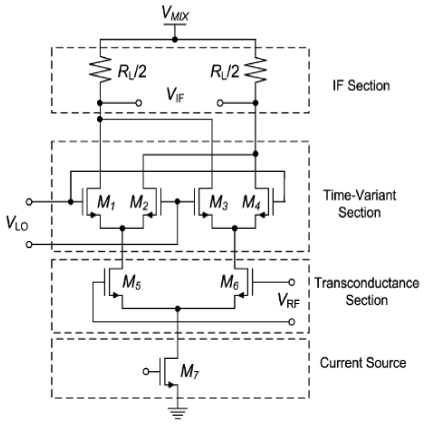

Figure-3. Mixer Schematic.

$$g_m = (\mu_n)(Cox)(W/L)(v_{gs}\text{-}v_{th}) \quad (3) \text{ (since saturation)}$$

There are three levels of active devices (M1, M5 and M7) and a resistor RL/2stack directly, and the minimum supply voltage for the mixer is

$$V_{mix} = (v_{gs7}\text{-}v_{th}) + (v_{gs5}\text{-}v_{th}) + (v_{gs1}\text{-}v_{th}) + V_{RL}/2 \quad (4)$$

Stacked oscillator mixer

In order to reduce these supply voltages (V_{mix} and V_{vco}) and power consumptions, the regular mixer and regular VCO are merged. Figure-3 shows the functional representation for the merged topology. In Figure-3, the VCO core generates the differential voltage signals for the switching function to turn on and off the mixer section (g_1, g_2, g_3, and g_4) by changing their source voltages. The mixer section plays the role to convert the input RF voltage signal to output current, and is switched on and off by the differential-LO signals to produce differential-IF signals.

The schematic of this down-conversion double-balanced oscillator mixer is shown in Figure-4 with each NMOS (M1-M8) of 32 fingers and total gate width of 80 µ. The NMOS (M7-M8) serve as LO buffers for testing purpose. (M1-M4) operating as transconductances (gm1-gm4), the devices (M5-M6) simultaneous serves as the oscillator and switch. NMOS devices (M1-M4) operating in the saturation region are used to increase the conversion gain. In other words,
$V_{DSX} > V_{GSX} - V_{THX}$ for X= 1 to 4.

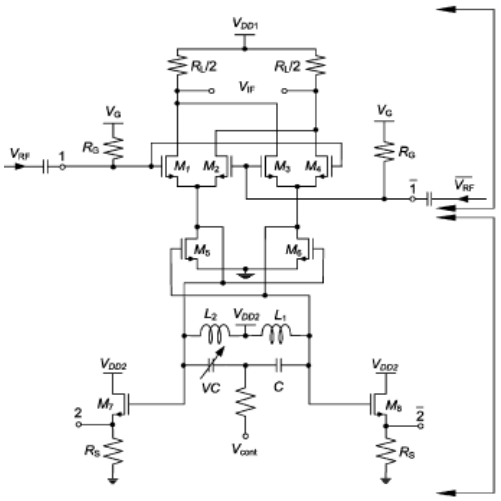

Figure-4. Stacked structure of oscillator mixer.

The differential-LO signals can turn on and off the NMOS (M1-M4) by changing their source voltages. To achieve low supply voltage, the tail current source of the regular mixer topology introduced by Gilbert is avoided. The supply voltages V_{DD1} and V_{DD2} are for the mixer and VCO, respectively. The minimum supply voltage (V_{DD2}) for the VCO is

$$V_{DD2} = V_{GS5} \quad (5)$$

This supply voltage is lower than that of a regular VCO by (V_{GS} - V_{TH}) if the processes are the same. The minimum supply voltage (V_{DD1}) for the mixer is

$$V_{DD1} = V_{GS5} + [(V_{GS1} - V_{TH}) - A_{LO}] + V_{RL/2} \quad (6)$$

Where A_{LO} is the amplitude of the oscillating signal from the cross-coupled pair (M5–M6). However, V_{GS1} is equivalent to A_{LO} for the large oscillating signal. Therefore, which is lower than that of regular mixer (4) by $2(V_{GS}- V_{TH})$ if the $V_{RL/2}$ is same.

$$V_{DD1} = V_{GS5} - V_{TH} + V_{RL/2} \quad (7)$$

Oscillator-mixer conversion-gain analysis

As shown in Figure-5, the differential RF currents are associated with the transconductances (g_{m1}–g_{m4}) and the RF input signal V_{RF} = ½ A_{RF} cos (W_{RF}t). Since is small, the relationship of them can be approximated as

$$I_{RF1}(t) = I_1 + g_{m1} \times [A_{RF} \cos(\omega_{RF} t)] /2 \quad (8)$$

$$I_{RF2}(t) = I_2 + g_{m2} \times [-A_{RF} \cos(\omega_{RF} t)] /2 \quad (9)$$

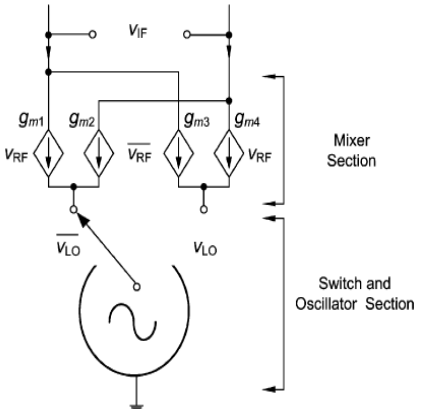

Figure-5. Functional representation of the stacked oscillator mixer.

Where I_1 and I_2 are the bias current of the transconductors (g_{m1} and g_{m2}). After the switching function provided by the VCO, the IF generated from M1and M2 can be written as

$$i_{IF1,2}(t) = g_{m1,2} A_{RF} \cos(\omega_{RF} t) \quad (10)$$

Where $g_{m1,2} = g_{m2} = g_{m1}$, for the same reason, the IF current produced from M3and M4 is

$$i_{IF3,4}(t) = g_{m3,4} A_{RF} \cos(\omega_{RF} t) \quad (11)$$

Due to the differential relation of $g_{m1,2}$ and $g_{m3,4}$ shown in Figure-5, the overall differential IF output voltage is

$$v_{IF}(t) = R_L g_m A_{RF} \cos(\omega_{RF} t) \quad (12)$$

Where $g_{m3,4} = g_{m3} = g_{m4}$.

By neglecting of the body effect and channel length modulation in all devices, the transconductance (g_m) for NMOS (M1-M4) can be expressed as:

$$g_m = \mu_n C_{OX} (w/L) (V_{GS} - V_{TH}) \quad (13)$$

$$= \mu_n C_{OX} (w/L) (V_{GS} - V_{DD2} - V_{TH} + A_{LO}) \quad (14)$$

Where A_{LO} is the amplitude of the oscillating signal. If the sinusoidal oscillating signal has a 50% duty cycle, the voltage conversion gain of the oscillator mixer can be derived as:

$$CG_v = (1/2) \mu_n R_{L/2} C_{OX} (w/L) (V_{GS} - V_{DD2} - V_{TH} + A_L \quad (15)$$

Thus, it can be seen that the voltage gain can be increased by increasing the oscillating amplitude A_{LO} or the loading resistor $R_{L/2}$ or the voltage (V_G- V_{DD2}- V_{TH}) if other parameters are constant [C. G. Tan. 2003]. In (15), the $R_{L/2}$ is approximately 320 ohms for this oscillator mixer cannot be too large since it will reduce the voltage headroom of the mixer. In order to achieve competitive conversion gain at low supply voltage, the supply voltage (V_{DD2}) of the VCO is 550 mV biased at only a little higher than the threshold voltage (500 mV). From the cross-coupled pair (M5-M6) will increase the conversion gain.

Current reuse in oscillator mixer

The dc currents fromV_{DD1} and V_{DD2} are defined as I_{Mixer} and I_{DD2} respectively. With the applied to the drain and gate of the VCO cross-coupled pair (M5-M6), the dc current consumption for the VCO (M5-M6) is defined as I_{VCO}. From simulation, the dc current (I_{Mixer}) from the highest supply voltage (V_{DD1}=900 m V) goes through the mixer (M1-M4), flows only into the cross-coupled pair (M5-M6), and finally sink into ground. The dc current (I_{Mixer}) does not flow into the supply voltage (V_{DD2} =550 mV). This is also verified by experiment. For example, the measured I_{Mixer} is 0.32 m A, I_{DD2} is 2.46 m A, and I_{VCO} is 2.78 m A. Therefore, the dc current I_{VCO} can be written as

$$I_{VCO} = I_{Mixer} + I_{DD2} \quad (16)$$

By increasing the mixer supply voltage (V_{DD1}) with a constant supply voltage (V_{DD2}), the mixer current (I_{Mixer}) from V_{DD1} is increased and the current (I_{DD2}) from V_{DD2} is reduced with the same amount. Moreover, the total currents flow through the VCO devices (I_{VCO}) is constant. In other words, the total current consumption (I_{VCO}) of the oscillator mixer is constant and entire mixer current (I_{Mixer}) can be reused by the VCO cross-coupled pair (M5-M6).

Noise figure calculation

For the regular double-balanced mixer, the thermal noise of the active devices are generated from the time-variant section (M1-M4), transconductance section (M5-M6), and tail current source (M7). The single-sideband (SSB) noise figure can be modified and approximately as at the bottom of the following page, where the transconductance, noise factor, and gate resistance of the transconductance section (M5-M6) are denoted by g_{m5}, γ_5 and r_{g5} respectively. The corresponding properties of the time-variant section (M1-M4) and tail current source (M7) are denoted by $\overline{G}$, γ_1, r_{g5} and g_{m7}, γ_7 and r_{g7} respectively. R_s is the signal-source resistance used for noise-figure evaluation, C represents the conversion gain of the switching pair, and α approaches one for large LO amplitude. During the time interval near zero-crossing of the LO voltage, the MOS (M1-M4) of the time-variant

section will conduct, and there will be a noise current path direct to the IF output port. A significant noise current will occur at the IF frequency during this time interval. For the proposed double-balanced oscillator mixer shown in Figure-4, the thermal noise introduced by the switch and oscillator section (M5-M6) results in a common-mode noise current at the IF output port. The noise current will cancel because of the differential-IF output voltage.

$$(\mathrm{NF})_{\mathrm{SSB,\,OM}} = \frac{\alpha}{c^2} + \frac{2(\gamma_1 + r_{g1} g_{m1})\, g_{m1} \alpha + \frac{1}{R_L}}{c^2 g_{m1}^2 R_S} \qquad (17)$$

RESULTS AND DISCUSSIONS

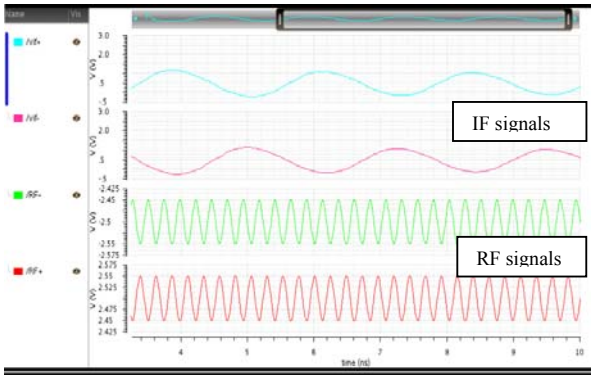

Figure-6. Stacked structure output.

The Figure-6 consists of RF signal whose frequency is 4.2 GHz. RF signal is mixed up with the Local Oscillator output (whose frequency is 4.35GHz) and gives the Intermediate frequency (IF) signal.
4.65 GHz-4.2GHz = 455 MHz.

The amplitude of RF signal is 10 mV and the amplitude of IF signal is 900 mV. The voltage conversion gain is 9. Voltage conversion Gain in dB is 39.

The Figure-7 shows the S-parameters. It express the impedance matching as S_{12} and S_{21} are equal at all frequencies ranging from 1GHz to 5 GHz.

Small signal Power gain is $|S_{22}|$ is 30.5 dB and output return loss $|S_{22}|$ is 12.25 dB.

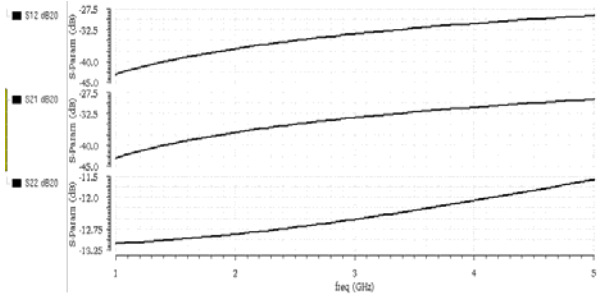

Figure7. S-parameters.

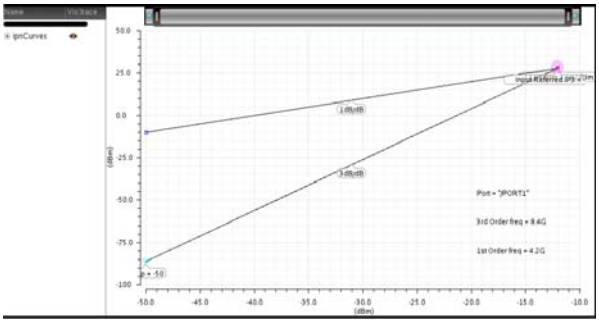

Figure-8. Measured IIP3 at 0.9 V. Figure-8 shows the existing IIP3 point is at -12.6 dBm.

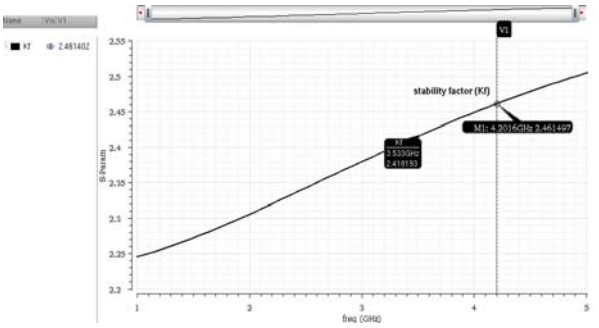

Figure-9. Stability factor (K_f) Figure-9 shows the stability factor. It is around 2.4 at 4.2 GHz.

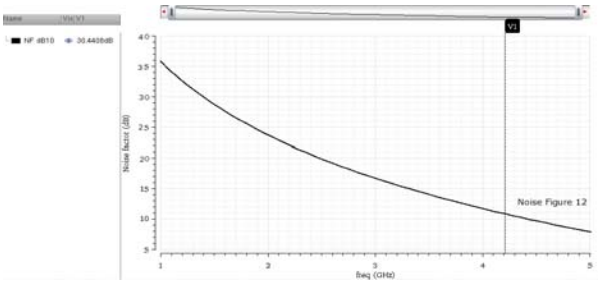

Figure-10. Noise figure Noise figure is about 12dB at 4.2 GHz.

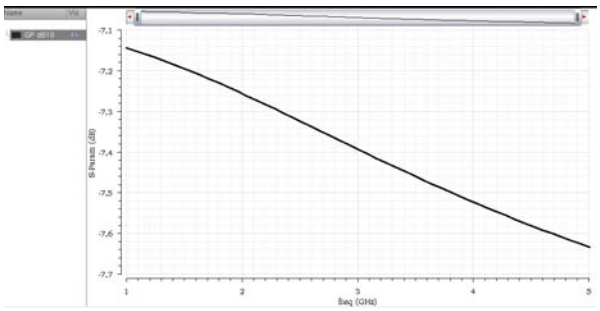

Figure-11. Operating power gain.

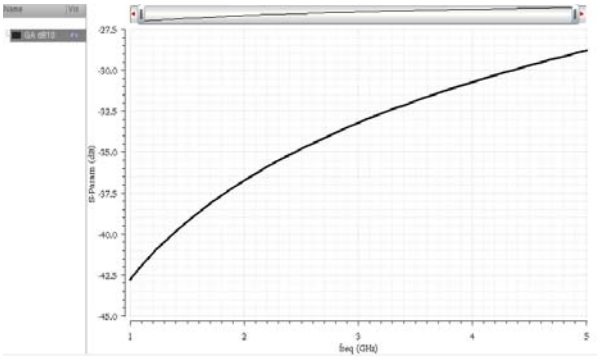

Figure-12. Available power gain.

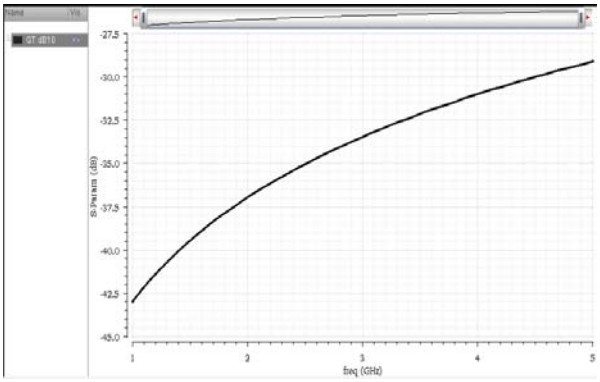

Figure-13. Transducer power gain.

Design parameters and comparison tables

Table-1. Parameter values of components.

Parameter	**C_1, C_2**	**L_1, L_2**	**r_s**	**R_L**	**Finger width** (M1-M8)	**Gate width** (M1-M8)
Value	10 pF	0.4 nH	50Ω	320Ω	32	80µm

Table-2. Comparison of recently reported low power mixers with stacked oscillator mixer.

Reference	**Mixer** [C. G. Tan. 2003]	**Mixer** [V. Vidojkovic et al]	**Mixer** [C. Hermann et al., 2005]	**Stacked mixer**
Process	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.9 µm CMOS
Architecture	Double balanced	Folded switching	Transformer based	Current reused
RF (GHz)	2.4	2.45	2.4	4.2
IF (MHz)	1	1	10	455
Mixer power consumption (mW)	7.2	3.2	1.6	0.2 (mixer only) 1.9 (stacked)
Mixer voltage conversion gain (dB)	13.3	11.9	15.7	39
IIP3 point	-11.5dBm	-10.8 dBm	-12.6 dBm	-12.4dBm
Need external VCO	Yes	Yes	Yes	No

CONCLUSIONS

This oscillator mixer achieves lower supply voltage, higher operating frequency, and better phase noise at free running among recently reported Si-based SOMs and MOS. Table-2 compares the recently reported low-power mixers in the CMOS process with this chip. The mixer in this oscillator mixer operates at a higher frequency and achieves lower power consumption with competitive conversion gain compared to other mixers. The total power consumption (VCO and mixer) of the oscillator mixer is 1.9 mW, which is also lower than the power consumption of a low-power mixer using a 0.18 nm CMOS process. As per this design, oscillator does not need an external VCO to operate in a communication system. The supply voltage of the VCO in an oscillator mixer is only a little higher than the threshold voltage. The low supply voltage and low-power consumption is obtained by using the individual supply voltages and current reuse topology. The phase noise is improved from previous reported SOMs and MOs by using the *LC* tank in this chip. As a result, the oscillator mixer combines the individual mixer and VCO to achieve low supply voltage, low current consumption, and low power consumption with competitive conversion gain. The voltage conversion is calculated and it is better conversion gain to the previous one. The IIP3 point is simulated and spotted and it is at 8.4 GHz and input power is 12.4 mW. The supply voltage and power consumption of this proposed topology can be further reduced by using more advanced CMOS technology.

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