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A LOW POWER AND AREA EFFICIENT CNTFET BASED GDI CELL FOR LOGIC CIRCUITS

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ABSTRACT

The main objectives for today's VLSI circuit designers are designing circuits which occupy less area, consume low power with improved performance. There has always been a tradeoff between these three factors while designing. This work presents a novel idea to satisfy all three factors without any tradeoff. In this work, Gate Diffusion input (GDI) technique is used along with the high performance Carbon Nanotubes Field Effect Transistor (CNTFET). This union of CNTFET and GDI results in low power, area efficient and high performance logic circuits maintaining less complexity. The layout of the logic circuits are also discussed which shows the inclusion of n-CNTFET and p-CNTFET on the same substrate without the need for a twin tub process as is the requirement in implementing GDI technique using MOSFETs. Thereby a standard cell library has been created for CNTFET based GDI logic circuits. The implementation is carried out in Cadence Virtuoso and Electric, a layout tool.

Keywords: CNTFET, GDI, layout.

INTRODUCTION

A low power digital circuit with less area and delay is the need of the hour. There are umpteen techniques in the literature to achieve this goal. However, there has always been a tradeoff between area, power and speed of operation. Carbon Nanotubes Field Effect Transistors (CNTFETs) are promising devices to complement the MOSFETs for three reasons:

a) Since, there is a similarity in the operation and structure of the device with MOSFETs, the well established CMOS infrastructure can be reused.
b) The fabrication process can be reused.
c) It has excellent current carrying capability which has been experimentally demonstrated since
d) Carbon Nanotubes discovery.

It is a hybrid technology evolved where Silicon still remains as the substrate for fabrication with carbon nanotubes as the channel material, which gives enhanced device operation and new functionalities.

Carbon nanotubes are an allotrope of carbon material and now are becoming an important member in the electronics world. The conductivity depends on various parameters and therefore the controlling of the current in these devices is more flexible.

This wonder device is combined with Gate Diffusion input (GDI), a low power technique which maintains low complexity and is very simple to implement. GDI approach allows implementation of a wide range of complex logic functions using only two transistors [1]. This method is suitable for design of fast, low power circuits, using reduced number of transistors, while improving power characteristics and allowing simple Shannon's theorem based design by using small cell library [2]. This paper aims to project the potential of CNTFETs, highlighting the effect of various parameters on its performance. Also, it aims at bringing GDI technique and CNTFET together by creating a standard cell library for CNTFET based GDI logic circuits.

The paper is organized as follows: Firstly, it presents the types of Carbon Nanotubes (CNTs), the electronic properties of CNTs, the CNTFET model that has been used in this work and the dependence of the drain current on various device parameters. Secondly, it presents the GDI technique and CNTFET for GDI cell where the power delay product for each operation of the GDI cell is presented. The layout for the CNTFET GDI cell with the n and p CNTFET on the same substrate is also presented finally.

CNTs and CNTFET

Types of carbon nanotubes

Carbon Nanotubes are cylinders of graphene. Monolayer of graphite is called graphene. The manner in which the graphene sheet is rolled is given by the integers (n, m) and depending on that the Carbon nanotubes are being classified as arm chair (n = m), zigzag (n = 0 or m = 0) and chiral (any other values of n and m). Structure of armchair, zigzag and chiral is shown in Figure-1. The ends of the tube show shape of armchair, zigzag and chiral.

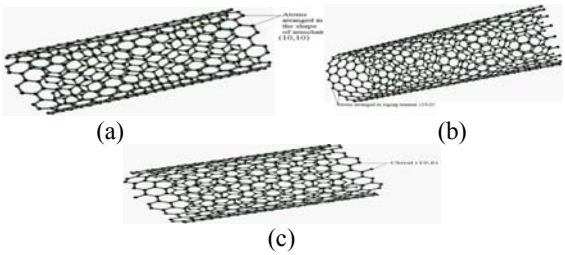


Figure-1. CNTs with different chiral vectors (a) Armchair (b) Zigzag (c) Chiral.

Electrical properties of the CNT can be varied by changing n and m values. The CNTs show metallic behavior as well as semiconducting behavior according to the chiral vectors (n, m). If n=m, the CNT is metallic, else it behaves as a semiconductor. The band diagrams for the CNTs can be obtained by varying the n and m values. The overlapping of valence band and conduction band for a metallic CNT band diagram is shown in the Figure-2.

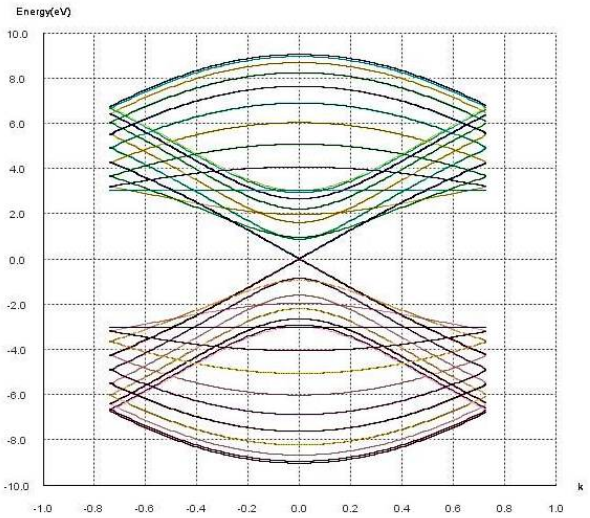


Figure-2. Metallic CNT - Overlapping of bands.

The energy band diagram for semiconducting CNTs is shown in Figure-3. There is a small energy gap between the valence and conduction bands, which makes conduction feasible by applying a small voltage.

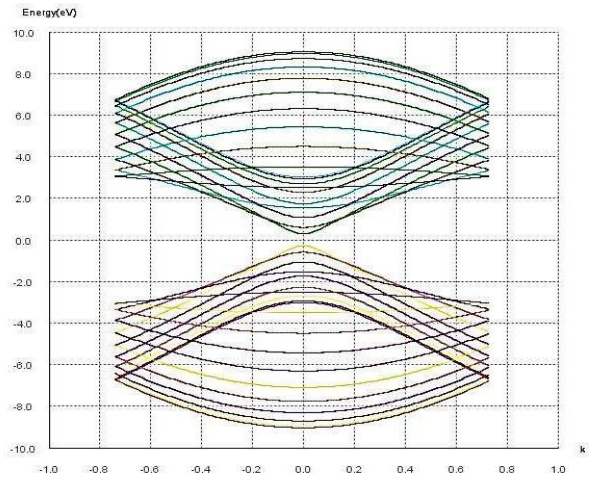


Figure-3. Semiconducting CNT - Energy gap between bands.

Electronic properties of CNT

Circumference of the CNT can be expressed in terms of chiral vector, and is given by the equation (1).

$$Ch = n\vec{a1} + m\vec{a2} \quad (1)$$

Where in equation (1) n and m are integers and $\vec{a1}$ and $\vec{a2}$ are unit vectors of the hexagonal honey comb lattice. Equations (2) and (3) give the chiral angle and the diameter of the CNT.

$$\Theta = \tan^{-1}\left(\frac{\sqrt{3}m}{2n + m}\right) \quad (2)$$

$$D_{CNT} = \frac{\sqrt{3}a}{\pi}\sqrt{n^2 + m^2 + nm} \quad (3)$$

In equation (3), a is the carbon to carbon atom distance and is approximately equal to 0.249nm, n and m are integers. Difference in properties of the CNT is caused by this chiral angle and diameter. This affects the CNT's band gap directly, thus the electronic properties of the CNT can be controlled by changing these parameters. For the semiconductor CNT the diameter dependency on bandgap can be expressed by the equation (4) [5].

$$E_g = \gamma\left(\frac{2a}{D_{CNT}}\right) \quad (4)$$

$$V_{th} = \frac{E_g}{2e} = \frac{aV_\pi}{eD_{CNT}} = \frac{0.43}{D_{CNT}} \quad (5)$$

Equation (5) gives the dependency of threshold voltage on band gap where a = 2.48 Å is the carbon-carbon atomic spacing, $V\pi$ = 3.033 eV is bond breaking energy of carbon molecule, e is the electron charge, and D_{CNT} is the diameter of the carbon nanotubes. From equation (5) it can be inferred that a multithreshold logic design can be effectively done using CNTFET since the threshold voltage is dependent on the diameter. The diameter of the CNT is inversely proportional to the threshold voltage, as diameter increases the voltage drop decreases.

CNTFET model

CNT based transistors are called CNTFETs where the channel is replaced by a CNT or an arrays of CNTs [5]. Experimental results have shown that CNTFETs have high on current and better performance compared to CMOS. Due to the quasi-1D structure, the movement of the electrons is restricted. Only backward or forward movement is possible, which is why the wide angle scattering is forbidden. The current in the CNTFET depends on its chirality, pitch and K_{gate} parameters. CNTFET is implemented using the Verilog-A model developed by Nanoelectronics Group of Stanford University [6] [4].The model is based on ballistic transport [5]. This model accounts for some practical non-idealities for improved accuracy. It includes a complete transcapacitance network in order to produce better

predictions of the dynamic performance and transient response [5].

Dependence on various parameters

The Stanford University Verilog A model is a very versatile model. The creators of the model have enabled the researchers to study the CNTFET by varying the circuit and device parameters. In this paper, we have chosen three device parameters which directly affect the performance of CNTFET. The chosen device parameters are:

a) Dielectric constant of gate dielectric material, K_{gate},
b) Pitch is the distance between the centers of two adjacent CNTs and
c) (n, m), the chiral vectors of CNT.

DC analysis of CNTFET is performed by varying these device parameters. In the model, the default value of the channel length is 32nm, K_{gate} is 16, pitch is 2e-08 and the chirality of the tube is (19, 0).

Firstly, the dielectric constant of the gate is varied to see the effect on the Ion/Ioff ratio. Table-1 shows the effect of different K_{gate} on the Ion/Ioff ratio. The model uses K_{gate}=16. Keeping the drain current of this as a reference value, the drain current of other K_{gate} values can be reviewed. For Silicon dioxide (SiO_2) with a dielectric constant of 3.9, the drain current is reduced. For high-k dielectrics such as Zirconium dioxide (ZrO_2) with a dielectric constant 25 and Hafnium dioxide (HfO_2) with a dielectric constant of 30, the drain current is increased and thereby has very high Ion/Ioff ratio. From this Table-1, one can infer that high-k dielectrics in CNTFET enhances Ion/Ioff ratio.

Table-1. Drain current variation for different Kgate values.

Parameter (K_{gate})	**Drain current at 0.32 V**	**Drain Current at 0 V**	**I_{on}/I_{off}**
SiO_2 - 3.9	417.9nA	554pA	754.33
Default-16	1.1uA	554pA	1985.55
ZrO_2 - 25	1.6uA	554pA	2888.08
HfO_2 - 30	2uA	554pA	3610.10

Secondly, the pitch is varied to see the effect on the Ion/Ioff ratio. Pitch is the distance between the centers of adjacent CNTs in CNTFET. Table-2 shows the effect of change in pitch on the drain current. The drain current increases slightly when the pitch is increased because as the CNTs come closer the screening effect increases and it leads to decrease in the drain current. When the pitch is increased, the distance between the CNTs increases and thereby the screening effect decreases which leads to increase in drain current.

Table-2. Drain current variation for different pitch values.

Parameter (Pitch) ($*10^{-8}$)	**Drain current at 0.32 V**	**Drain Current at 0 V**	**Ion/Ioff** ($*10^3$)
1	1.12uA	42.57pA	26.3
2	1.19uA	42.57pA	27.9
5	1.22uA	42.57pA	28.6

Thirdly, the chirality of the tube is varied to see the effect on the Ion/Ioff ratio. Table-3 shows the variation in drain current for different chiral vectors. When the chirality of the tube is for an armchair (10, 10), i.e. n=m, the tube is metallic. But the model does not show metallic behavior. When the chirality of the tube is (19, 0) for a zig zag type and (19, 8) for a chiral type, the CNT behaves as a semiconductor. The semiconducting CNT gives high Ion/Ioff ratio.

Table-3. Drain current for different chiral vectors.

Parameter (n and m)	**Drain current at 0.32V**	**Drain current at 0V**	**Ion/Ioff**
n=10, m=10	4.12nA	14.48 pA	284.53
n=19, m=0	0.8uA	44pA	18181.8
n=19, m=8	2.39uA	1.09nA	2192.66

The properties of the CNTFET model can be varied as per the requirement. This data can be used as a reference for further research.

GDI Technique

Gate diffusion input

The basic GDI cell is similar to the schematic of an inverter except that the drain and source of PMOS and NMOS transistors are not connected to VDD and GND. Instead the GDI cell has two extra input pins P and N for logic utility thereby increasing the flexibility. The GDI cell with the three input terminals N, P and G is shown in Figure-4. The Table showing the various functions is shown in Table-5. Most of these functions may require 6 to 12 transistors in CMOS, whereas only two transistors are employed in this technique. However, the only drawback of this GDI input will be the fabrication process in which a twin well process should be employed which is more expensive than the standard CMOS process.

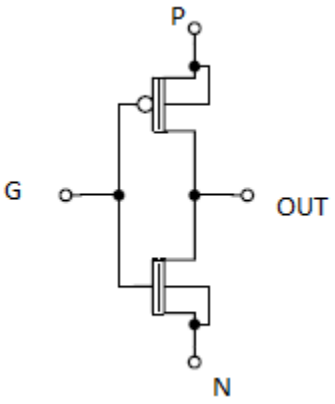


Figure-4. Basic GDI cell.

Table-4. Truth table of gdi cell.

N	P	G	Out	Function
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

With the use of just two transistors, the GDI technique enables the implementation of a wide range of logic functions. Researchers in [1] have already shown that power and delay are much less in GDI logic style when compared to the CMOS logic style.

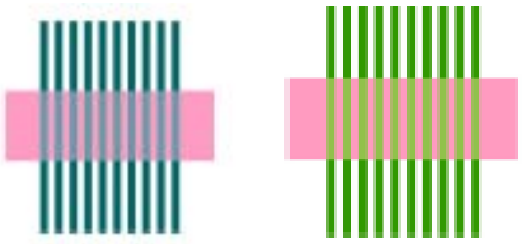
CNTFET for GDI cell

Cost effectiveness is the major problem in CMOS GDI cell, as it requires a twin well process. In this work, this problem is solved by the use of CNTFETs instead of MOSFETs. A complementary CNTFET with p-CNTFET and n-CNTFET can be fabricated on a single substrate. Well fabrication can be avoided thereby making this work cost effective. Using the Verilog A model of CNTFET, the functions were simulated. Table-5 shows the power, delay and the power delay product (PDP) for various functions of the GDI cell. The power is in the order of nano Watt (nW) when CNTFET is used to implement the GDI logic style. In [1], the power is in the milli Watt (mW) order when MOSFET is used for implementation. The delay is also much less when compared to the delay in [1]. This is due to the fact that the model assumes ballistic transport in the channel as opposed to the diffusive transport in the MOSFET channel. The power delay product is a Figure of merit to determine the quality of a digital gate by measuring the average energy consumed per switching event. Due to the union of GDI cell and CNTFET in this work, the power delay product is reduced drastically. For functions without the inverter operation, the PDP is lower than for the functions with the inverter operation.

Table-5. Power delay product of all functions using cntfet based gdi cell.

Function	Power (nW)	Delay (ns)	Power delay product
A'B	5.531	0.014	$7.7 *10^{-20}$
A'+B	12.426	0.0013	$1.615 *10^{-20}$
A+B	0.0639	0.032	$2.047 *10^{-21}$
AB	0.0662	0.049	$3.245 *10^{-21}$
A'B+AC	5.219	0.016	$8.35 *10^{-20}$
A'	27.85	0.035	$9.478*10^{-19}$

Electric, a layout tool is used to create the standard library for CNTFET based GDI cell. This tool supports schematic and layout entry, HSpice/VerilogA netlist generation, and rule checking [7]. The basic layout panel in the Electric tool is used by invoking the mocmos–cn xml technology library. The panel consists of p-CNTFET and n-CNTFET layers, metal layers for routing, substrate contacts, metal to metal contacts and vias. The tool also provides a customizable CNFET technology library with the ability to specify λ-based design rules [7]. Figure 5a and 5b shows the n-CNTFET and p-CNTFET layers respectively.



(a) (b)

Figure-5. (a) n-CNTFET (b) p-CNTFET.

The layout of the CNTFET based GDI cell is shown in Figure-6. A standard cell library for the CNTFET based GDI cell can be created. This standard cell creation will enable ASIC design of the CNTFET GDI cell which implements a wide range of complex functions.

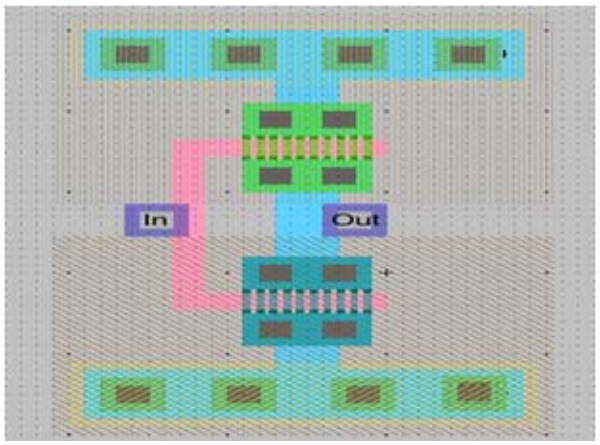


Figure-6. Layout of CNTFET based GDI cell.

CONCLUSIONS

CNTFET based GDI cell has been simulated and presented. There has always been a tradeoff in achieving the low power, less area and faster circuits for integrated circuits. In this work, there is no need for compromise on any of the three factors. The low power is achieved by using the GDI technique which is complemented by the use of CNTFET for the implementation. As CNTFETs have ballistic transport, the power dissipation is very less. The less area is achieved by employing only two transistors in the GDI cell. This is again complemented by the use of CNTFETs for the implementation which occupies less space as compared to MOSFETs. On a single substrate, the p-CNTFET and n-CNTFET can be fabricated which reduces complexity in fabrication too. Faster circuits are achieved due to the ballistic transport of CNTs in the channel. The potential of CNTFETs is presented by showing the effect of device parameters on the Ion/Ioff ratios. A layout for the GDI cell is also presented to create a standard cell library for the GDI cell. The results illustrate a significant improvement in terms of minimizing power consumption, enhancing the speed of the design which leads to best PDP.

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