VOL. 10, NO. 1, JANUARY 2015 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences


www.arpnjournals.com

DESIGN OF LOW POWER WRITE DRIVER CIRCUIT FOR 10T SRAM CELL

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ABSTRACT

Aggressive scaling of transistor dimensions with each technology generation has resulted an increased integration density and improved device performance at the expense of increased leakage current. Diagnosis is becoming a major concern with the rapid development of semiconductor memories. In this paper, we propose a very low cost Design-for-Diagnosis (DfD) solution for design of write driver circuit and to improve access time in write operation, in which two decoders and one sense amplifier are used in each column of 10T Static Random Access Memory (SRAM) cell. In SRAM bit- cells utilizing minimum sized transistors are susceptible to various random process variations. The 10T SRAM cell for low voltage and energy constrain application is analyzed with respect to power dissipation. The analyzed 10T SRAM cell is compared with low power 6T SRAM cell. The simulation result based on 32nm technology shows that 37.03% power reduction compared to 6T SRAM bit cell. A control circuitry is used to enable the both column decoder and row decoder. However, there is a marginal increment in the area due to additional components used in the proposed design without compromising with the power.

Keywords: write driver circuit, static random access memory, design-for-diagnosis, 10T SRAM, SoC.

INTRODUCTION

Static RAM cells are used in a wide variety of applications. These range from memory arrays to ICs of all kinds containing embedded SRAMs [1, 2, 3]. As the demand for reduced power and delay in components containing SRAMs increases, adjustments will need to be made to meet these requirements. There have been many proposed designs for SRAM cells that increase performance in some way, but the six-transistor (6T) differential memory cell is still recognized as being a good balance between size and performance [4, 5, 6]. There have also been proposals for different methods of accessing memory cells that improve on speed and/or power [7]. One such method, ten-transistor (10T), focuses on reducing the voltage level on the bit-lines during read and write operations in order to minimize power consumption. The problem with this design is that while it significantly reduces power, it also causes delay to increase. In this work has been making memories responsible of SoC yield [1]. SRAM memoy is one of the major concerns for designing embedded systems. Memory chip will occupy 90% of the chip area and the SRAM cell transistors normally use minimum width-to-length ratios to stringent area constrain. Increasing fluctuations in transistor parameters (e.g., threshold voltage) and process parameters (e.g., doping level) as device dimensions and supply voltage scale down in the nanoscale range, leads to maximize the cell stability for future technology.

The purpose of this paper is to present our novel technique for decreasing power during a write memory access. The description of the 10T SRAM with proposed write logic is given. DfD principle is discussed in designing decoder and sense amplifier [7, 8]. Section III explains the methods for designing and comparing the standard 6T and proposed 10T SRAM cell writing techniques and the results are presented. The fourth section gives a power analysis and discussion of the results, followed by concluding remarks in Section V. CMOS SRAM memory is a main role in modern microprocessors. Due to its complex 10T structure memory density is constantly growing in system-on-chip (SOC). This is confirmed by the SIA roadmap (Semiconductor Industry Association) which forecasts a memory density.

10 T SRAM cell design

In the 10T bit cell, as shown in Figure-1, a separate write port comprised of 10-transistors was used, while write access mechanism and basic data storage unit are similar to standard 6T bit cell. This bit cell also offers the same benefits as the 6T bit cell, such as a non-destructive write operation and ability to operate at ultra low voltages. In particularly, the problem with the isolated write-port 6T cell is analogous to that with the standard (non-isolated read-port). The only difference here is that the leakage currents from the un-accessed bit cells sharing the same write bit-line, RBL, affect the same node as the write-current from the accessed bit cell. As a result, the aggregated leakage current, which depends on the data stored in all of the un accessed bit cells, can pull-down RBL even if the accessed bit cell based on its stored value should not do so. This problem is referred as an erroneous read. The erroneous write problem caused by the bit line leakage current from the un-accessed bit cells is managed by this 10T bit cell by providing two extra transistors in the read-port [11-13]. These additional transistors help to cut-off the leakage current path from RBL when RWL is low and makes it independent of the data storage nodes content.

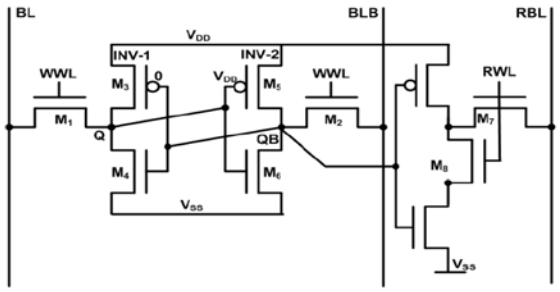

Figure-1. Schematic diagram of 10T SRAM bitcell.

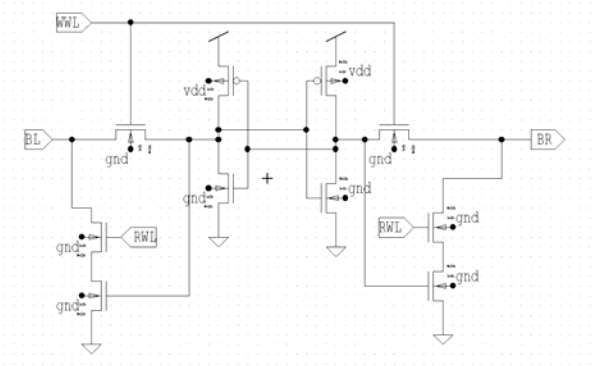

Figure-2. Simulation of 10T SRAM cell.

MEMORY CELL OPERATIONS

Read operation: Considering the case of reading Q=0; before reading a value from the storage nodes, the bit line BL is pre-charged to VDD. The read word line RL is then asserted to VDD. The storage node Q' that stores a 1 is statically connected to the gate of MRA (Read Access Transistor) and will drain the charges on the bit line through MRD to GND as the RL is 1, which means that the bit line has just read a 0. On the contrary, when Q=1, Q' will be 0 and MRA will be in cutoff and the bit line BL would not be able to discharge through MRD to Gnd, and it would read a 1. [17].

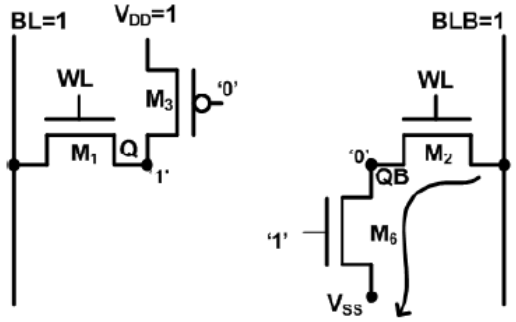

Figure-3. Memory read and write equivalent circuit.

Figure-3 shows the 6T SRAM equivalent schematic diagram during read operation. Bit lines are pre charged to supply voltage before read operation. The read operation is initiated by enabling the word-line (WL) and thereby connecting the internal nodes of the SRAM bitcell to bit-lines. The bit line voltage is pulled down by the nMOS transistor at the '0' storage node and the difference between two bit line voltages will be detected by sense amplifier. When the word line (WL) is high, one of the bit line voltages is pulled down through transistors M2 and M6 or M1 and M4. The transistors M2 and M6 forms a voltage divider, because of current flowing through M2, the potential at node QB is no longer at '0'V. Also it should not go beyond switching threshold of inverter (INV1) to avoid destructive read. The rising of potential depends on sizing of access transistor and pull down transistor which is defined as a bitcell ratio.

Write operation: The word-line WL is charged to VDD as in 6TStandard SRAM. Since NMOS is a stronger driver than PMOS, no problem is incurred while writing a 0 into the cell. The absence of the pull down NMOS for memory node Q allows writing a 1 into the cell easily. Writing a 1 is done by pre-charging bit-line BL to VDD. While writing 0, the bit-line BL is discharged and then word-line WL is charged to VDD as in 6T Standard SRAM. The write operation begins by forcing a differential voltage (V*DD*, and 0) at the bitline pairs (BLB and BL). This differential voltage corresponds to the data to be written at the storage nodes (Q and QB) and it is controlled by the write drivers. The WL is then activated to store the information from the bit-line pairs to corresponding storage nodes. Assume, the nodes Q and QB initially store values '1' and '0' respectively. When the WL is asserted the access transistor (M1) connected to BL (at '0') is turned on, a current flows from V*DD* to BL through M3 and M1. This current flow lowers the potential at Q. The potential at the node Q has to go below the trip point of the inverter (INV2) for a successful write operation and this depends on the ratio of pull-up transistor (M3) and the access transistor (M1). This ratio is referred to as the pull up- ratio.

4X4 SRAM memory cell

This section describes the designing of 4x4 SRAM cell arrays of 4 rows and 4 columns. Each block of the array is of 10T SRAM cell. There are 4 rows and 4 columns arranged to form a 4x4 SRAM cell array. To address these rows of cells, the decoder is used prior to the array arrangement. As the row consists of 4 cells it constitutes to form half a byte. The AND based 2:4 decoder is used to generate the address lines, the number of transistors used for the decoder circuit is 28 These address lines which form the outputs of decoder are connected to each row of the array.

The input and output data control consists of write and ready circuitry. From the decoder the address is selected in the array and 4 bits of data is written or read in parallel from cell 1 to cell 4. Input-output buffers are also

required for each column as the decoder selects only one row of the array, the other cells may generate glitch, this can be nullified by the buffers. Also a 8x1 Multiplexer can be used to combine all the output of single SRAM cells of each column to make a single output data. The Figure-3 shows the 4x4 SRAM cell array design consists of 10T one bit SRAM cell, decoders and buffers. The total number of transistors utilized in this 4x4 SRAM cell array is 172 [10].

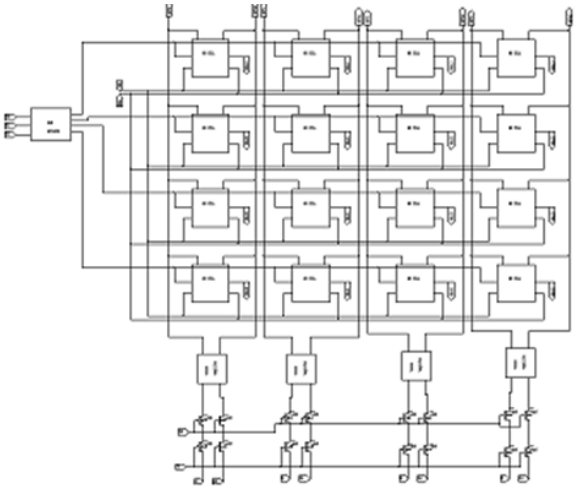

Figure-4. Designed 4x4 SRAM cell array.

Design of 2:4 decoder

A decoder is a digital logic circuit which takes multiple coded input and converts to coded multiple outputs where the input and output codes are different. The decoding is necessary in applications like data multiplexing, 7 Segment display and memory address decoding. The simple example of the decoder is an AND gate, the AND gate output will be high when all the inputs are high, this output is also known as active high output. A little more complex decoder is the n-2n binary decoders. These decoders convert n coded input to 2n unique outputs. The Figure-4 illustrates the decoder circuit for 2 coded inputs to 4 coded outputs. It consists of 2 NOT logic gates and 4 AND logic gates. The output of the 2:4 decoders further clarified from its inputs like r1, r2 and outputs like WL1, WL2, and WL3 AND WL4. Figure-5 shows the inputs r1, r2 and corresponding outputs [8].

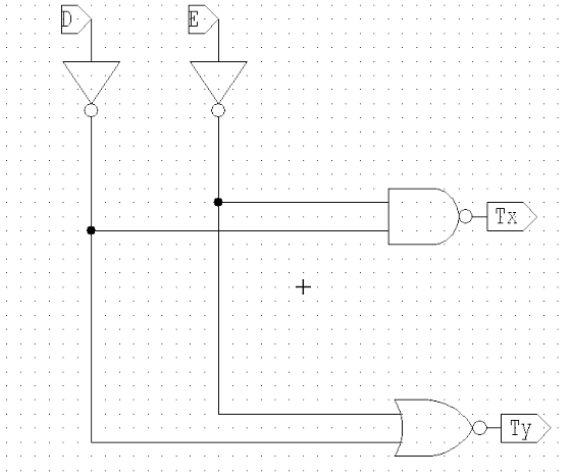

Figure-5. Design of 4:2 Decoder circuit.

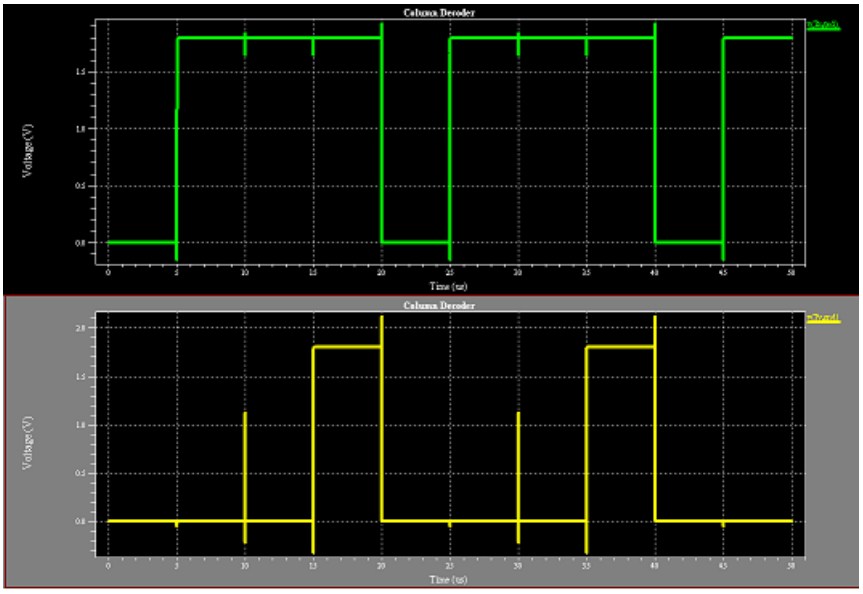

Figure-6. Output response of 4:2 Decoder circuit.

The output of the 2:4 decoders further clarified from its inputs like r1, r2 and outputs like WL1, WL2, and WL3 AND WL4. Figure-6 shows the inputs r1, r2 and corresponding outputs [8].

Read and write operation of 4x Sram's cell array

At initial stage of read operation, decoder will be in inactive mode. As soon as decoder is enabled, they are pre-charged first. This process makes all output high for a small amount of time. This address is invalid then address settles down according to the input of the decoder and one particular SRAM cell is activated. Activation of read enable (RE) signal activates the read buffer.

The ready SRAM cell data traverses towards ready buffer. Thus the data bit is read from memory cell. To continue the read operation address bits are changed to address the next memory cell. During write operation, the address is selected and data is given to write circuit as input. Upon the activation of write enable (WE) signal activates the write buffer output change according to the input. The feedback action in SRAM cell then stabilizes the data of the memory. This signal is disabled for safe write operation and to avoid further writing of spurious data. To continue the write operation to other cells address bits are changed and same procedure is repeated again and again for required times. The Figure-7 shows the simulated output of 4x4 SRAM cell array.

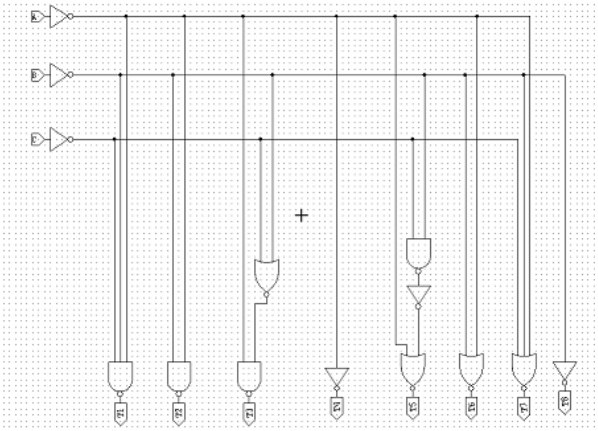

Figure-7. Simulated output of 4x4 SRAM cell array.

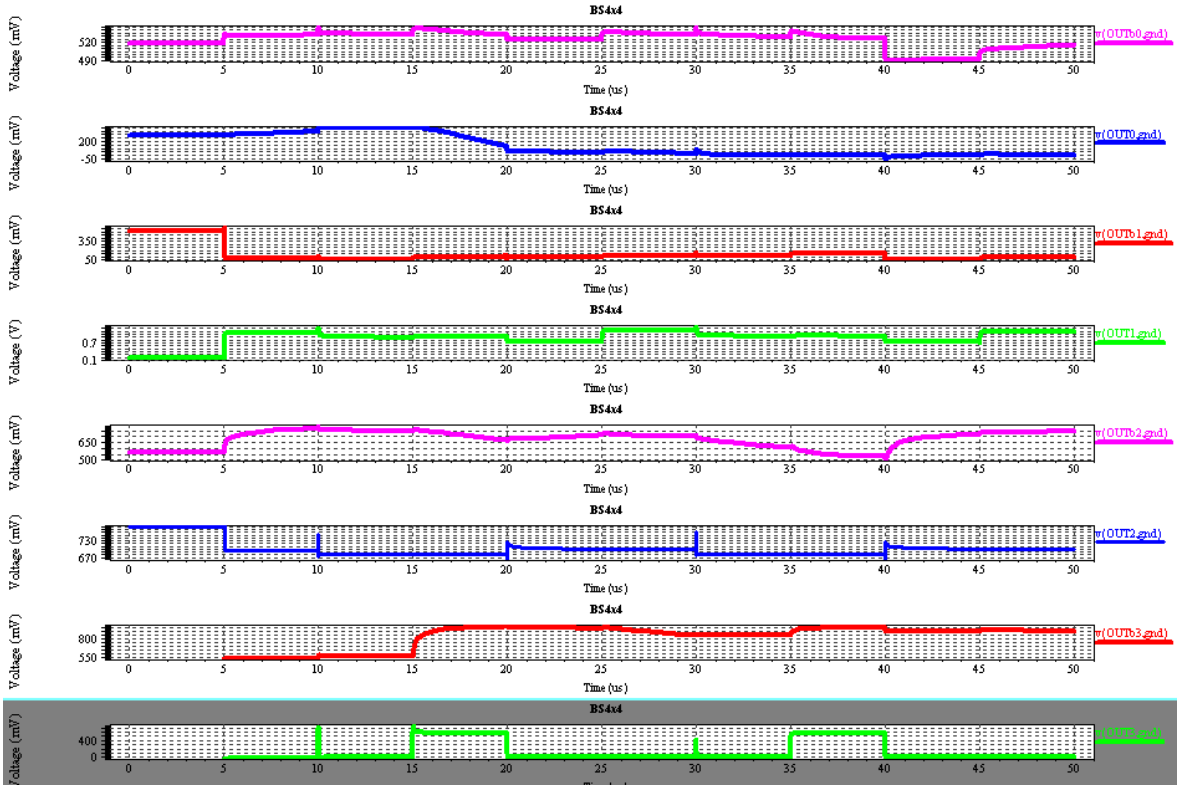

Figure-8. Simulation output of 4X4 SRAM memory cell.

Design of write driver circuit for 10 T SRAM cell

Logic condition

As shown in Section 2, the write driver must act the pull down of one of the two bit lines. The other bit line is maintained at Vdd during the write operation. From this statement, we can extract a first condition for a fault-free operation of the write driver:

$$BL \oplus \square BLB \; \square\square 1 \qquad (1)$$

If this equation is not satisfied during a write operation, then it means that both bit lines have the same voltage level. In case of Vdd, no write operation is performed. Conversely, the two bit lines at Gnd indicate that both w0 and w1 operations are performed simultaneously. This first condition allows performing a logical diagnosis of the write driver. Nevertheless, it does not allow verifying the exact voltage level driven on the bit lines during the write operation. Thus, an additional analog condition is needed to diagnose weak write drivers. The final diagnosis result (S) is a function (NOR gates) of both outputs VLOW and VHIGH levels in order to verify the logic condition. Table-1 provides the truth Table of the structure. A fault free behavior is observed (S = 1) if WD is below 10% of Vdd, i.e. final VLOW level is low, and WDB is above 70% of Vdd, i.e. final VHIGH level is high (gray line on Table-1) in case of a W0 operation. Consequently, such a DfD solution allows the diagnosis of low and high levels at the same time as two sense amplifiers and two reference voltage levels are embedded in the structure.

Table-1. Truth table of the DfD solution

VLOW	VHIGH	S
0	0	0
0	1	1
1	0	0
1	1	0

Simulation of write driven circuit for 10 T SRAM cell

Figur-9. shows the simulation result of 10T SRAM cell with write driven enable circuit.Additional BL, BLb lines are added along with transistors. This forms write driver circuit (4:2 decoder). The power for both static and dynamic is calculated for various temperature range. This will be shown in Table-2. [18]

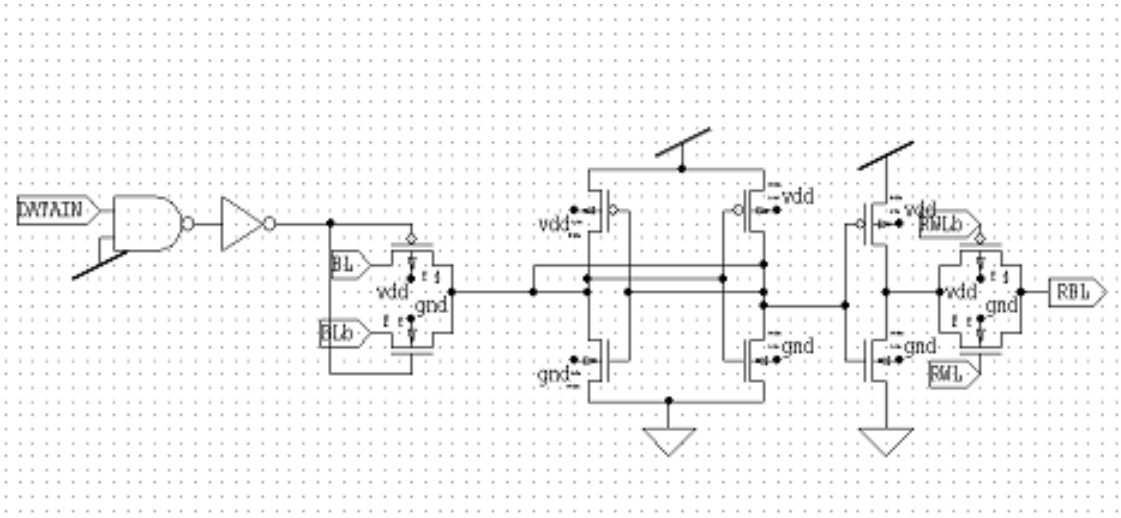

Figure-9. Simulation of write driven circuit for 10 T SRAM cell.

10T output waveform for the circuit with write enable

Figure-10 shows the waveform of 4X4 SRAM array with room temperature. If the temperature various in any one of the component in a SRAM cell, dynamic power, static power and total power will be varied shown in Table-2.

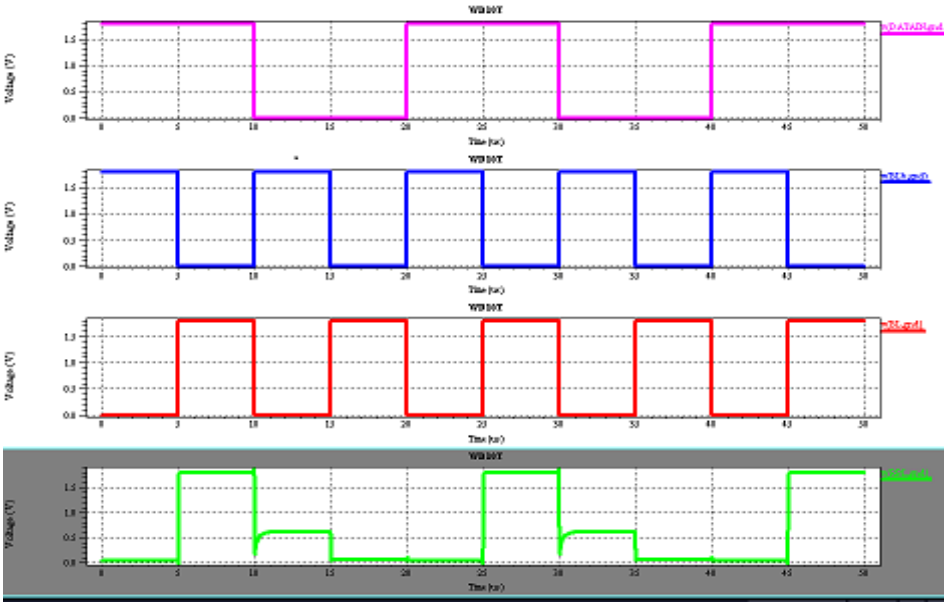

Figure-10. Simulation of 10T SRAM cell with write driver circuit.

Table-2. shows various power calculation at different temperature conditions for input voltage range 0 to 33mV.

S. No.	Temperature (°C)	Transient analysis time (Sec)	Total time (Sec)	Static power (Watts)	Dynamic power (Watts)	Total power (Watts)
1	0	0.18	0.20	0.151	0.036	1.879
2	25	3.78	4.13	0.162	0.057	4.334
3	45	4.01	4.61	0.193	0.056	6.429
4	65	3.54	3.81	0.131	0.052	14.372
5	75	3.90	4.49	0.135	0.050	14.372

From Table-2 we found that when temperature increases from 0°C the total power increases with respect to time. Dynamic and static power remains constant for greater temperature range. [14, 15] Transient time increases so total time of the write drier circuit increases, thereby speed of operation also increases.

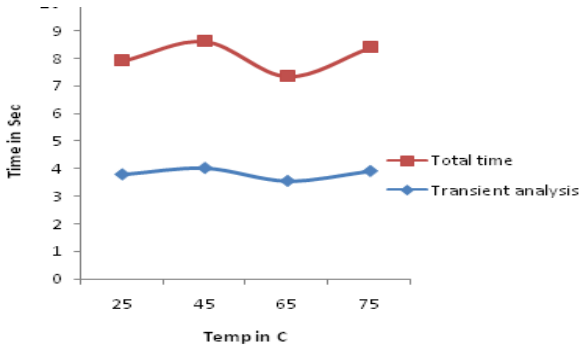

Figure-11. Comparison of total and transition time between memory cells.

CONCLUSIONS AND FUTURE WORK

The output of the decoder and 4X4 SRAM cell array is taken as the word line WL of SRAM. The bit lines BL from bl 3 to bl 0 are common to SRAM of each column. Table-2 shows the effect on dynamic power, static power and total power with various temperatures by giving variable Supply Voltage ranging from 0 V to 1 V to CMOS SRAM cell Array. It allows to identifying wrong or weak write drivers by verifying logic and analog conditions that guarantee the fault-free behavior of the write drivers. Moreover, it allows a fast diagnosis (only three write operations are needed) and induces a low area overhead. In a future work, we plan to extend this DfD solution so that it can deal with others blocks connected to the bit lines such as pre-charge circuits and sense amplifiers for total SRAM cell array.

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