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# PERFORMANCE EVALUATION OF BPN BASED VITERBI DECODER FOR DECODING 2-BIT AND 3-BIT ERRORS

V. Balamurugan and Dr.N. M. Nandhitha
Department of Electronics and Communication Engineering
Sathyabama University, Jeppiaar Nagar, Old Mamallapuram Road, Chennai, India
E-Mail: vbbala@gmail.com

#### ABSTRACT

In communication, convolution codes are extensively used for reliable data communication at receiver's end the coded messages are decoded with Viterbi Decoders. However when the channel is noisy decoding becomes computationally complex even with enhanced Viterbi Decoder, hence it necessitates an efficient computationally less complex decoders. In this paper Viterbi Decoders are realized in BPN, performance of the decoder for 2-bit errors and 3-bit errors is studied in terms of accuracy. It is found that Back Propagation Network (BPN) based Viterbi Decoder functions well for both 2-bit and 3-bit errors even after shrinking the hidden layer architecture.

Keywords: Viterbi decoders, BPN, 2-bit errors, 3-bit errors, accuracy.

#### 1. INTRODUCTION

In general Viterbi Decoders are extensively used for obtaining the message bits from the convolution encoded bits. These Viterbi Decoders are consisting of Branch Metric Unit (BMU), Add Compare Select Unit (ACSU) and Survivor Memory Unit (SMU). Though these decoders are computationally complex, they are highly capable of detecting one bit error. However if the channel is noisy and more than one bit error occurs, then the decoder involves more number of stages. Hence it is unsuitable for high speed decoding applications in real time applications like video conferencing, defense etc. Thus data transmission necessitates an efficient decoder that extracts the message bits accurately with less complexity. In this paper, BPN based convolutional decoder is developed for 2 bit and 3 bit errors. This paper is organized as follows: In section II related work is presented, section III provides the proposed work, in section IV results and discussion and Section V concludes the work.

## 2. RELATED WORKS

Mohamed *et al.* 2013 implemented register exchange method on FPGA. This replicates the trace back method with less hardware. The numbers of registers are reduced by normalizing the state metrics of the symbol. Normalization is achieved through split search which provides an output rate of one symbol thereby reducing the number of registers. The proposed method also eliminated the use of RAM thereby requiring lesser silicon area. Also the speed is higher and the latency is decreased. In the proposed method, modified register exchange method is used to reduce the power consumption.

Ted Frumkin *et al.* 2012 designed an optical Viterbi Decoder on a silicon chip using an optical memory cell with 2 input arms. Incoming bits are encoded with Quadrature phase-shift keying (QPSK) modulation technique. Initially Viterbi Decoder memory cell was simulated using RF module by choosing TE wave with a

transient propagation. The refractive index is 3.48. The input signal wavelength is  $1.1\mu m$  and  $1.2\mu m$  for the gain. During fabrication, the amount of energy stored in the ring resonator is increased by increasing the coupling area. A single mode fiber with  $3\mu m$  edge is used for input and a multimode fiber is used as an output. The proposed nanophotonic Viterbi Decoder has higher processing speed with lesser hardware.

Peiyu Tan and Jing 2012 proposed a modified Quantum Viterbi Decoder (QVD) for efficient retrieval for messages from convolutional codes. An efficient linear circuit based technique is used to map the syndrome to the candidate vector. Also in the proposed technique, the number of iterations is drastically reduced. It used the principal of syndrome decoding which is similar to the maximum likelihood decoding. The proposed Decoders used a systematic and concrete procedure that resulted in low complexity. The steps involved in the decoding algorithm are as follows: Quantum convolutional code is represented as a transfer polynomial; syndrome decoding is performed on the classical convolutional code, feeding the error pattern to the recovery block.

Tijjani Adam *et al.* 2012 analyzed the performance of hamming code and convolution code over uncoded techniques for reliable data transfer in a communication channel. Hamming and convolution codes were generated for the same set of three bit messages that is message bits from 000 to 111. Noise was deliberately introduced to affect 6 bits in the code word. An adaptive decoder was then used to decode the noisy code words from the study, it was concluded that convolution codes provided higher reliability than the hamming coded and the uncoded transmission of data bits.

Y.H.Shiau *et al.* 2012 implemented a power efficient decoder for extracting message bits from convolution codes. It is based on the state transparent convolutional code definition by which a bit reverse decoder is used to recover the error free segments and Viterbi Decoder is used for decoding the erroneous

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segments. Bit reverse decoder results in reduced power consumption, switching between these two decoder is achieved through clock gating which further saves the power in order to reduce power consumption of Adaptive Survivor Memory Unit( ASMU) the registers are grouped into several RE segment and clock gating is applied to each segments rather than every register. It is found that bit error rate degradation is avoided as the correct start and terminal states of the survival path where correctly determined.

JinJin He et al. 2012 proposed a precomputation architecture which reduces the power consumption without degrading the decoding speed, q-step precomputation was pipelined into q-stages, thereby reducing the delay of each stage by q. However the performance of the proposed technique is dependent on the optimal choice of q. In order to reduce the computational overhead in the Branch Metric Unit (BMU) was also reduced. However it is found that precomputation is unsuitable for low rate convolution codes but in the case of TCM systems, precomputation drastically decreases the computational overhead. The proposed Viterbi Decoder consumes only 30.8% of the power of the conventional Viterbi Decoder.

## 3. PROPOSED METHODOLOGY

BPN is a multilayered feed forward network which is widely used for prediction and classification. It consists of one input layer, one or more hidden layers and an output layer. This network learns from a set of exemplars and predicts the output for a new set of inputs. Once the neural network is trained and tested, it is implemented with the updated weights and bias values. As Viterbi Decoders also accepts a set of input codes and determine the message bits, BPN can be used for realizing a Viterbi Decoder.

However the complexity of the neural network increases with the hidden layers. On the other hand if the number of neurons in each hidden layer is decreased the accuracy of the result is compromised. Based on this aspect a tradeoff has to be obtained between the number of hidden layer and the number of neurons in the hidden and the accuracy of the result. In this paper, two sets of exemplars are created by deliberately introducing two bit and three bit errors. Three different BPN architectures are designed with 2, 3 and 1 hidden layers with 20, 10, 5; 20, 5 and 10 neurons respectively. Tansigmoidal is the activation function for the hidden layer and "pure linear" is the activation function for the output layers the learning and momentum parameters are fixed as 0.1. The mean square errors is 0.00001, the number of exemplars are 81, 72 out of which 2 different sets of 40 and 36 exemplars are used for test and training.

## 4. RESULTS AND DISCUSSIONS

In order to have a tradeoff between the accuracy and the computational complexity the numbers of neurons in the hidden layers are varied. In this paper, two bit and three bit errors are deliberately introduced into the convolutional codes. Five bit convolutional codes are generated for three bit messages using two parity generators. All the probabilities in which two bit and three bit errors can occur are exploited and the exemplars are generated with all the combinations.

Table-1 and 2 shows the exemplars of two bits and three bits altered convolutional codes for training the BPN. In row 1 of Table-1, the code bits D9, D8 are altered. Similarly in Table-2, the code bits D9, D8 and D7 are altered. After training the BPN, the performance of the network is measured in terms of accuracy for a separate set of exemplars. In order to reduce the computational complexity, the number of hidden layers and the neurons in the hidden layer are reduced. From Tables-3 and 4, it is found that the accuracy is good for message bits 010, 011 and 110 (two bits altered due to errors). However the performance has degraded for highly corrupted noisy channel that resulted in three bit errors.

**Table-1.** Exemplars with Two Bit Error.

S.No	Convolutional code									Output codes			
1	1	1	0	0	0	0	0	0	0	0	0	0	0
2	0	0	1	0	1	1	0	0	0	0	0	0	1
3	1	1	1	1	1	0	1	1	0	0	0	1	0
4	0	0	0	1	0	1	1	1	0	0	0	1	1
5	1	1	0	0	1	1	1	0	1	1	1	0	0
6	0	0	1	0	0	0	1	0	1	1	1	0	1
7	1	1	1	1	0	1	0	1	1	1	1	1	0
8	0	0	0	1	1	0	0	1	1	1	1	1	1

**Table-2.** Exemplars with Three Bit Error.

S.No.	Convolutional code									Output codes			
1	1	1	1	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	1	1	0	0	0	0	0	0	1
3	1	1	0	1	1	0	1	1	0	0	0	1	0
4	0	0	1	1	0	1	1	1	0	0	0	1	1
5	1	1	1	0	1	1	1	0	1	1	1	0	0
6	0	0	0	0	0	0	1	0	1	1	1	0	1
7	1	1	0	1	0	1	0	1	1	1	1	1	0
8	0	0	1	1	1	0	0	1	1	1	1	1	1

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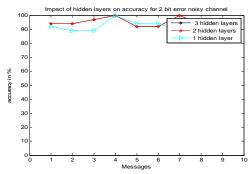
**Table-3.** Accuracy of the proposed decoder including (+/-1 bit) error.

	2 Bit Er	ror		3 Bit Error				
Samples	20,10, 5,3	20,5,3	10,3	20,10, 5,3	20,5,3	10,3		
000	94	94	94	44	22	33		
001	97	94	92	33	27	39		
010	100	100	97	44	39	17		
011	100	100	100	28	50	31		
100	92	92	97	30	36	36		
101	97	97	100	36	36	31		
110	100	100	94	30	14	33		
111	94	94	94	36	41	39		

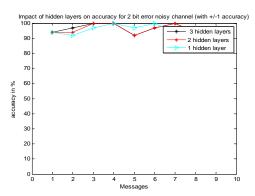
**Table-4.** Accuracy of the proposed decoder with no error.

	2 Bit E	ror %		3 Bit Error %				
Samples	20,10, 5,3	20,5,3	10,3	20,10, 5,3	20,5,3	10,3		
000	94	94	92	31	8	19		
001	94	94	89	0	8	19		
010	97	97	89	31	11	8		
011	100	100	100	8	19	14		
100	92	92	94	19	22	22		
101	92	92	94	19	25	11		
110	100	100	89	22	5	22		
111	94	94	94	14	28	25		

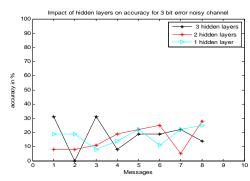
The results are also shown in Figures-1-4. In applications like video conferencing, video downloading etc, one bit errors may not pose a serious problem. Hence the performance of these networks is measured by allowing one bit errors.



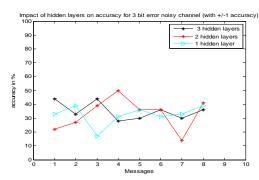
**Figure-1.** Impact of hidden layers on accuracy for 2 bit error noisy channel.



**Figure-2.** Impact of hidden layers on accuracy for 2 bit error noisy channel (with +/- 1 accuracy).



**Figure-3.** Impact of hidden layers on accuracy for 3 bit error noisy channel.



**Figure-4.** Impact of hidden layers on accuracy for 3 bit error noisy channel (with +/- 1 accuracy).

## 5. CONCLUSIONS

In this paper, BPN based Viterbi Decoders are developed to decode the message bits coded with convolution encoder. Deliberately two bit and three bit errors were introduced and the performance of the network is analyzed in terms of accuracy. It is inferred that BPN based classifier works well for two bit error recovery rather than three bit errors. In order to improve the performance it is necessary to optimize the learning and momentum parameters in weight updating during gradient decent learning as the major concern about BPN is its complexity. In this paper complexity of BPN is reduced by reducing the number of hidden layers and hidden layer

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neurons. It is found that the accuracy of detection is not compromised even when the number of hidden layers and neurons were reduced.

#### REFERENCES

- [1] Abdulrazaq Muhammad B., Abdullahi Zanna M., Almustapha Mohammed D, Dajab Danjuma D, Low Complexity FPGA Implementation of Register Exchange Based Viterbi Decoder, IEEE International Conference on Emerging & Sustainable Technologies for Power & ICT in a Developing Society (NIGERCON). 2013, pp.21-25.
- [2] Ted Frumkin., Amihai Meiri. and Zee Zalevsky. Nanophotonic Viterbi Decoding, IEEE 27<sup>th</sup> Convention of Electrical and Electronics Engineers in Israel. 2012, pp.1-5.
- [3] Tijjani Adam., Uda. Hashim. and Usman S., Sani Retrieving the Correct Information: Channel Coding Reliability in Error Detection and Correction, Fourth International Conference on Computational Intelligence, Modeling and Simulation. 2012, pp.400-404.
- [4] Y.H. Shiau, H.Y. Yang, P.Y. Chen, S.G. Huang, Power-efficient decoder implementation based on state transparent convolutional codes, The Institution of Engineering and Technology, IET Circuits Devices Syst., 2012, Vol. 6, Issue. 4, pp. 227–234.
- [5] Jinjin He., Huaping Liu., Zhongfeng Wang., Xinming Huang. and Kai Zhang. High-Speed Low-Power Viterbi Decoder Design for TCM Decoders, IEEE Transactions On Very Large Scale Integration (VLSI) Systems. Vol. 20, No. 4, April 2012, pp.755-759.
- [6] Peiyu Tan. and Jing Li. Quantum Convolutional Codes: Practical Syndrome Decoder, 46<sup>th</sup> Annual Conference on Information Sciences and Systems. (CISS), 2012, pp.1-6.