



EFFECT OF STRUCTURAL AND DOPING PARAMETER VARIATIONS ON NQS DELAY, INTRINSIC GAIN AND NF IN JUNCTIONLESS FETS

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ABSTRACT

This paper investigates the effect of process variations on RF metrics, non-quasi static (NQS) delay, intrinsic gain and noise figure (NF) in 30 nm gate length Junctionless FET by performing extensive 3D TCAD simulations. Sensitivity of NQS delay, intrinsic gain and NF on different geometrical parameters and fin doping are studied. The most significant parameters are found to be gate length, fin width and fin doping. The underlap and gate oxide thickness have a least impact over these RF metrics.

Keywords: junctionless FET, NQS delay, intrinsic gain, NF, TCAD.

1. INTRODUCTION

Junctionless transistor is a novel device that has gained significant attention recently. This is proposed by (J.P. Colinge *et al.* 2009; C.W. Lee *et al.* 2010). Since the Junctionless FETs use the same doping type and concentration in the channel region to that in the source and drain, or at least to that in the source and drain extensions, these devices do not have any source or drain junctions. Because the gradient of the doping concentration between source and channel or drain and channel is zero, no diffusion can take place, which eliminates the need for rapid thermal annealing (RTA) techniques and allows one to fabricate devices with shorter channels (J.P. Colinge *et al.* 2010; J.P. Colinge *et al.* 2010a).

The DC characteristics of Junctionless devices are discussed in the literature (C.W. Lee *et al.*, 2010a). Junctionless FET based 6T-SRAM cell is already reported (Kranti *et al.* 2010). Few papers are also available on RF/analog performance of Junctionless FETs (Cho *et al.* 2011; Doria *et al.* 2011) where the authors compared the analog performance of the Junctionless devices with the inversion mode devices.

Recently the RF performance of Junctionless MOSFETs for ultra-low power analog applications has been reported by Ghosh *et al.* (2012). Sensitivity of threshold voltage to nanowire width variation in Junctionless transistors has been studied (Choi *et al.* 2011). A more comprehensive sensitivity analysis of Junctionless RF performance is yet to be explored.

In this paper, nine different geometrical parameters and one doping related parameters of Junctionless FET are varied over a wide range to study their effect on NQS delay, intrinsic gain and noise figure. Next section describes the simulation environment. Section III discusses the simulation results. Finally section IV we provides conclusions.

2. SIMULATION ENVIRONMENT

2.1 Device description

Sentaurus TCAD simulator from Synopsys (Synopsys, 2012-13) is used for this study. Figure-1 shows the 2D structure of the Junctionless FET. The 3D device structure is shown in Figure-2(a). Figure-2(b) shows a 2D cut of the above 3D structure which depicts the fin cross section i.e. in Figure-2(b) source to drain axis runs perpendicular to the page.

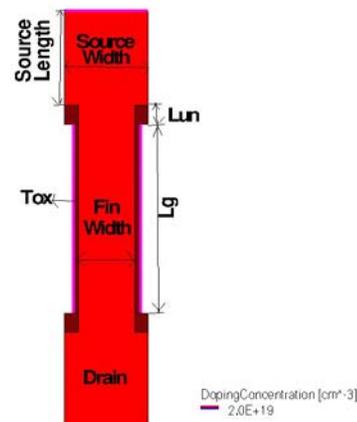


Figure-1. 2D structure of Junctionless FET.

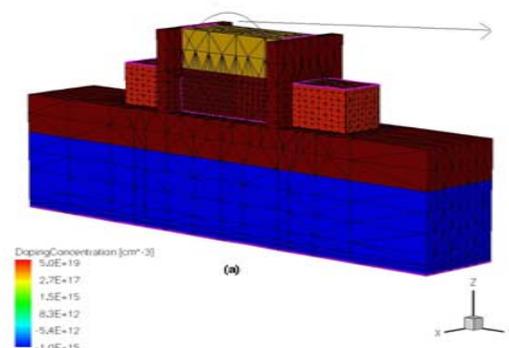


Figure-2(a). 3D structure of Junctionless FET.

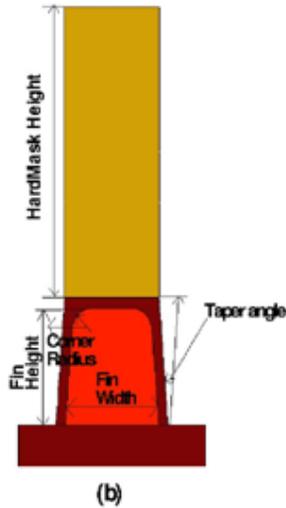


Figure-2(b). Enlarged portion of the rounded region.

2.2 Parameter space

The effect of process parameters, gate length (L_g), underlap (L_{un}), fin width (W), gate oxide thickness (T_{ox}) and fin doping (N_{fin}) on NQS delay, intrinsic gain and NF are studied with the 2D simulations. The channel doping and source/drain doping can be combined into fin doping in Junctionless FET. Some of the parameters like fin height (H), source/drain cross-sectional area, fin taper angle, corner radius and hard mask height (HM) cannot be studied with 2D simulations. So these parameters are studied with 3D simulations.

Device simulator includes the appropriate models for band to band tunneling, quantization of inversion layer charge, doping dependency of mobility, effect of high and normal electric fields on mobility, and velocity saturation. The simulator was calibrated against the published results on Junctionless FETs (C.W. Lee *et al.* 2010). After calibration, the device dimensions are brought to the requirements as given in Table-1.

Table-1. Dimensions of the nominal device and their range of values in FinFETs.

Process parameters	Nominal value	Range of values
Gate length (L_g)	30 nm	20 nm - 40 nm
Fin width (W)	10 nm	5 nm - 14 nm
Fin height (H)	10 nm	5 nm - 15 nm
Underlap (L_{un})	3 nm	1 nm - 10 nm
Source/Drain cross sectional area	115.5 nm ²	100 nm ² - 168 nm ²
Oxide thickness (T_{ox})	1 nm	0.5 nm - 2 nm

Fin-taper angle	2 °	0° - 5°
Corner radius	1 nm	0 nm - 2 nm
Hard mask height (HM)	10 nm	0 nm- 100 nm
Fin doping (N_{fin})	2X10 ¹⁹ /cm ³	1.5X10 ¹⁹ /cm ³ - 3X10 ¹⁹ /cm ³

2.3 Simulation methodology

The RF non-quasi-static delay in the devices is studied using transient simulation. To evaluate the small signal response, a small time varying ac signal along with a DC bias is applied to the gate. The delay between the applied gate signal and drain current is measured to get the NQS delay. The intrinsic gain can be defined as the product of trans-conductance (g_m) and output resistance (R_o). Noise simulation in SDEVICE is a standard AC simulation with noise models included in the physics section. The results from the noise simulation are used to extract the noise figure which is given by

S_S^I is the current noise spectrum of the noisy source admittance and is given by

$$NF = 1 + \frac{1}{S_S^I} \left\{ S_I^{gg} + |\alpha|^2 S_I^{dd} - 2 \operatorname{Re}(\alpha S_I^{gd}) \right\} \quad (1)$$

$$\alpha = \frac{Y_S + Y_{11}}{Y_{21}} \quad (2)$$

$$S_S^I = 4k_B T \operatorname{Re}(Y_S) \quad (3)$$

S_I^{gg} and S_I^{dd} are the noise current spectrums, at the gate and drain terminals respectively, S_I^{dg} is the cross-correlation noise spectra between the drain and gate terminals, Y_{11} (i.e. Y_{gg}) and Y_{21} (i.e. Y_{dg}) are the respective admittance parameters.

3. RESULTS AND DISCUSSIONS

3.1 Impact on NQS delay

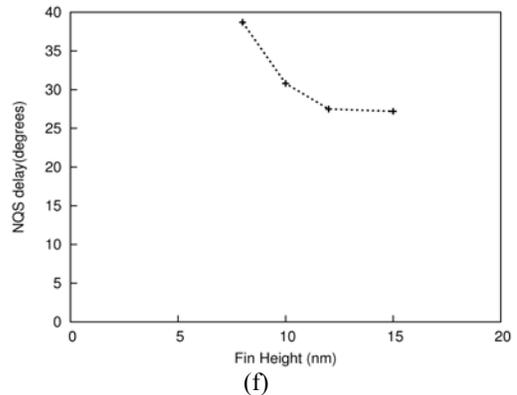
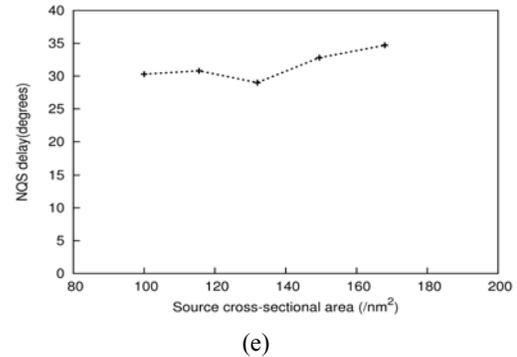
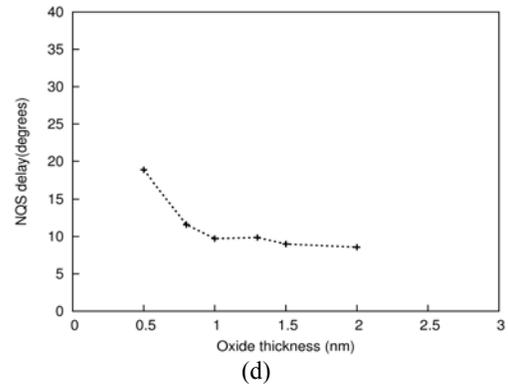
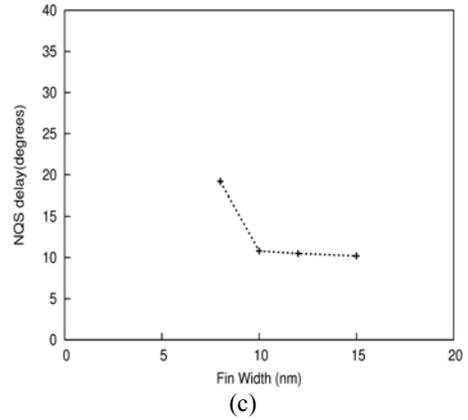
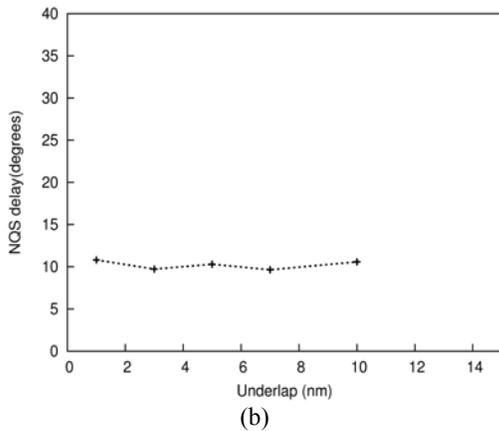
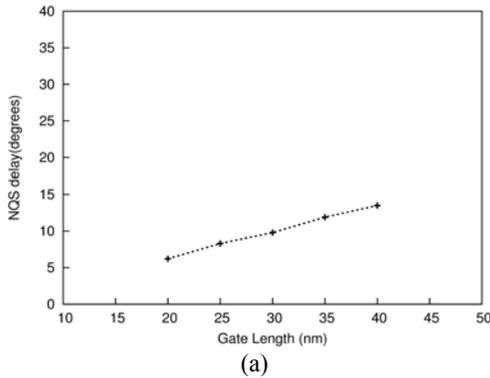
The ten different process parameters are varied one at a time, according to the range given in Table-1 and their impact on NQS delay is studied in this section. NQS delay is extracted as discussed in Section 2.3 at a frequency of 200 GHz. To reason out the simulation result, the expression given by Allen et al (F.L. Allen *et al.* 2002) is used. For a particular NQS delay, the NQS frequency (f_{NQS}) is given by



$$f_{NQS} = \frac{\alpha \mu_{eff} (V_{GS} - V_T)}{2\pi L_g^2} \quad (4)$$

where α is the fitting parameter depending on the accuracy required for the simulation to an NQS event, μ_{eff} the mobility, V_{GS} the gate bias and V_T the threshold voltage of the transistor.

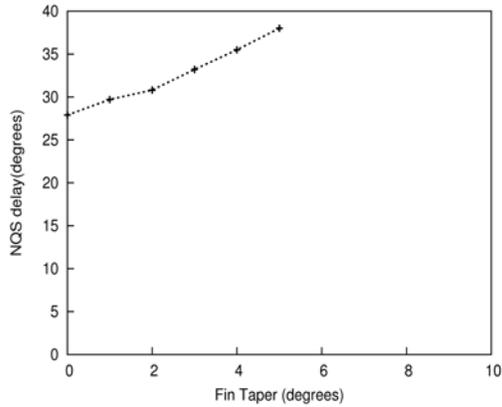
Figure-3 shows the variation of NQS delay (extracted at 200 GHz) with respect to various parameters. Figure-3 (a) shows the variation of NQS delay with respect to L_g . It can be seen that the delay increases with respect to L_g . Equation 4 predicts that as L_g increases f_{NQS} decreases i.e. for the given frequency NQS delay increases. Figure-3(b) shows the variation of NQS delay with respect to L_{un} . It can be observed that the delay is almost constant. Delay is more significant with respect to fin width, fin height and fin taper. For all other geometrical parameters, the device has the least significant delay. The doping parameter is almost insignificant to the delay.



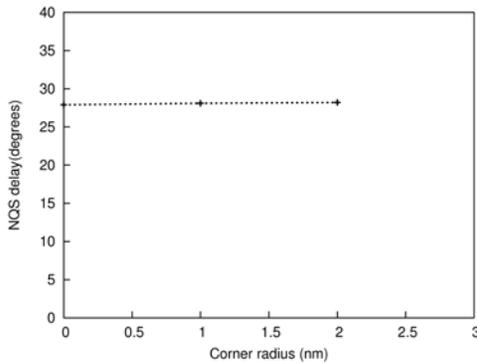


3.2 Impact on intrinsic gain

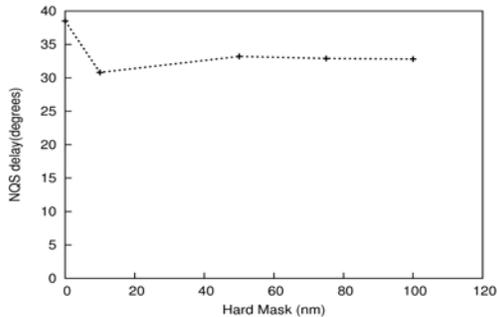
The different structural and doping parameters are varied one at a time, according to the range given in Table-1 and their impact on intrinsic gain is studied in this section. Since intrinsic gain depends on both g_m and R_o , their combined behavior brings the increasing or decreasing tendency with respect to the parameter variation. In the studied region, R_o dominates and decides the trends seen in the Figure-4. For all the geometrical parameters except under lap, source/drain cross sectional area, corner radius and hard mask height, intrinsic gain affects significantly. Here the fin doping is a significant parameter.



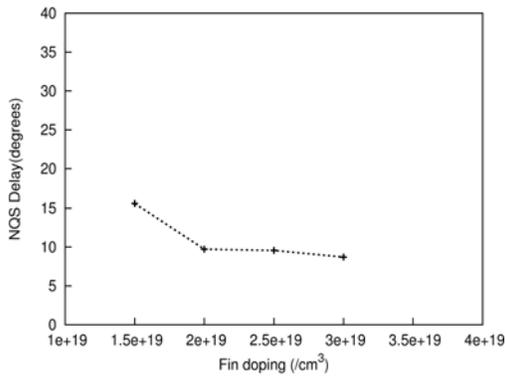
(g)



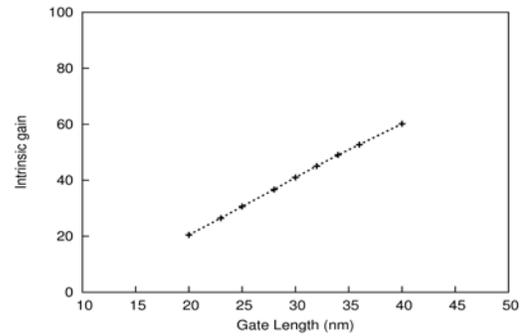
(h)



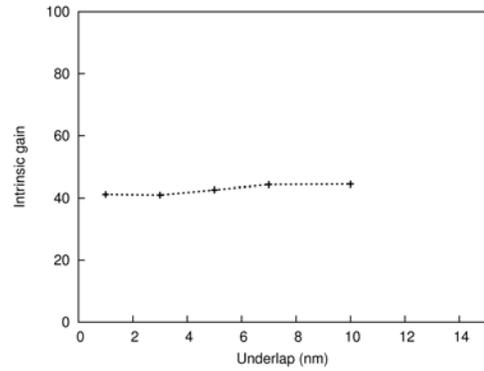
(i)



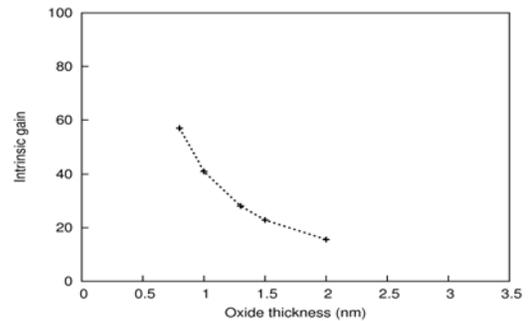
(j)



(a)



(b)



(c)

Figure-3(a)-(j). NQS delay versus structural and doping parameters.

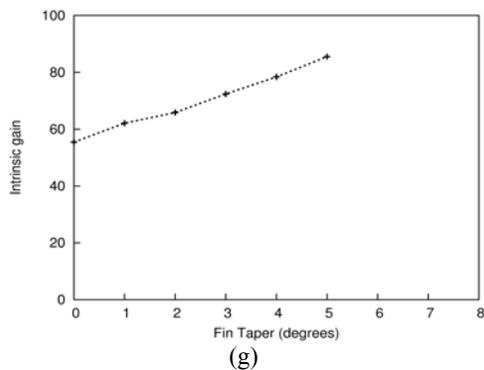
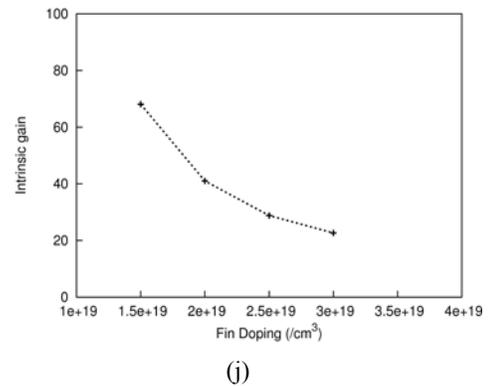
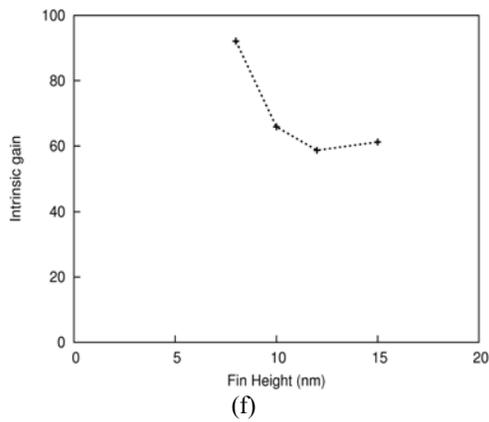
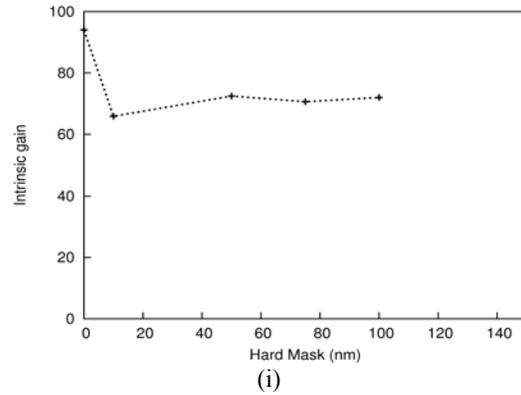
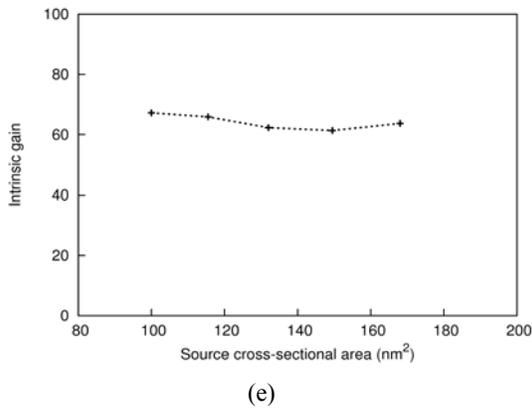
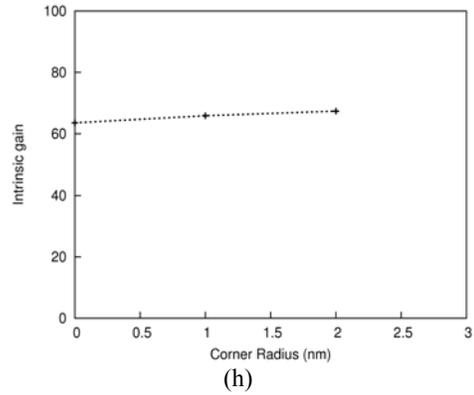
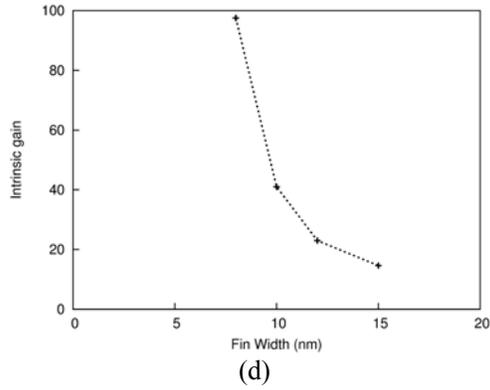


Figure-4(a)-(j). Intrinsic gain versus structural and doping parameters.

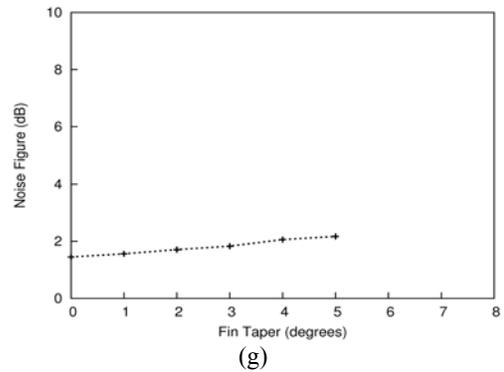
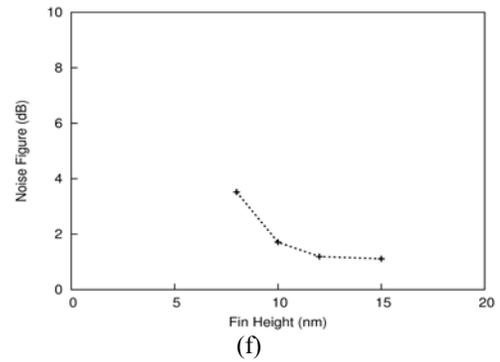
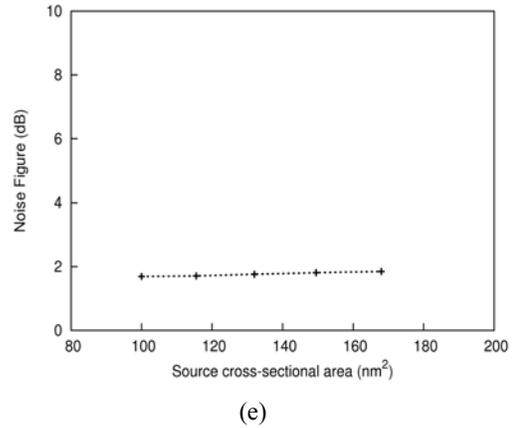
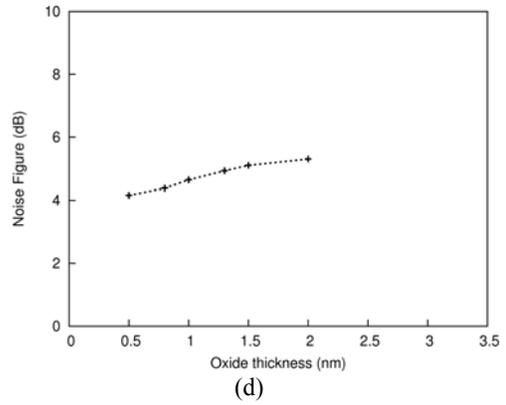
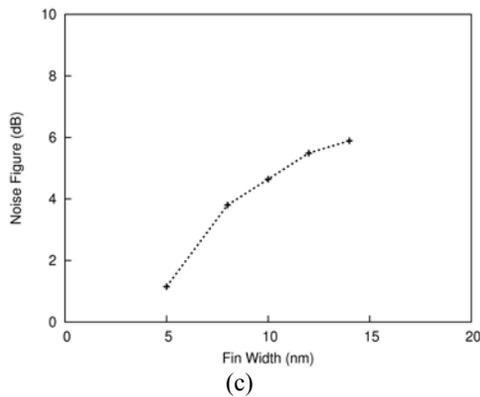
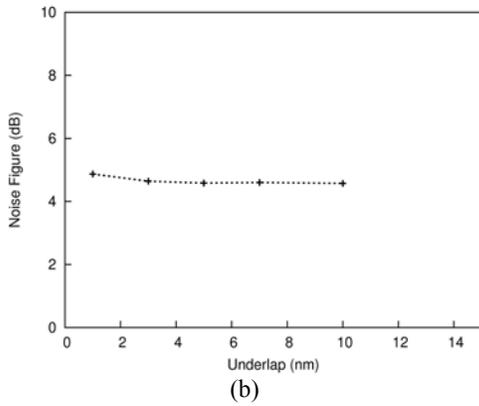
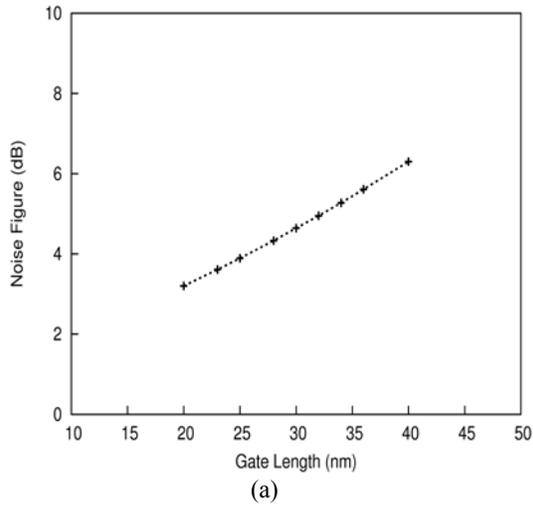
3.2 Impact on noise figure

In this section the parameters are varied one at a time, according to the range given in Table-1 and their impact on noise figure is analyzed. NF is extracted using the Equation 1 as discussed in Section 2.3, at a frequency of 10 GHz. The results can be reasoned out using the following expression which relates the noise figure and f_t .

$$NF = 1 + \left(\frac{f_0}{f_t} \right) K \tag{5}$$



where f_o is the resonant frequency, f_t is the unity gain frequency and K is the noise factor scaling coefficient. It can be observed from Equation 5 that NF is inversely proportional to f_t and so the trends of various parameters with respect to noise figure. This can be evidently seen from our previous results (B. Lakshmi *et al.* 2013)



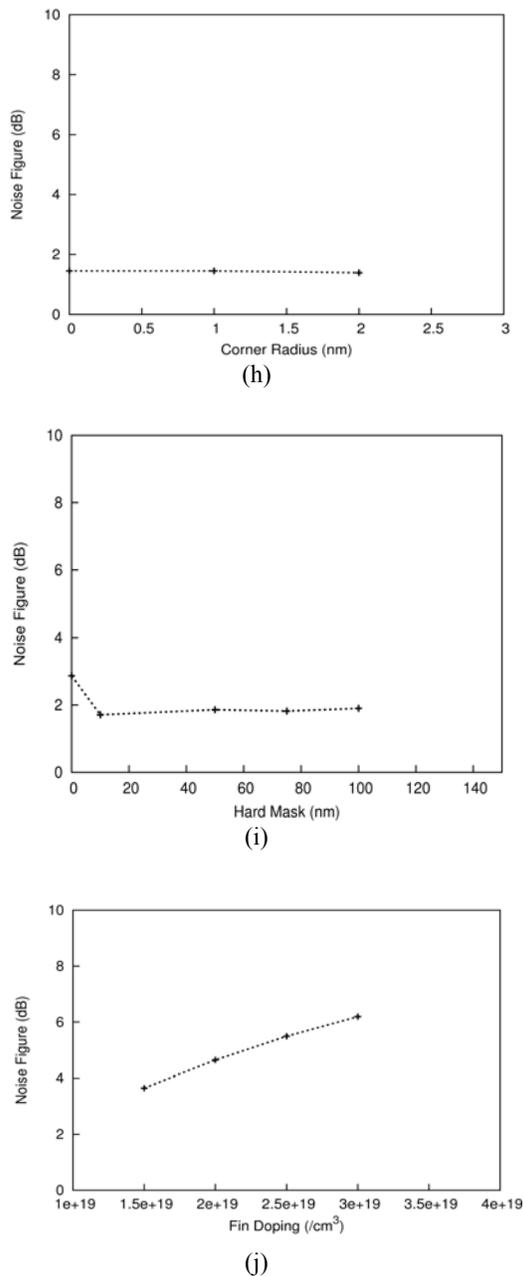


Figure-5(a)-(j). Noise figure versus structural and doping parameters.

4. CONCLUSIONS

In this paper, Junctionless FET is studied for structural and doping parameter variation. Nine structural and one doping parameter are taken as input and their effect on NQS delay, intrinsic gain and noise figure have been studied. The inputs are varied over a wide range to understand the general behavior. It has been found that gate length, fin width, and fin doping were the most significant parameters with respect to NQS delay, intrinsic gain and NF. The least significant parameters are

underlap, gate oxide thickness, source/drain cross sectional area, fin taper, corner radius and hard mask height.

ACKNOWLEDGEMENTS

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