



BANG OF LER AND RDF IN CMOS DEVICES

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ABSTRACT

Device level variability in silicon double gate lateral Tunnel Field Effect Transistors (TFETs) due to Line Edge Roughness (LER) and Random Dopant Fluctuation (RDF) is researched for designs with a 20 nm gate length and body width of 5 nm. Variability in TFET threshold voltage (V_{th}), on state drive current (I_{on}), off state leakage current (I_{off}) and sub threshold swing is examined by means of statistical technology computer aided design (CAD) simulations with forethought of body LER likely 1 nm in amplitude as well as RDF for body heights ranging from 10 to 40 nm. The effects of body Line-Edge Roughness (LER) and Random Dopant Fluctuations (RDF) are found to be alike in magnitude and also comparable to those in identical designed Fin FETs, with the uncommonness of Ion variability which is roughly three times higher for TFETs. Arguments are submitted to explain these research based on the operating principle of TFETs be like to standard metal oxide.

Keywords: Line Edge Roughness (LER), Random Dopant Fluctuation (RDF), CMOS devices.

1. INTRODUCTION

Our world of PCs, tablets and smart phones has grown because of one remarkable trend: the relentless miniaturization of the metal-oxide-semiconductor field-effect transistor or MOSFET. This device, which is the building block of most integrated circuits, has shrunk a thousand fold over the past half century, from tens-of-micrometers scale in the 1960s to tens of nanometers today. But now this steady progress is under threat. And at the main of the problem lies quantum mechanics. The main objective of this paper is to find out the variability impact of LER and RDF on Tunnel Field Effect Transistor. MOSFET is most commonly used component in electronic devices today. It is used in low power devices such as processor, microcontrollers, in order to reduce the chip size and also the operating speed. But as the size of the chip is reduced more and more MOSFET shows high variability's and it is found that the size of the channel cannot be reduced more than 30 nm. Whereas, a new component Tunnel FET is being examined for much smaller channel length i.e. 20 nm or less. Tunnel FET consumes much less power than MOSFET and also occupies lesser area. During fabrication of any IC some variability gets introduced in the chips randomly. These variability's are highly undesirable and can degrade the performance of the component. This paper presents these variability's on Tunnel FET. The variability's are Line Edge Roughness (LER) is the modification of a feature edge from a smooth, ideal shape i.e. the edge deviations of a feature that occur on a structural scale little than the immovability limit of the imaging tool that was used to print the feature. Random Dopant Fluctuation -Random Dopant Fluctuation (RDF) is a form of process variation resulting from variations in the implanted impurity concentration. In MOSFET transistors, RDF in the channel region can adapt the transistor's properties, especially

threshold voltage. In latest process technologies RDF has a wider effect because the total number of dopants is fewer and the addition or deletion of a few impurity atoms can significantly adapt transistor properties.

1.1 Variability

Variability can be defined as the study of how the statistical variations in the design parameters, affect the performances of a large ensemble of devices. Sources of variability can be generally distinguished into extrinsic and intrinsic ones; the former mainly consisting of deterministic type of variations shown from chip-to-chip or wafer-to-wafer, due to strain induced and layout induced changes between devices; the latter being concerned with statistical fluctuations from the design parameters induced by processing steps and/or by the nature of the particular phenomena of interest, that can be described only with statistical methods. This paper is focused on a particular type of variability due to the fluctuations induced by the random placement of dopant atoms in the channel region. This analysis is commonly referred to as variability from RDF and LER. The variability's can be either intrinsic or extrinsic based on the place where they are being introduced. Intrinsic variability's are much difficult to remove than the extrinsic variability's.

1.2 Line Edge Roughness (LER)

When modification in the width of a resist feature happens quickly over the length of the feature, this modification is called line width roughness. When examining these variations along just one edge it is called Line Edge Roughness. LER becomes important for feature sizes on the order of 100 nm or less and can become a significant source of line width control problems for features below 50 nm. LER is caused by a number of



statistically fluctuating effects at these minimum dimensions a specific as shot noise (photon flux variations), statistical distributions of chemical species in the resist such as photo acid generators, the random walk nature of acid diffusion during chemical amplification and the non-zero size of resist polymers being dissolved during development. It is unclear which process or processes dominate in their contribution to LER. LER is usually characterized as the 3σ deviation of a line edge from a straight line, though a more absolute frequency analysis of the roughness can be valuable as well. The impact of LER on device performance depends on the specific device layer and specific aspects of the device technology. For lithography generations below 100 nm, typical specifications for the 3σ LER are about 5% of in effect on CD. It is possible that LER will become the main limiter of CD control below 65-nm production. LER is highly undesirable factor in any component. The roughness along the gate or body will cause wide variations in characteristics of any component from its ideal structure.

1.3 Random Dopant Fluctuation (RDF)

RDF is a form of process resulting from modification in the implanted impurity concentration. In MOSFET transistors, RDF in the channel region can modify the transistor's properties, especially threshold voltage. In newer process technologies RDF has a lot of effect by the reason of the total number of dopants is fewer and the addition or removing a less number of impurity atoms can decidedly alter transistor properties. RDF is a regional form of process variation, meaning that two neighboring transistors may have significantly various dopant concentrations. RDFs are produced by the placement of dopant atoms in channel occurring in implantation steps. Accordingly, RDFs will affect the device performance in the sense that they will show changes in their I-V characteristics due to different current transport occurring in each channel.

2. RELATED WORKS

Junction less FinFET variability due to RDF was investigated for sub 32 nm technology generations using TCAD simulations. Results indicate that variations in threshold voltage, drive current, leakage current and drain induced barrier lowering are heavily impacted by RDF for Junction Less FinFET (JL-FinFETs) with sufficiently high channel doping (greater than 10^{19} cm^{-3}). Unexpectedly, the RDF impact is found to be less severe for finer technology generations, although the overall magnitude is still significant compared to LER induced variability. Using TCAD simulations, it is shown that RDF can be a major source of variability in nanoscale JL-FinFETs. When the devices are scaled from 32 to 15 nm technology nodes, the RDF impact on device variability is alleviated to a small extent, even though the overall variations remain high compared with inversion-mode technology. Given their inherent susceptibility to RDF—other variability sources notwithstanding—implementing JL-

FinFETs at sub-32-nm generations in circuits requiring precise matching may prove challenging [1].

It has been investigated that the variability impact of LER on inversion mode and JL-FinFETs was designed 2009 ITRS high-performance logic 32, 21 and 15 nm nodes used an TCAD simulations. Fluctuations in threshold voltage (V_{th}), drive current (I_{on}), leakage current (I_{off}), sub threshold swing and DIBL were found to be decidedly poor in junction less device comparing to IM devices at Root-Mean-Square LER amplitudes up to 1nm. It has been invoked that a simple physical argument to explain these findings depend on the operating principles of IM and junction less devices and the particularly that means by which LER affects both device architectures. The findings show that JL-FinFETs are inherently more sensitive to variability than standard IM devices and will pose significant challenges as a feasible post CMOS technology [2].

The impact of LER on the variability of IM and JL-FinFETs has been explored using TCAD simulations. The results indicate that JL-FinFETs were more significantly impacted by Fin LER than equivalent IM-FinFETs and attributed this to a different conduit by which LER affects device performance and operation for junction less devices. On this basis, Nano scale JL-FinFETs may have difficulty competing against IM-FinFETs in an extremely variability prone era. [3].

In our project, we cultivate an evaluation framework to assess variability in nanoscale IM and JL-FinFET due to Line Edge Roughness and Random Access Memory design and large-scale digital circuits. From a device-level perspective, JL-FinFETs are acutely impacted by process modification: up to 40% and 60% fluctuation in threshold voltage is noticed from LER and RDF. Conversely results show that variability indeed shifts and broadening of timing and power in large-scale digital circuits are not significant and can be accommodated in the design budget. We find that LER has a more impact on static noise margin analysis of 6T SRAMs required values for SRAMs using JL devices reach up to 2 times those implemented in conventional IM technologies. The earning of JL SRAM is completely compromised in the presence of realistic levels of LER and RDF. Fortunately, the impact of variability is somewhat reduced with scaling for JL designs: both LER and RDF induce less variation for 15 nm mode compared with the 32 nm mode. The observed reduction in with technology scaling suggests that digital circuits implemented with JL FinFETs may eventually offer the same level of operability as those based on IM FinFETs, especially in the presence of circuit level SRAM robustness optimization's.(3)..Investigations on device variability for three different emerging FET technologies are performed to determine the statistical dependence or independence of LER and RDF variability mechanisms. The device candidates include standard IM-FinFETs JL-FinFETs and TFETs designed for sub 32 nm generations. Using TCAD simulations, extracted standard deviations in linear and saturation threshold voltages (V_{thsat} and V_{thlin}), ON-state current (I_{on}), OFF-state



current (I_{off}), sub threshold swing and DIBL are compared for the case 1: when LER and RDF are separately modeled during device simulations and assumed to combine in an uncorrelated fashion; case 2: when LER and RDF are simultaneously modeled in device simulations and assumption is made about their interaction. After performing the comparisons for each FET technology, we find that LER and RDF cannot be considered independently for IM-FinFETs and TFETs but can be for JL-FinFETs. The different outcomes are related to local versus distributed variability dependencies in each transistor type. Our conclusions reinforce the need for more comprehensive treatment of variability effects to provide accurate estimations of expected device variability in junction based FETs.[4]. The Metal Oxide Semiconductor Field Effect Transistor (MOSFET, MOS-FET, or MOS FET) is a transistor used for amplifying or switching electronic signals. Although the MOSFET is a four-terminal device with source (S), gate (G), drain (D) and body (B) terminals which is shown in Figure-1. The MOSFET is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common.

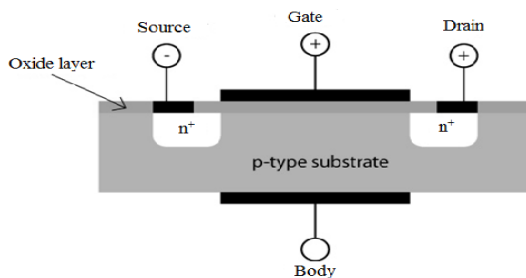


Figure-1. Structure of MOSFET.

The electron has a good ability to penetrate barriers; this phenomenon is known as quantum tunneling. As chip designer have squeezed ever lot transistors onto a chip, transistors has achieved smaller and the distances between different transistor regions have decreased. So today, electronic barriers that were once thick enough to anticipate current are now so thin that electrons can barrel right through them. Chip designer have already stopped thinning one key transistor component, the gate oxide. This layer electrically uncouples the gate. More charge in the channel can be induced by making the oxide thinner, current gets boosted and transistor becomes faster. The oxide thickness cannot be reduced to much less than roughly a nanometer. Beyond this too more current will flow transversely the channel when the transistor is OFF, when initially no current should flow at all. And that is just one of several leakage points. It has been hard to pin down the precise year when size reductions will end. Industry road maps now project the main attraction of the MOSFET out to 2026, when gates will be just 5.9 nanometers long, about a quarter the length they are today. But even then there is a need to find a alternate for the

MOSFET soon to continue getting the performance improvement that is needed

2.1 Operation of MOSFET

Enhancement mode MOSFETs are the common switching elements in most MOS logic families. when the gate–source voltage v_g is zero the device are OFF and can be turned on by pulling the gate voltage in the direction of the drain voltage; that is, approx. the VDD supply rail, which is positive for NMOS logic and negative for PMOS logic. In a depletion mode MOSFET, at zero gate–source voltage, the device is in on state. Such devices are used as load resistors in logic circuits (in depletion-load NMOS logic). For N-type depletion-load devices, the maximum threshold voltage might be about $-3V$, so it could be turned off by pulling the gate $3V$ negative (the drain, by comparison, is more positive than the source in NMOS). The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals. Figure-2 explains the different modes of operation in MOSFET. i) Cut-off, sub threshold or weak-inversion mode

When $V_{gs} < V_{th}$

ii) Saturation or active mode

iii) Triode mode or linear region

When $V_{gs} > V_{th}$ and $V_{ds} < (V_{gs} - V_{th})$

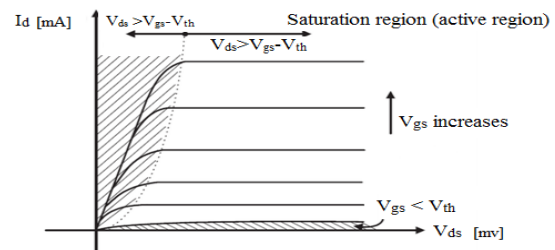


Figure-2. Modes of operation of MOSFET.

2.2 Advantages of MOSFET

Over the rear most few years MOSFETs have become the default choice of power switch for many power management circuit designers. MOSFET technology is preferred due to its thin size, reduced leakage and improved power consumption characteristics. Earlier trends in VLSI include BJTs, FETs show a number of limitations as compared to MOSFET. MOSFET is preferred over BJT because of the following reasons: i) allay of scaling: MOSFET drain current based on the ratio its geometry W/L . So, MOSFET drain characteristic is the same as far as ratio of W/L is kept at the same value. According to theory MOSFET with $W/L=4/2=2/1$ will have same characteristics. In BJT current is not directly dependent on its geometry. So it is easy to scale down MOSFET distinguished to BJT. So, there are many transistors in smaller area i.e. more functionality lesser area can be implemented. ii) reduced power: MOSFET logic consumes low power compared to BJT. Complementary logic in MOS gives zero static power



dissipation though it is not practically true. BJT have much higher power consumption.iii) Fabrication process: MOSFET have simpler fabrication process compared to BJT. BJT have much complex fabrication process which includes buried layer diffusion.

2.3 Impact of LER and RDF on MOSFET

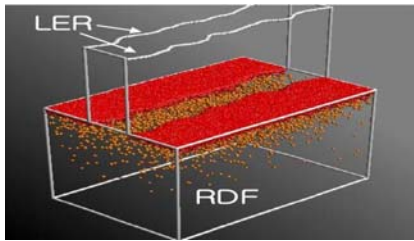


Figure-3. LER and RDF on MOSFET.

Figure-3 shows nano-scale MOSFET with gate line edge roughness across the width of the transistor, randomly placed dopants in source/drain and channel regions. LER affects the electrical performance of bulk devices like MOSFET. The off-state leakage current is greater sensitive compared to the on-state drive current to gate LER. Also, the high frequency LER can spermicide to decrease in effective channel length by improve lateral diffusion of the self-aligned source/drain extension. Low frequency LER causes local CD variation simply due to the statistical variation of average CD in a finite width sample.

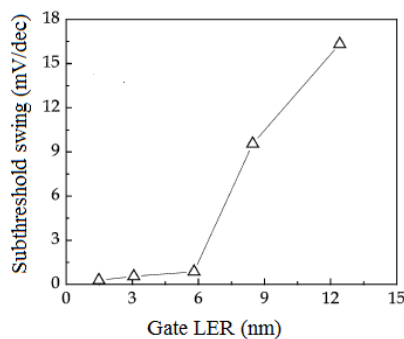


Figure-4. LER variability in MOSFET with respect to sub threshold swing.

Sub threshold swing is obtained below the threshold point where the device starts conducting in off state. When MOSFET experiences LER effect, the channel width from source/drain side shrinks leading to fast flow of electrons. As a result the sub threshold slope increases .RDF is an arrangement of process variation resulting from variation in the implanted impurity concentration. In MOSFET transistors, RDF in the channel region can alter the transistor's properties, especially threshold voltage. In newer process technologies RDF has a larger effect because the total number of dopants is fewer and the addition or deletion of a few impurity atoms can

significantly alter transistor properties. RDF is a local form of process variation, meaning that two neighboring transistors may have significantly different dopant concentrations. The trigate bulk MOSFET structure is more robust to RDF than a planar bulk MOSFET structure with identical nominal body and source/drain doping profiles and layout width. The effects of body RDF (versus source/drain RDF) are dominant. Precise control of the body doping profile is critical for minimizing V_{th} variation in a bulk MOSFET technology. The sub threshold swing of a MOSFET is definite by the diffusion current physics of the device in weak inversion, such that the minimum possible swing in an ideal device is more then 60 mV/dec at room temperature.

2.4 Limitations of MOSFET

Along with many advantages, MOSFET also has some disadvantages. Some of them are:

Short-Channel Effects

The short-channel effects are attributed to two physical phenomena:

- The limitation imposed on electron drift characteristics in the channel,
- The modification of the threshold voltage due to the shortening channel length.

In particular five different short-channel effects can be distinguished:

- drain-induced barrier lowering and punch through surface scattering
- velocity saturation
- impact ionization
- hot electrons

3. PROPOSED SYSTEM

3.1 Introduction

The investigated device structure is a lateral n-type Tunnel FET in a light silicon layer, alone from the substrate by a dielectric layer. The basic design is a gated p-i-n diode. The tunneling takes place in this device between the intrinsic and p+ regions. Schematics of two of the devices simulated are shown.

Because of heterojunction structure I_{off} (leakage current) is maintained low.

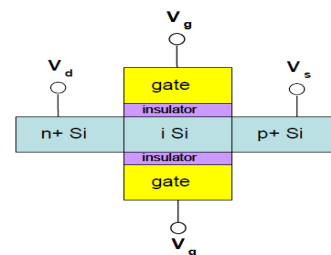


Figure-5. Structure of TFET.

3.2 Device operation

TFET is reverse bias p+ i n+ structure. It operates on the principle of BTBT. The voltage applied to gate causes conduction band and valence band to overlap each



other which leads to tunneling. To operate these devices the p-i-n diode is kept reverse biased, the source is grounded and a positive voltage is enforced to the drain and a voltage is applied to the gate(s). bereft a gate voltage, the thickness of the energy barrier between the intrinsic region and the p+ region is much wider than 10 nm and the device is in the OFF state, as shown in the cross section of the device in Figure-5. As the positive gate voltage increases, the bands in the intrinsic region are pushed down in energy, narrowing the tunneling barrier .Consider a TFET device initially with zero gate voltage and 1 volt drain current. When the gate voltage $V_g=0$ TFET is turned off and there is no operation. When the gate voltage is increased to 1 volt, the device turns on, resulting in transfer of electrons. As the gate voltage keeps increasing the channel width keeps reducing resulting in electron flow from valance band to conduction band.

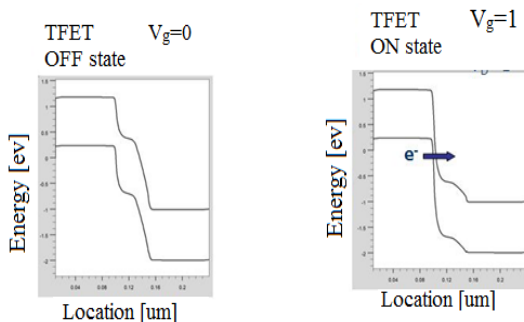


Figure-6. Operation of TFET.

3.3 Impact of LER and RDF on TFET

Device variability on TFET can be seen by the following parameters:

- Drive current (on-current/ I_{on})
- Threshold voltage (V_{th})
- Off-current (Leakage current/ I_{off})
- Sub threshold Swing

3.4. Line Edge Roughness (LER)

LER may occur along the gate line or the body sidewalls, resulting in gate LER or body LER. Body LER results in spatial fluctuation of body thickness, hence the source-channel tunnel junction in a TFET can be significantly affected. LER is caused by a number of statistically fluctuating effects at these small dimensions such as shot noise (photon flux variations), statistical distributions of chemical species in the resist such as photo acid generators, the random walk nature of acid diffusion during chemical amplification and the non-zero size of resist polymers being dissolved during development. It is unclear which process or processes dominate in their contribution to LER. When variations in the width of a resist feature occur quickly over the length of the feature, this variation is called line width roughness. Figure-7 shows the structure of TFET with LER and without LER. Without LER is an idle case of a TFET with a normal flow

of electrons. With LER the variations on the source and drain ends are observed.

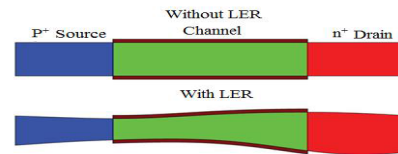


Figure-7. Structure of 20/5 TFET with and without LER.

When examining these variations along just one edge it is called LER. LER becomes important for feature sizes on the order of 100 nm or less and can become a significant source of line width control problems for features below 50 nm. When the gate voltage is applied to TFET the device turns on and the electrons flow from source to drain. But due to LER variation on TFET the source or drain end of TFET shrinks, which causes the concentration to be high in side of shrinking. This causes the device to switch on for low current.

3.5 Random Dopant Fluctuation (RDF)

RDFs are produced by the placement of dopant atoms in channel occurring in implantation steps. Accordingly, RDFs will affect the device performance in the sense that they will show changes in their I-V characteristics due to different current transport occurring in each channel.

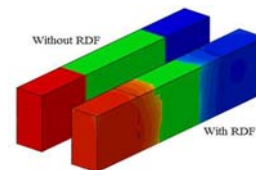


Figure-8. Structure of 20/5 TFET with and without RDF.

Figure-8 shows the ideal and variable case of TFET due to RDF. During the fabrication process the dopant atoms get added in the channel including source and drain. These dopants reduce the size of the channel, resulting to fast tunneling. Fast tunneling reduces the I_{on} . From the data, it appears that LER and RDF exhibit some correlation and that an accurate estimation of TFET variability must account for both mechanisms simultaneously rather than independently. Despite this, separate treatment remains useful to improve our understanding of how these effects impact performance and influence TFET design.

3.6 Advantages of TFET over MOSFET

A TFET is designed as one of the most promising replace to a MOSFET. It is because the Sub threshold Swing of the TFET can be smaller than 60 mV/dec at room temperature, which is the physical limit of the MOSFET. However, the TFET has suffered from smaller on current (I_{on}) than the MOSFET at the same channel length (L_{ch}). It is originated from the fact that the sub threshold swing of the TFET is a function of the gate



voltage (V_{gs}) unlike that of the MOSFET and the physical reason is the large tunneling barrier. TFETs are immune to short channel effects because to their low I_{off} , TFET uses the principle of band to band tunneling for operation. MOSFET use quantum tunneling mechanism. Tunnel FETs operate by tunneling through the source drain barrier other than apply over the barrier two required conditions:

- i. Thin enough barriers over a large enough area for effective tunneling.
- ii. Sufficient density of states on both the transmission and receiving sides to feed energetic locations for the carriers.

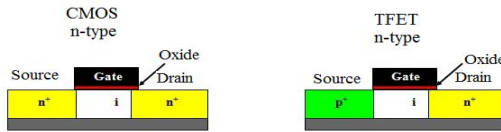


Figure-9. Comparison of MOSFET and TFET single gate n-type structures.

The oxide thickness of MOSFET cannot be reduced to much less than a nanometer. Beyond that, too much current will flow across the channel when the transistor is OFF. If the size is further shrinking, the sub threshold leakage current and gate oxide leakage is high.

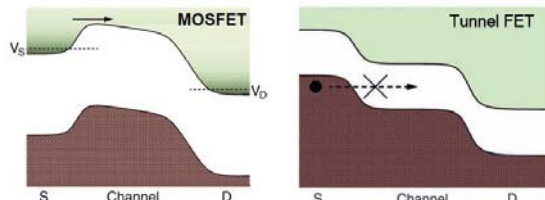


Figure-10. BTBT in TFET and Quantum tunnelling in MOSFET.

In TFET the electrons flow through the barrier but in MOSFET the electrons flow above the barrier. In MOSFET as V_g is applied, the barrier is lowered from source to drain. Figure-10 explains quantum tunneling and BTBT in MOSFET and TFET respectively. When the gate voltage applied increases the barrier is lowered from source to drain in MOSFET, exponential increase in drain current as a function of gate voltage is observed.

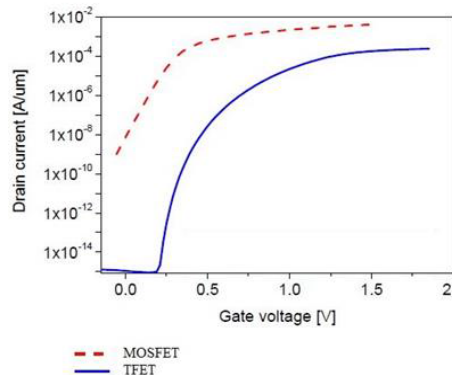


Figure-11. Comparison of sub threshold swing of MOSFET and TFET.

Figure-11 shows the sub threshold swing of TFET and MOSFET. The dimensions of TFET and MOSFET are considered to be same. The TFET swing is observed to be much steeper (closer to off-state) than that of MOSFET. Also, I_{off} (leakage current) is much lower for TFET.

4. RESULTS AND DISCUSSIONS

MOSFET and TFET device variabilities are simulated with respect to the ideal case in Silvaco TCAD tool.

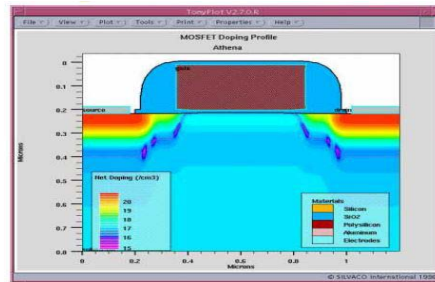


Figure-12. Simulated MOSFET structure without variability.

MOSFET is fabricated from the scratch in the TCAD tool using ATHENA and is simulated using ATLAS.

The following figures shows the Simulated TFET structure using TCAD

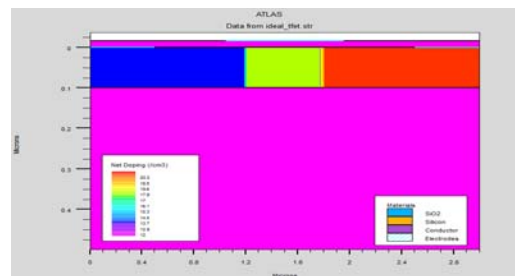


Figure-13. Ideal TFET structure.

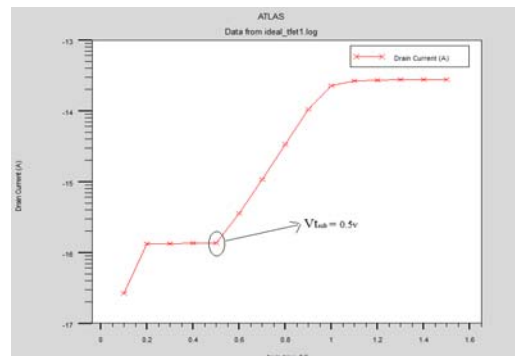


Figure-14. Subthreshold voltage in ideal TFET.

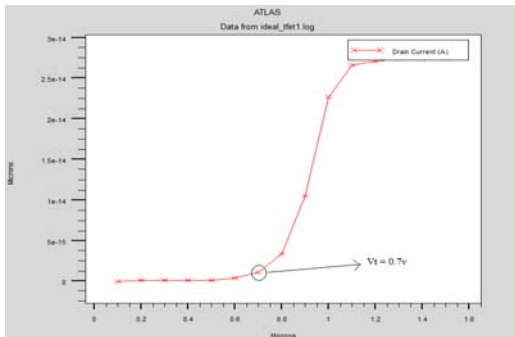


Figure-15. Threshold variation in ideal TFET.

The following figures show the simulated TFET results and LER variability.

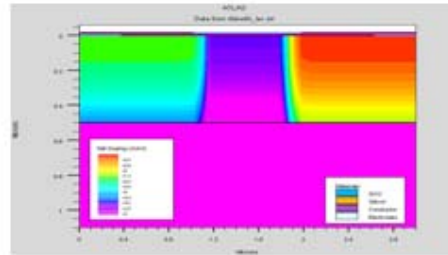


Figure-19. Structure of TFET with LER variability.

4.1 Simulated TFET results with RDF variability

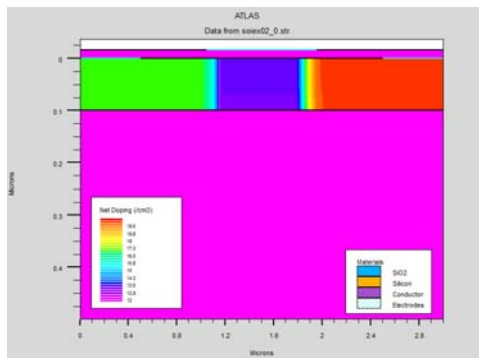


Figure-16. Structure of TFET with RDF variability.

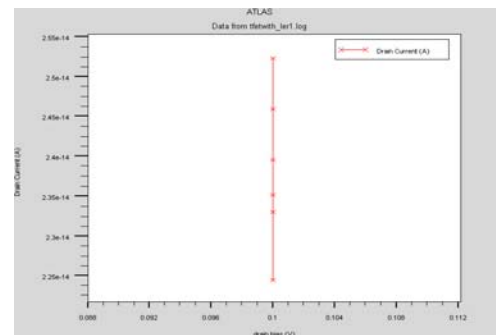


Figure-20. Subthreshold Swing measurement of TFET (LER).

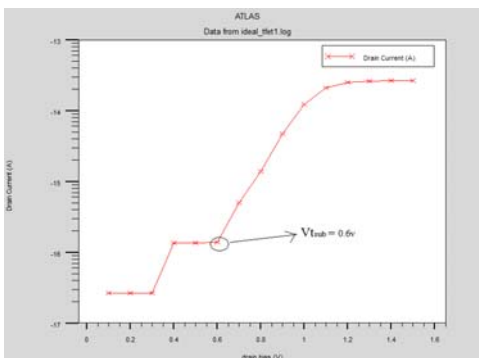


Figure-17. Subthreshold Swing measurement of TFET (RDF).

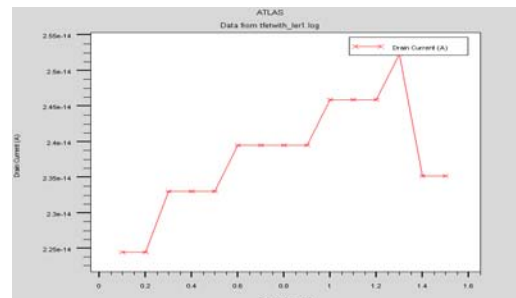


Figure-21. Measurement analysis of the gate to drain voltage with respect to threshold voltage variation (LER).

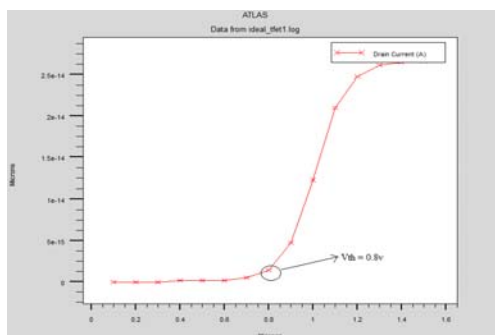


Figure-18. Measurement analysis of the gate to drain voltage with respect to threshold variation (RDF).

4.2 Analysis of simulated results

Figure-12 shows the simulation of MOSFET structure without variability. The ideal TFET structure without any variability with the doping concentration of $e^{17.3} \text{ cm}^{-3}$ in the source region and $e^{19.5} \text{ cm}^{-3}$ in the drain region is shown. TFET structure used is a heterogeneous structure with different concentrations in source and drain. The ideal TFET structure has a sub threshold swing of 44.7 mV/decade as shown in Figure-17 which is much smaller compared to the sub threshold value of MOSFET. Simulated variability impact of RDF on TFETs is shown in Figure-18 for different device heights H ranging from 10 to 40 nm, representing typical values that may be used in actual fabrication. Shorter device heights yield more RDF variability due to the fractionally larger variation in dopant population that occurs in smaller device volumes. Major degradation in



sub threshold swing and threshold voltage variation for TFETs with RDF is present compared to their baseline values. Intuitively, this occurs because the source-channel junction is no longer perfectly abrupt and consequently any increase/decrease in applied gate voltage will have a weaker impact on the peak electric field and tunneling barrier width. This results in weaker gate control of the tunnel barrier as more of the band bending is distributed laterally over the entire channel length rather than localized at the source junction. Figure-18 when compared with ideal TFET structure, it is observed that the channel length is reduced by the addition of RDF effect. The dopants diffuse from source and drain to the channel with their doping concentration. The subthreshold swing effect on TFET with RDF is observed in Figure-8.

Figure-19 describes the TFET structure with LER variations.

Table-1. LER and RDF variations with respect to ideal TFET structure (20/5 TFET).

Variability source (s)	σV_{th} (mV)	σ Subthreshold Swing (mV/dec)
TFET with LER	7.79 %	7.62%
TFET with RDF	5.34%	8.88%

5. CONCLUSIONS

The variability of double-gate silicon TFETs from two common stochastic mechanisms has been investigated through statistical TCAD characterization. LER-induced variation in V_{th} , Ion and subthreshold swing exhibited linear dependencies with σ_{LER} , whereas I_{off} variation appeared exponential versus σ_{LER} . Based on the findings, the contributions from LER and RDF on TFET performance variability will likely require careful treatment prior to use in nanoscale circuit applications.

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