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DESIGN OF SI/SIGE HETEROJUNCTION LINE TUNNEL FIELD EFFECT TRANSISTOR (TFET) WITH HIGH-K DIELECTRIC

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ABSTRACT

In this paper we propose a Si/SiGe heterojunction line tunnel field effect transistor (TFET) with high-K dielectric. The main objective of this device is to increase the ON current. In the case of Si TFETs the ON current is very low. It is because of poor band-to-band tunneling efficiency. This problem can be avoided using heterojunction materials, high-k gate insulators. The device is designed with the source material replaced by SiGe material. The device aims at providing high ON current without compromising the OFF current and sub threshold swing. In this work a heterojunction line tunnel FET is designed using TCAD and the various characteristics of the device are analysed. The device has high ON current of about 2.5mA/μm.

Keywords: TFET (Tunnel field effect transistor),band-to-band-tunneling, ON current, OFF current.

1. INTRODUCTION

Due to aggressive scaling the performance of metal–oxide–semiconductor field-effect transistors (MOSFETs) has degraded. An important figure of merit is the sub threshold swing (SS). It is defined as the change in gate voltage required for a change of an order of magnitude of current from OFF to ON state. The switching speed of a device is determined by SS. The SS of a MOSFET is limited to 60 mV/ dec at room temperature. Thus, without significantly increasing the OFF -state current further scaling down of MOSFET supply voltage is very difficult.

For future generations of integrated circuits, ultra low-power and energy-efficient transistors with SS below 60 mV/decade are required. Efforts have been made to create new devices that can be used for ultra low-power applications. Among such devices tunneling field-effect transistor (TFET) is a promising candidate. Tunnel FETs, are gated p-i-n diodes in which on-current arises from band-to-band tunneling. In TFETs, the carrier transport occurs by tunneling through a barrier instead of diffusion over the barrier as in conventional MOSFETs. Tunneling is a quantum mechanical phenomenon and occurs due to the wave-like properties of electrons on the atomic scale. The probability of transmission through, or tunneling, depends upon the height, width, and shape of the barrier. For the case of n-channel TFETs, tunneling occurs in the source-channel p+n+ junction. When the conduction band of the intrinsic region aligns with the valence band of the P region the band-to-band tunneling occurs and then the electrons from the valence band of the p-type region tunnel into the conduction band of the intrinsic region. The TFET has sub-60 mV/dec subthreshold swing (SS).Due to lower SS they can be used for low power applications[1]–[10]The TFET does not suffer from short channel effects when compared to conventional MOSFET devices due to its built in tunnel barrier. Planar, FinFET, nanowire, vertical structures are present in TFETs. Si, SiGe which are homo and heterojunctions and semiconductor compound of group III–V are used for TFET design [11-14]. Line TFETs are very promising class of TFETs. These devices have the gate placed on top of the source. The tunneling in these line TFETs happens uniformly along the gate length and tunneling will be orthogonal to the gate, thus improving the ON -current and the SS of the device [15]. This paper presents a Tunnel FET which is based on interband tunneling .Tunneling current is a quantum mechanical effect that shows exponential dependence on tunnel width. The ON -state current in Si TFETs is very low due to poor band-to-band tunneling efficiency which is lower than the ITRS requirement. It can be stated that lowering the tunneling gap can be a way to overcome the on current limitation. In order to meet the ITRS requirement, Hetero-structures, materials with low bandgap, high-k gate dielectrics etc. can be used[16-17].One promising method is to use hetero-junction TFET.As a result of this ON current is increased due to reduced tunnel gap in ON state and OFF current is reduced due to increased tunnel gap in OFF state.

In this paper we propose a Si/SiGe hetero-junction line tunnel field effect transistor. The device is designed and simulated using TCAD. The device is compared with another TFET structure with Si as the source material. The ON currents of both the devices are compared. With the proposed device a higher ON current was obtained when compared with other TFET structures.

2. DEVICE STRUCTURE AND OPERATION

Tunnel FETs are gated p-i-n diodes, or less commonly, gated p-n diodes. The transport mechanism in a TFET relies on band-to-band tunneling (BTBT) instead of thermal emission over a potential barrier as in a MOSFET. To switch the device on, the diode is reverse biased, and a voltage is applied to the gate. A reverse bias

is needed across the p-i-n structure in order to create tunneling. To operate NMOS a positive voltages are applied to the drain and gate. The n-region of NTFET is drain and source is the p+ region. On applying sufficient gate voltage the energy bands in the intrinsic region are pushed down and tunneling takes place between the valence band of the p+-region and the conduction band of the intrinsic region.

The structure of a line tunnel FET with Si source is shown in figure 1.The structure consists of Si as drain, intrinsic silicon as channel, HfO_2 as gate oxide and molybdenum as gate. The silicon film thickness (T_{si})=50 nm, gate oxide thickness (T_{ox})=1 nm, channel length (L) = 40 nm and gate work function = 4.5 eV . The structure of a line tunnel FET with SiGe as the source is shown in figure 2. The structure consists of Si as drain, intrinsic silicon as channel, HfO_2 as gate oxide and molybdenum as gate. The figure 2 is designed with the same parameters as Figure-1.The parameters of Figure-2 is shown in Table-1. For N-type, source is doped with P-type material and here Boron is used, intrinsic region and drain is dropped with N-type material and here it is Arsenic is used. The source doping is $10^{19}cm^3$ intrinsic region doping is $10^{17}cm^3$ and drain doping is $10^{20}cm^3$.The simulations are performed using synopsis TCAD.

Table-1. Design parameters of the proposed device.

Parameters	Dimensions
Length of the gate (L_g)	60nm
Gate oxide thickness(HfO_2)	1nm
Doping conc. for source(SiGe)	1e+19
Doping conc. for intrinsic region(Si)	1e+17
Doping conc. for drain(Si)	1e+20
Channel length	40nm
Si channel thickness	50nm

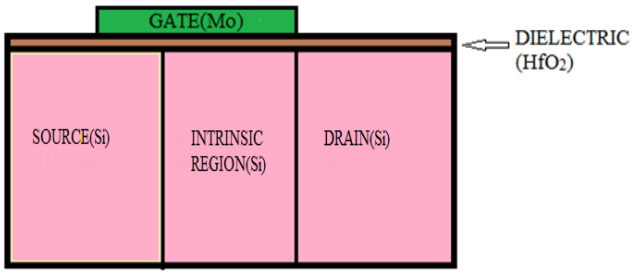

Figure-1. Structure of a line tunnel FET with Si source.

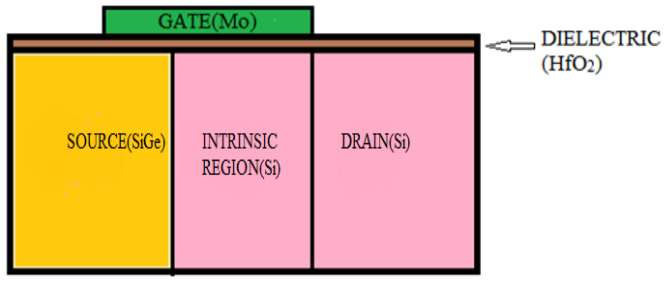

Figure-2. Structure of a line tunnel FET with SiGe source.

The Si tunnel FETs has lower ON current due to poor band-to-band tunneling. To overcome this problem SiGe heterojunction material is used. The heterojunction materials will lower the tunneling barrier in ON state. Thus ON current is increased. Also it increases the tunneling barrier in OFF state thus reduce the OFF current.

3. RESULTS AND DISCUSSIONS

The device is operated by applying gate bias so that electrons are accumulated in the intrinsic region. When sufficient gate bias is applied, band-to-band tunneling occurs. The conduction band of the intrinsic region aligns with the valence band of the P region. At this state tunneling occurs as the electrons from the valence band of the p-type region tunnel into the conduction band of the intrinsic region. Thus current can flow across the device. As the gate bias is reduced, the bands become misaligned and current can no longer flow. Generally the band gap between the valence band of source and conduction band of intrinsic region are close to each other in TFET than conventional MOSFET.

When V_{GS}=2V and V_{DS}=0.5V an ON current of 0.8mA/μm is obtained for the tunnel FET with Si as the source material. The transfer characteristics of the device is shown in Figure-3.For the tunnel FET with SiGe as the source when V_{GS}=2V and V_{DS}=0.5V an ON current of 2.5mA/μm. The transfer characteristic of the device is shown in Figure-4.

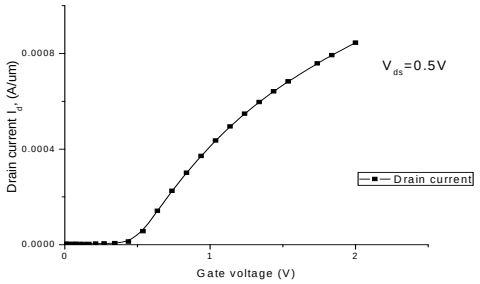

Figure-3. Transfer characteristics of tunnel FET with Si source.

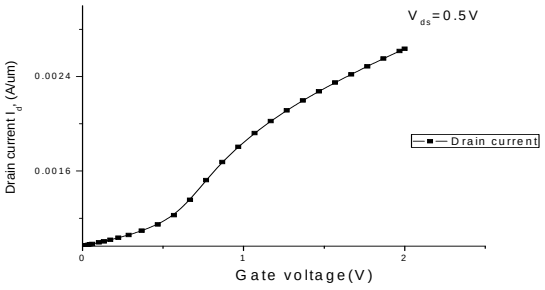

Figure-4. Transfer characteristics of tunnel FET with SiGe source.

On comparing both the devices the device with SiGe source is found to have more ON current. The Si tunnel FET has lower ON current due to poor tunneling efficiency. When SiGe is used the tunneling barrier is reduced and hence more electrons can tunnel through the tunneling barrier which in turn increases the ON current. On comparing the proposed device with another heterojunction line tunnel FET in "[18]" the proposed device is found to have an higher ON current. The existing line tunnel FET has an ON current in the range of 10^{-6}A/µm for a gate voltage of 2V and drain voltage of 0.5V.The proposed device has higher ON current of about 2.5mA/µm at the same voltage conditions.

The output characteristics of the device with Si as the source is shown in Figure-5. The curve is drawn with gate voltages 1.2V, 1.4V, 1.6V, 1.8V, 2V and V_{DS}=2V.As the gate voltage is increased the bands in the intrinsic region are pushed down in energy. The barrier is reduced and the current starts flowing. As a result the drain current increases with the increase in gate voltage .The output characteristics of the device with SiGe as the source is shown in Figure-6 with gate voltages 1.2V, 1.4V, 1.6V, 1.8V, 2V and V_{DS}=1.5V.In this case also as the gate voltage is increased the bands in the intrinsic region are pushed down in energy. The barrier is reduced and the current starts flowing. As a result the drain current increases with the increase in gate voltage.

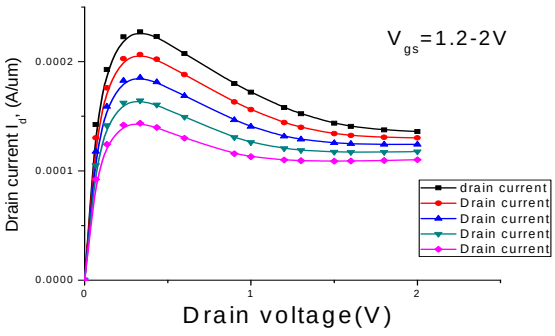

Figure-5. Output characteristics of tunnel FET with Si source.

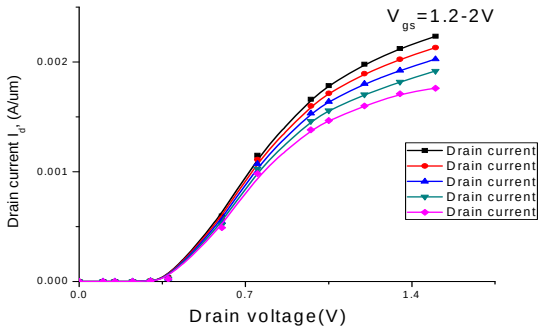

Figure-6. Output characteristics of tunnel FET with SiGe source.

4. CONCLUSION

A line tunnel FET with SiGe at source is proposed and analyzed using 3D device simulations. The proposed device shows orders of improvement in ON current over the conventional TFET. On comparison with tunnel FET with Si as the source, the proposed device with SiGe at the source is found to have high current. The ON current of the proposed device is 2.5mA/µm. TFET devices can be used in future for the digital logic designs at ultra low voltages.

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