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DESIGN AND SIMULATION OF A DUAL MATERIAL DOUBLE GATE TUNNEL FIELD EFFECT TRANSISTOR USING TCAD

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ABSTRACT

High leakage currents and short channel effects become significant enough to be the major concerns for circuit designers as semiconductor devices are miniaturized. Tunnel field effect transistor(TFET) show good scalability and have very low leakage current .These transistors have very low leakage current, good sub-threshold swing, improved short channel characteristics and lesser temperature sensitivity. In this paper a dual material gate (DMG) in a tunnel field effect transistor is proposed in order to optimize ON current and nature of output characteristics. Significant improvement is shown by a TFET if appropriate work functions are chosen for gate material on the source side and drain side. A dual material gate in double gate TFET is applied to show an overall improvement in performance. In comparison with conventional TFET, the proposed model provides a higher ON state current.

Keywords: Tunnel field effect transistor (TFET), Band to band Tunneling, ON state current.

1. INTRODUCTION

Tunnel field-effect transistors (TFETs) exhibit an excellent subthreshold swing and a very low leakage current and hence they are actively investigated for future low-power complementary metal–oxide–semiconductor (CMOS) applications [1]–[15]. However, as TFETs suffer from low ON current, there are various techniques to improve the I_{ON} in a TFET that has been suggested [4]-[14]. The mechanism of current conduction and its saturation in the output characteristics in a TFET are quite different from a conventional MOSFET. As a result, we often find a phenomena of delayed saturation in the output characteristics. This can be detrimental for CMOS applications; therefore, the nature of the output characteristics must be carefully considered while designing TFETs. In addition, the dependence of the drain current on the drain voltage in a TFET is different from that of a conventional MOSFET. Strong drain-induced barrier lowering (DIBL) effects are sometimes a major concern in TFET, and this can severely limit the utility of the device. Therefore, to employ TFET for low-power CMOS applications, it is desirable that, the overall device characteristics of the TFET has to be improved in addition to improving the ON-current and the subthreshold swing. In this paper, the application of a dual material gate (DMG) in a double-gate TFET (DGTFET) is proposed and demonstrated using 3-D device simulations using TCAD and thereby engineering the work functions of the dual gates, it is possible to simultaneously optimize the ON state current (I_{ON}), the nature of the output characteristics, and the immunity against DIBL effects. It has already been demonstrated in the previous works that a conventional DGTFET suffers from an unacceptably low ON state current. Different aspects of DMGTFETs have been studied using TCAD simulations. Therefore, we demonstrate the application of the DMG technique in a DGTFET to not only achieve an improved I_{ON} but also improve the overall performance of the device. It is shown that, by using a DMG, the scalability of the TFET can be extended below 20-nm channel lengths. Finally, considering the potential application of a TFET in low power applications, the suitability of DMG-DGTFET is studied at V_{DD}=1 V. The rest of this paper is organized as follows: Section II describes the structure of a DM-DGTFET, DGTFET and the simulation model used in this study. Section III presents simulation results for a DM-DGTFET and DGTFET and demonstrates the advantages of using a DMG. In this section, the channel length of the device is taken as 20 nm. Finally, Section IV draws important conclusions out of this study.

2. DEVICE STRUCTURE AND SIMULATION MODEL

Figure-1 shows the cross-sectional view of a DGTFET and Figure-2 shows the cross sectional view of the proposed DMG-DGTFET in which both the top and bottom gates are composed of materials with two different work functions. We refer to the gate closer to the source as the tunnel gate and the one closer to the drain as the auxiliary gate. All the simulations have been carried out using TCAD. Since the tunneling process is a nonlocal, the spatial profile of the energy bands and the band-gap

narrowing effects are included. The parameters for the conventional double-gate TFET used in our simulation are: channel region doping N_D =$1\times10^{17}/cm^3$,P^+ source doping N_A =$1\times10^{20}/cm^3$,N^+ drain doping N_D =$5\times10^{18}/cm^3$ and gate work function=4.5 eV . The silicon body thickness (t_{si})=10 nm, gate oxide thickness(t_{ox})=2 nm and channel length(L)=20 nm. The parameters for the conventional DMG-DGTFET used in our simulation are: channel region doping N_D =$1\times10^{17}/cm^3$,P^+ source doping N_A =$1\times10^{20}/cm^3$,N^+ drain doping N_D =$5\times10^{18}/cm^3$ .The gate work function=4.5 eV for auxillary gate and 4.0eV for tunneling gate .The silicon body thickness (t_{si})=10 nm, gate oxide thickness(t_{ox})=2 nm and channel length(L)=20 nm where tunnel gate length (L_{tunn})=10 nm, and auxiliary gate length (L_{aux})=10 nm. The simulation model used in this paper is hydrodynamic mobility model.

The operation of tunnel field effect transistors is entirely different from conventional MOS devices. The analysis of DM-DGTFET operation has been done by considering two separate cases of varying work functions φ_{m1} and φ_{m2} alternatively to get improved I_{OFF} and I_{ON} current.

Case (i): In the OFF-state, there is no band overlap on the source side, when the metal work function φ_{m1} is reduced to 4.0 eV, and hence, the leakage is expected to be quite low. In the ON-state, with the reduction in φ_{m1}, the band overlap increases, and the tunneling width decreases, leading to a significant increase in the tunneling probability on the source side. Hence the electrons tunnel from the valence band of the p-doped source to the conduction band in the intrinsic body and then move towards the n-doped drain by drift diffusion.

Case (ii): In the OFF-state, as φ_{m2} increases, the tunneling width increases, and the band overlap reduces on the source side, leading to a considerable reduction in the OFF-state tunneling probability. In the ON-state, the increase in φ_{m2} does not show any significant change the band diagram. In our model, we assume that the device is operated in the subthreshold region. And there is no assumption made in the

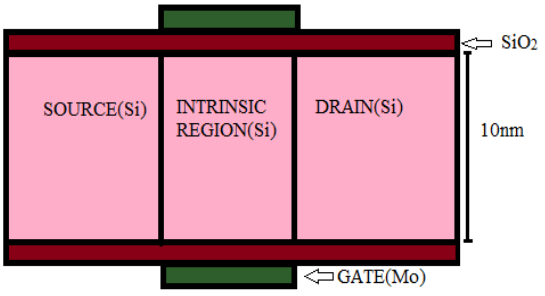

Figure-1. Structure of a DGTFET.

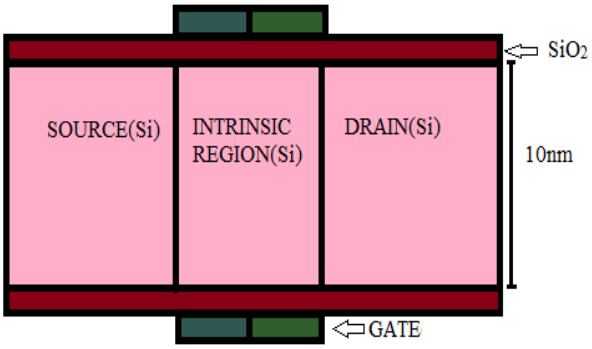

Figure-2. Structure of aDM- DGTFET.

depletion of the source and drain region has been assumed. The only limitation of TFET is the presence of an ambipolar state which means conduction in two directions (i.e. both for positive gate voltage and negative gate voltage).It is caused due to the transfer of tunnel junction from source side to the drain side when the gate voltage $V_{GS}<0$ for an n-type TFET operation. The basic requirement for an ideal switch in digital circuits is to work in only one direction, but if it also starts conducting in other direction this can create a problem in complementary logic circuit applications and thus limits the utility of the device for digital circuit designs.

3. RESULTS AND DISCUSSIONS

TFET has different current-voltage characteristics than that of MOSFET. In conventional MOSFET, diffusion current is dominant in the subthreshold regime where as drift current is dominant in the ON condition. However tunneling current is dominant in TFETs. The device is operated by applying gate bias so that electron accumulation occurs in the intrinsic region. Band-to-band tunneling occurs when the conduction band of the intrinsic region aligns with the valence band of the P region when sufficient gate voltage is applied. Electrons from the valence band of the p-type region tunnel into the conduction band of the intrinsic region and current can flow across the device. As the gate bias is decreased, the bands becomes misaligned and this

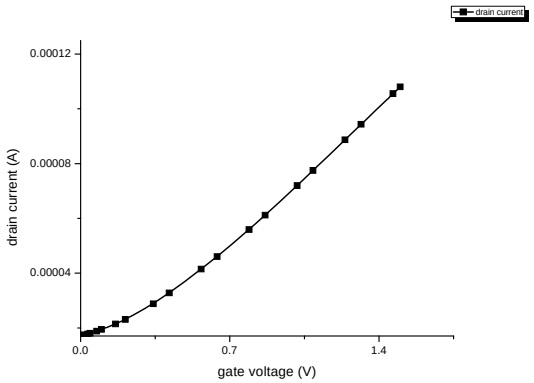

Figure-3. Transfer characteristics of a DGTFET when V_{GS} is 1.5V and V_{DS} is 1V.

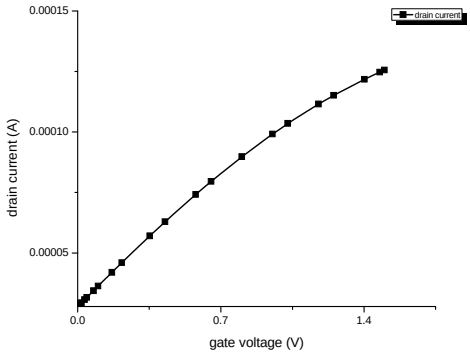

Figure-4. Transfer characteristics of a DM-DGTFET when V_{GS} is 1.5V and V_{DS} is 1V.

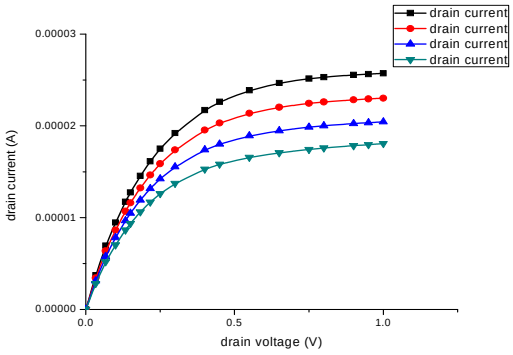

Figure-5. Output characteristics of a DGTFET when V_{GS} is varied from .6-1V and V_{DS} is 1V.

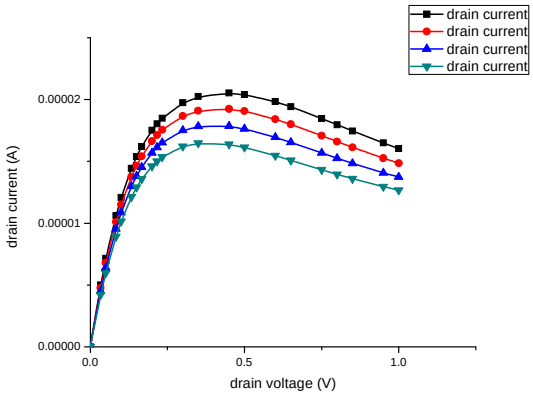

Figure-6. Output characteristics of a DM-DGTFET when V_{GS} is varied from .6-1V and V_{DS} is 1V.

increases the current flow. When V_{GS} is 1.5V and V_{DS} is 1V, the ON state current in the DGTFET is 1.08×10^{-4} A/µm and that for a DM- DGTFET is 1.26×10^{-4} A/µm. The transfer characteristics of the devices are shown in Figure-3 and 4.

In the ON-state, with the reduction in φ_{m1} (4.0eV), the band overlap increases. As a result tunneling width is decreased, leading to a significant increase in the tunneling probability on the source side. Hence the electrons tunnel from the valence band of the p-doped source to the conduction band in the intrinsic body and then move towards the n-doped drain by drift diffusion. In the OFF-state, as φ_{m2} is increased, the tunneling width increases, and this decreases the band to band overlap on the source side, leading to a considerable reduction in the OFF-state tunneling probability. The output characteristics of the devices are shown in Figure 5and 6. As the gate voltage is increased the conduction band of the intrinsic region lowers and the band gap between the valence band of source and conduction band of drain decreases, thus increasing the drain current. The drain voltage V_{DS} is 1V and the gate voltage V_{GS} is varied from .6V to 1V.The saturation region in the output characteristics is due to the tunneling width becoming progressively less dependent on V_{DS} as the drain voltage is increased.

4. CONCLUSIONS

In this paper, we have studied the implications of the application of a DM in a TFET to simultaneously improve the overall performance of the device. The proposed model of a DM-DGTFET gives a higher ON state current as compared to a conventional DGTFET. The ON state current in the DGTFET is 1.08×10^{-4} A/µm and that for a DM- DGTFET is 1.26×10^{-4} A/µm. Using a DM

in a DGTFET will bring further complexity to the device fabrication. In addition to it, fabricating a DMG at a very small device dimension (channel length less than 100 nm) and extending it to below 10 nm may be challenging. However, since there is an appreciable improvement in the overall device characteristics, the complexity in the device fabrication might be acceptable.

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