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# A FULLY DIFFERENTIAL READ-DECOUPLED 7-T SRAM CELL TO REDUCE DYNAMIC POWER CONSUMPTION

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**ABSTRACT**

To improve the performance of an SRAM cell and reduce the area consumption, researchers are scaling down the technology node of MOSFET. But power consumption is not yet improved below 65-nm technology node. Since then the $V_{DD}$ (supply voltage) remains more or less constant and dynamic power consumption improvement is almost stagnated, while leakage current increases exponentially. Hence, prime area of concern of present days circuit is to reduce the power consumption with minimum device size. In this article a fully differential read decoupled 7T SRAM cell is proposed that consumes substantial amount of less read and write power. Side by side it shows 4% (10.57×) shorter read (write) delay and 4×/9.24% improvement in RSNM/WSNM (Read static noise margin/write static noise margin) @ 700 mV.

**Keywords:** read delay, read power, read-decoupled, RSNM, write delay, write power, WSNM.

## 1. INTRODUCTION

As the technology is getting advanced, the performance of microprocessors is improved considerably. But the speed of operation of the memory is not as improved as that of the processor. Therefore, there is a gap between processor and memory in terms of speed of operation. To bridge this gap, on chip integration of semiconductor memory, which is known as cache is developed by silicon industry. The system performance is enhanced by higher on chip integration. SRAM cells are the major area consumer (90%) in present days' NoC (Network-on-Chip) and SoC (System-on-Chip) as mentioned in ITRS 2011 (International technology road map for semiconductor) [1]. The transistor size used in SRAM cell need to be scale-down even bellow 100-nm of technology node to achieve higher integration density. But this scaling down of transistor size, causes variations in device parameter, like threshold voltage (Vt). Crucial design metrics of an SRAM cell, like read stability, write ability and reliability are affected because of variations in device parameters [2]. Conventional 6-T (CON6T) fails to provide its functionality because of this high Vt fluctuations and process variations [3].

CON6T suffers from weak write ability and read instability below 65-nm technology node [4]. Moreover, if an SRAM cell is more stable during read operation, it is more difficult to write on that cell to change the content while writing. Hence, researchers are focusing on modifying conventional 6T SRAM cell to mitigate the above mentioned issues with reduced power in the deep sub-micron or nano range. Different SRAM cell are proposed earlier in the literature [5-7]. To enhance the SNM (static noise margin), fundamental method used in those structures are decoupled read path, cutting the feedback, asymmetric sizing and one sided access. However, it is necessary to design a fully differential structure, which will provide differential output for SA (Sense Amplifier) and augment the stability during read operation [8]. In this paper, a fully differential read decoupled 7-T (FDRD7T) cell is proposed. This paper has following contribution:

1) A fully differential read decoupled 7-T SRAM cell is proposed which performs fully differential read operation. The design metrics of the proposed cell are estimated and compared with CON6T (Figure- 1).
2) Read stability is improved because of the read decoupled scheme. Therefore, the chance of read failure is eliminated.
3) The proposed cell enhances the write ability. Therefore, desired data can be easily written into the cell.
4) The FDRD7T cell consumes less dynamic (read/write) power while achieving shorter read (write) delay.

Monte Carlo simulations are executed using 16-nm PTM (developed by the Nano scale Integrations and Modeling (NIMO) Group at Arizona State University (ASU) ) [9] to investigate design metrics of the SRAM cell and compared with standard 6T SRAM cell.

Further, proposed design is discussed in Section II. Simulation results are discussed and compared in Section III. Finally, concluding remarks are presented in Section IV.

## 2. PROPOSED DESIGN AND DEVICE SIZING

In this article, a 64 byte (16 bit × 32 bit) fully differential read decoupled 7-T SRAM cell is proposed. The proposed design consists of majority of PMOS transistors. PMOS transistors are used because it has an advantage of higher tolerance against radiation. In PMOS, leakage current does not get affected from radiation bombardment, whereas it increases in NMOS [10]. Moreover, PMOS offers lower flicker (1/f) noise than NMOS transistor. In addition shallow trench isolation (STI) offers compressive stress, which causes degradation in mobility of electrons rather than holes nearthe verge of active region.

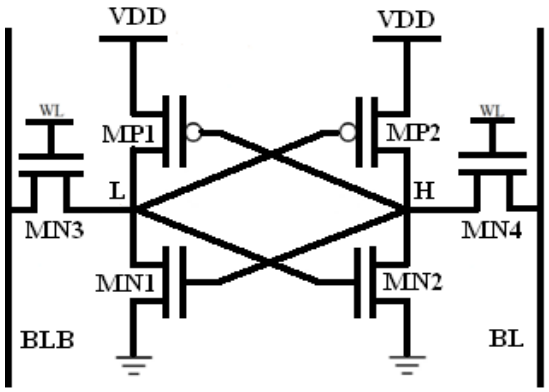


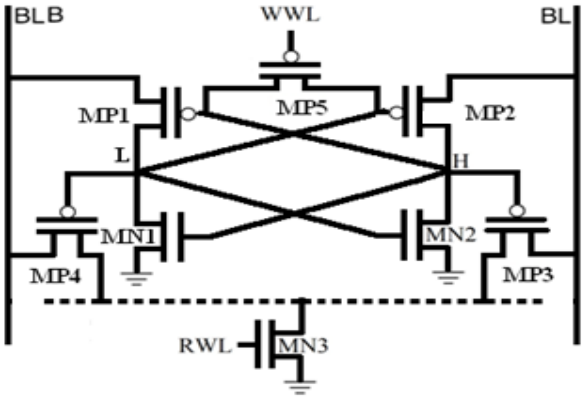

**Figure-1.** Conventional 6T (CON6T) SRAM cell.

In conventional 6-T read current flows from bitline to GND via transistors MN3 and MN1 or MN4 and MN2 depending upon the data stored in the storage nodes. Therefore, a voltage divider will form between MN3 (MN4) and MN1 (MN2). Hence, voltage at zero storage node may increase upto a certain level (beyond the switching threshold (VM) of the other inverter which is holding logic '1') and can flip the cell content.

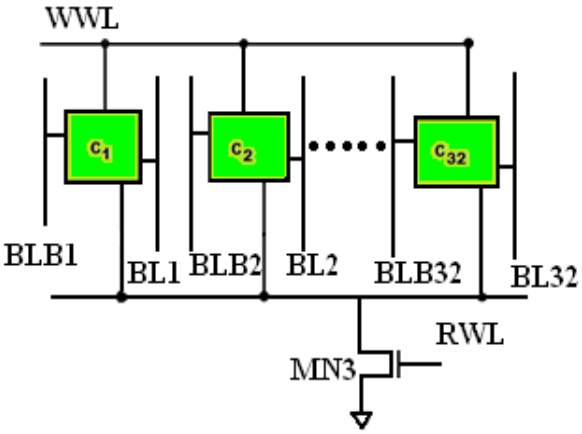
For illustration: let's assume node L is holding logic '0' and H is holding logic '1' (see Figure-1). While reading WL is pulled high and both the bitlines (BL and BLB) are precharged to supply voltage VDD. Hence, both the access transistors MN3 and MN4 will be ON and since H is holding logic '1', transistor MN1 will conduct. Therefore, voltage at BLB will discharge through transistors MN3 and MN1. Hence, a voltage divider will form between MN3 and MN1. Because of the formation of this voltage divider, voltage at node L will increase. If this increased voltage exceeds the VM of the inverter, which is holding logic '1' then the content of the storage node will flip, resulting in read failure.

Therefore, if it is possible to avoid the formation of voltage divider then the problem of read upset can be alleviated. The proposed cell (see Figure-2 (a)) in this article does exactly the same thing. It decouples the storage nodes from their respective bitlines. Read current will flow from bitline to GND via MP3 (MP4) and MN3 depending on the stored data where MN3 is common for the entire row as shown in Figure-2 (b). Therefore, storage nodes do not get affected by the read current. Hence, the problem of read failure is avoided. Finally, it can be said that RSNM of the proposed cell is improved.

A write assist transistor MP5 is incorporated in the proposed cell which will be turned ON during write operation only. Because of this write assist transistor, write ability (WSNM) of the proposed cell will be improved.




(a)




(b)

**Figure-2.** Proposed FDRD7T SRAM cell design (a) cell schematic (b) row configuration.

In conventional 6-T, RSNM and WSNM are two conflicting design metrics which mean if it is desired to improve the RSNM then WSNM will be adversely affected or vice-versa. But in the proposed cell both the design metrics is improved simultaneously because read operation is performed independently by the read decoupled scheme.

The channel length (L) is kept at its minimum value (i.e. 16-nm) for all the transistors used in the CON6T and FDRD7T. fT (transition frequency) for short-channel devices is inversely proportional to L [11]. This is the main design strategy to keep the L at its minimum value. The width (W) is kept at 16-nm for all the PMOS transistors (i.e. MP1, MP2, MP3, MP4 and MP5). For driver transistors (i.e. MN1 and MN2) the W is set at 32-nm. The width of MN3 is taken as 64-nm because read current from all the cells in corresponding row flows through it. This will help to reduce the delay during read operation.

## 3. RESULTS AND DISCUSSIONS

In this section, the following design metrics of an SRAM cell i.e. read and write delay, RSNM and WSNM, dynamic power are investigated.

### a) Read access time analysis

For read operation both read word line (RWL) and write word line (WWL) are turned high. Therefore, write assist transistor MP5 will be OFF. Both the bitlines (BL and BLB) are precharged to supply voltage (VDD). Since, RWL is high, transistor MN3 (see Fig. 2(a)) will be ON. Depending upon the content in the holding node either one of the two read access transistors (MP3 or MP4) will conduct. Therefore, one of the bitline (BL or BLB) will discharge through MP3 and MN3 or MP4 and MN3.

For example, assume node L contains logic '0' and H contains logic '1'. Therefore, read access transistor MP4 will conduct. Thus, BLB will discharge through MP4 and MN3.

Read delay or read access time or TRA is estimated as the time taken to discharge one of the bitline by 50 mV after read word line (RWL) starts increasing from its initial low voltage. Therefore, the difference between the two bitlines will be 50 mV, which is the necessary voltage difference between two input lines of a sense amplifier to avoid misread [12]. Read delay for both CON6T and FDRD7T are simulated at different supply voltage as tabulated in Table I and also plotted in Fig. 3.It can be seen that for all the supply voltages, the proposed FDRD7T shows shorter read delay than the CON6T.

### b) Write access time analysis

For write operation, write assist transistor MP5 is turned ON by pulling the WWL signal to ground and transistor MN3 is made OFF by turning RWL to low value. The desired, which is to be written, is loaded on BL and BLB.

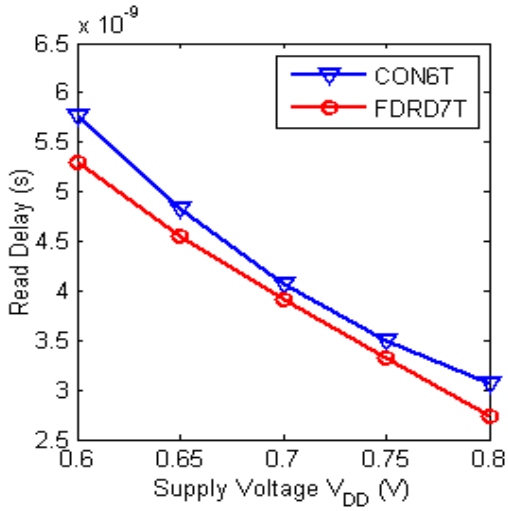



**Figure-3.** Read delay vs $V_{DD.}$

**Table-1.** Read selay.

| VDD (V) | TRA of CON6T (ns) | TRA of FDRD7T (ns) | Improvement (times) |
|---|---|---|---|
| 0.80 | 3.07 | 2.740 | 1.12× |
| 0.75 | 3.50 | 3.317 | 1.06× |
| 0.70 | 4.07 | 3.914 | 1.04× |
| 0.65 | 4.83 | 4.560 | 1.06× |
| 0.60 | 5.76 | 5.304 | 1.09× |

For example, suppose node H contains high value (logic '1') and L contains low value (logic '0'). Hence, transistor MP2 and MP1 will remain ON and OFF respectively. If it is desired that '0' is to be written at H and '1' at L, then BLB is set to high value (supply voltage) and BL is pulled down to ground. Therefore, voltage at H node will decrease through transistor MP2 consequently voltage at node L will increase. In this way voltage at node L will reach a certain value (switching threshold voltage of the other inverter) that will flip the cell content since node H and L are output nodes of two cross coupled inverter. Therefore, finally the desired data is written i.e. '0' at node H and '1' at L.

**Table-2.** Write delay.

| VDD (V) | TWA of CON6T (ns) | TWA of FDRD7T (ns) | Improvement (times) |
|---|---|---|---|
| 0.80 | 4.23 | 0.2713 | 15.60× |
| 0.75 | 4.38 | 0.2872 | 15.25× |
| 0.70 | 4.67 | 0.4419 | 10.57× |
| 0.65 | 4.71 | 0.4450 | 10.58× |
| 0.60 | 4.88 | 0.9602 | 05.08× |

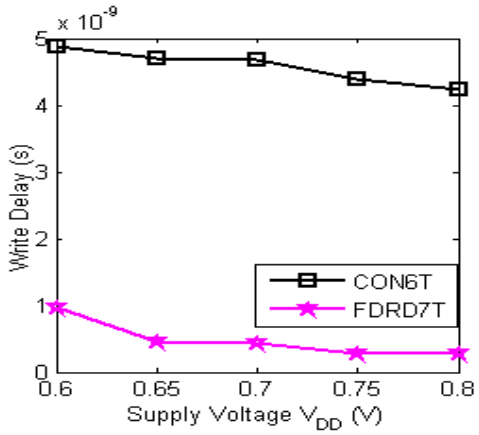



**Figure-4.** Write delay vs $V_{DD.}$

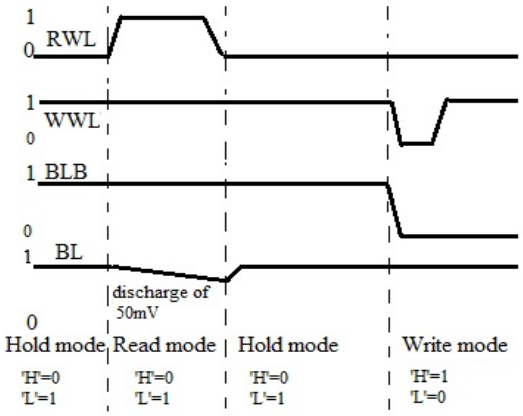



**Figure-5.** Operation of the proposed cell during read, write and hold mode.

Write delay or write access time or TWA is the time taken to reach the voltage at node L upto 90% of the supply voltage after WWL continues to decrease from its initial high value.

Write delay for both CON6T and FDRD7T are simulated at different supply voltage as tabulated in Table II and also plotted in Figure-4. It can be seen that for all the supply voltages the proposed FDRD7T shows shorter write delay than the CON6T.

### c) Investigation of read static noise margin

Read stability is quantified with the help of RSNM (read static noise margin) after seminal work of Seevinck in 1987. RSNM is defined as the minimum noise voltage that can cause read failure in an SRAM cell [13].

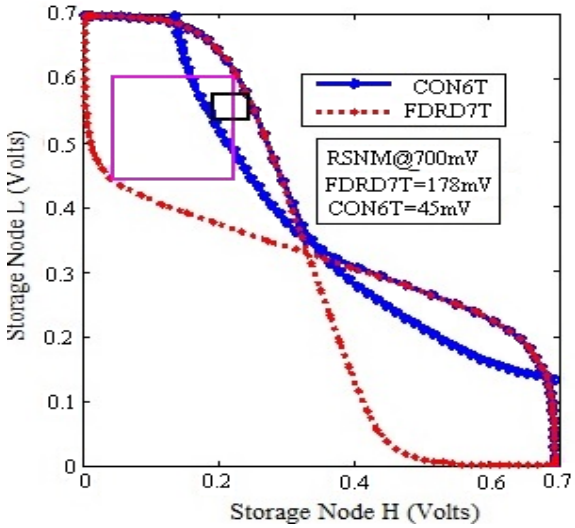



**Figure-6.** Static VTCs of SRAM cell during read operation.

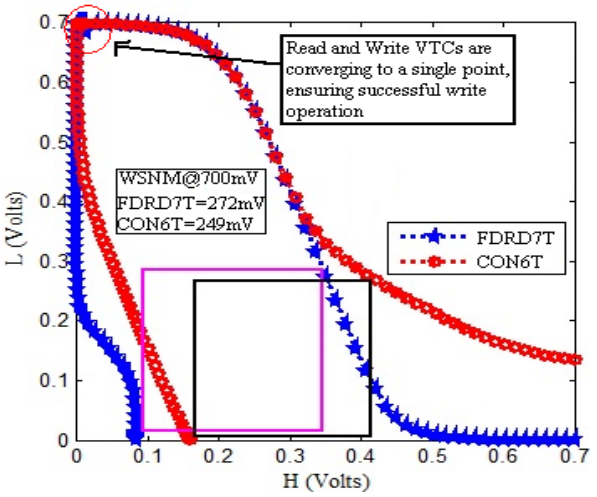



**Figure-7.** Static VTCs of SRAM cell during write operation.

RSNM is evaluated by driving the cell in the read mode i.e. turning both RWL and WWL high. RSNM is estimated from VTCs (voltage transfer characteristics) curves during read mode, which form a butterfly curve as shown in Figure-6. The largest square that can be incorporated inside the smaller lobe of that butterfly curve, a side length of that square is the measurement of RSNM. RSNM of CON6T is 45 mV whereas for FDRD7T it is 178 mV @700 mV supply voltage (see Figure-4).

Hence the proposed cell improves the read stability by a factor of 3.96. As the read current for the proposed cell does not flow through the storage nodes (unlike CON6T), it reduces the probability of read failure. This is the reason for improvement in RSNM. Therefore, read stability is improved.

### d) Investigation of write static noise margin

Write static noise margin or WSNM is used to estimate the ability of an SRAM cell to write the desired data in the storage nodes. The voltage at which (say at node H) logic '0' is to be written (suppose initially holding logic '1') has to be pulled down to a value low enough so as to flip the cell contents. Therefore, opposite data i.e. logic '1' will be written at node L. WSNM is used to measure the ability of an SRAM cell to pull down this voltage.

WSNM is estimated as aside length of the smallest square that can be included inside the lower half of the read VTC and write VTC as shown in Figure-7. From the figure, it can be seen that both the VTCs are converging to a single point. This is the sign of successful write operation [14]. WSNM of CON6T is 249 mV, while the same for proposed FDRD7T is 272 mV (see Figure-7). Therefore, there is improvement in WSNM for the proposed cell (9.23%).

**e) Dynamic power consumption**

Dynamic power consumption in an SRAM comprises of two components–one is power consumption during read operation (read power) and other is power consumption during write operation (write power). While reading, bitlines voltage swing is restricted to a smaller value on the other side, almost full bitlines voltage swing is necessary for write operation. This charging and discharging of these high capacitive bitlines contributes to the major portion of the total dynamic power dissipation.

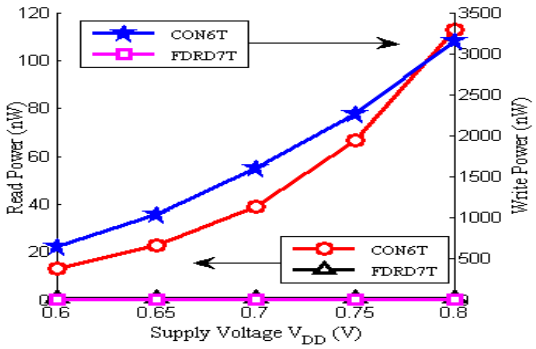



**Figure-8.** Dynamic power vs supply voltage.

Therefore, energy consumption during write operation is much higher than the energy consumption during read operation [15]. This holds true for the proposed cell also. Both the SRAM cells are simulated at 27°C. The simulated results plotted graphically in Figure-8. From the figure it can be seen that proposed FDRD7T cell consumes lower dynamic power than the CON6T for all the supply voltages.

## 4. CONCLUSIONS

The center point of this paper is to improve the SNM of an SRAM cell. The read SNM is improved by the fully differential read decoupled scheme and write SNM is enhanced because of the write assist transistor. Therefore, the proposed SRAM cell FDRD7T shows major improvement in both read and write SNM. The proposed cell also shows improvement in both read delay and write delay. Moreover, it dissipates less dynamic power. Hence, the proposed FDRD7T cell is the feasible option where SNM, speed of operation and power consumption are the major concern.

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