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DISTANCE BASED REORDERING FOR TEST DATA COMPRESSION

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ABSTRACT

The system-on-chip (SoC) revolution imposes a threat in the area of power dissipation by challenging designing as well as the testing process. Basically, a circuit or a system consumes more power in test mode than in normal mode. This increase in test power is due to increase in the number of switching activity in the device due to test pattern used for testing. This extra power consumption gives rise to severe hazards in circuit reliability and also can provoke instant circuit damage. Many techniques are available for test data compression. The "Proposed Tanimoto Distance Based Reordering" technique is a modification to the earlier proposed "Hamming Distance based Reordering - Columnwise Bit Filling and Difference vector".

Keywords: weighted transition, hamming distance, tanimoto distance, jaccard distance.

1. INTRODUCTION

Although there is an increase in the density of transistors, silicon industry has been able to cut down the manufacturing cost per transistor. But the testing cost per transistor was notable be reduce in great manner. Even though the testing cost has so many parameters, one of the major parameter is cost of Automatic Test Equipment (ATE). The Time taken for a chip to be tested depends on the number of channels, clock rate of channel and the required test data. So to reduce the time taken for testing, the amount of test data needs to be compressed. The test cost is allied to test data volume and test data transfer time. The Test data compression is the solution test cost by reducing the test data transfer time. In Testing Dynamic test power plays a major role in the overall test power. From the overall test power switching activity contributes the most of the dynamic power and overall test power [3]. Dynamic power consumption occurs due to the charging of the load capacitance C. The dynamic power consumption of the logic gate during the time interval [0, T] can be expressed as Pdyn =(1⁄2)C.Si.⟦Vdd⟧^2 Where Si is the number of switching's during the interval. In literature, there are many test data compression techniques like

- Linear decompression-based.
- Broadcast scan-based and
- Code-based techniques.

Code-based test data compression scheme is more appropriate for larger devices. From the various code-based test data compression schemes like dictionary codes, statistical codes, constructive codes, and run length-based codes. The do not care bit filling methods and test vector reordering further enhance the test data compression. Hence to increase compression ratio and also to reduce the number of switching activity run length-based test data compression method is used. Combining the Reordering techniques, Bit filling and run length codes can increase the test data compression. Run length based codes provide higher compression when the number of zero's is high in the test data. Hence reordering is done to achieve higher compression.

2. BACKGROUND

I. Run length codes

Run-length codes is a very simple form of test data compression in which runs of zeros are encoded using fixed-length code words [4]. The various Run length codes are Golomb codes, Frequency Directed run length codes (FDR), Extended Frequency-Directed Run-Length Code (EFDR), Alternating Frequency-Directed Run-Length Code (AFDR). Each Run length code is explained in detail with example in [9].

A. Run length codes

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B. Reordering

Reordering is used to minimize the average power and peak power dissipation during test operation [2]. There are many reordering techniques available. Reordering reduces the internal switching activity by lowering the transition density at circuit inputs. The techniques used here for reordering are Hamming Distance, Tanimoto distance, Jaccard Distance, Minimum Transition Filling, Weighted Transition, Columnwise bit filling and Difference vector.

3. DESIGN METHODOLOGY

In this paper, the compression is increased by the reordering the test data before applying Run length codes. The reordering is done by various techniques and is explained below.

a) Weighted transition based reordering

A simple heuristic is needed for comparing the power dissipated by two vectors [7]. Every vector does not

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dissipate the same amount of power. These are the scan vector for which weighted transition is explained as shown in Figure-1.

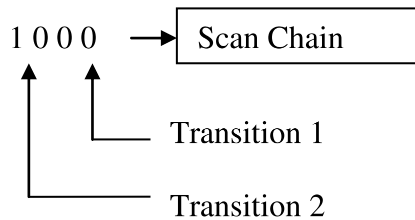

Figure-1. Method for finding weighted transition.

It has two transitions. When this vector is scanned into the CUT, Transition 1 passes through the entire scan chain. This transition dissipates power at every flip-flop in the scan chain. On the other hand, Transition 2 dissipates power only at the first scan flip-flop during scan in. The number of scan flip-flop transitions caused by a transition in a test vector being scanned in depends on its position in the test vector. In this example where there are 5 scan flip-flops, a transition in position 1 (which is where Transition 1 is) would be weighted 4 times more than a transition in position 4 (which is where Transition 2 is). The weight assigned to a transition is the difference between the size of the scan chain and the position in the vector in which the transition occurs. Similar reasoning can be applied for scan-out vectors. Hence, the power dissipated when applying two vectors can be compared by counting the number of weighted transitions in the vector. The number of weighted transitions is given by

Weighted Transitions = ∑ (Size of Scan Chain – Position of Transition) - (1)

$$WT = \sum_{i=1}^{n}[t(j,i) \oplus t(j,i+1)] * (n-i) \qquad (2)$$

b) Minimum transition fill

A series of don't care bit entries in the test vector are filled with the same value as the first don't care bit entry on the right side of this series [1]. This minimizes the number of transitions in the test vector when it is scanned in. The conventional approach for filling the don't care bit's in the test cube is to do a random fill in which the don't care bits are randomly replaced by 0's or 1's.

Example for Minimum Transition Fill

The test vector which is having reduced no of don't care bit is MT filled as shown below.

Test vector

Before MT filled 1 0 1 1 0 x 0 0 x x x 0 1 0
After MT filled 1 0 1 1 0 0 0 0 0 0 0 0 1 0

c) Hamming distance

The Hamming distance of block with highest frequency of occurrence is calculated from the other block having second highest frequency [6]. The Hamming distance is 1 if the bits are the same. The Hamming distance between two blocks is the summation of the bits having opposite values. The Hamming distance between two scan vectors is equal to the corresponding number of incompatible bits. This is similar to the Hamming distance with the extension of don't-care bits. Incompatible bits are bits having different values.

d) Tanimoto distance

The Tanimoto distance is defined as the number of similar bits, divided by the number of bits. Presented in mathematical terms, if samples X and Y are bitmaps, is the 'i'th bit of X, and are bitwise and, or operators respectively, then the common bits ratio is given as

$$T_S = \frac{\sum(X_i \cap Y_i)}{\sum(X_i \cup Y_i)}$$

Xi 1 0 1 1 0 0 0 0 0 0 0 0 1 0

Yi 1 1 1 1 0 x 0 0 x x x x 0 0

$$T_S = \frac{3}{5} = 0.6$$

e) Jaccard distance

The Jaccard distance, it measures the dissimilarity between sample sets, it's the complementary of the Jaccard coefficient and is obtained by reducing the Jaccard coefficient from 1, or, equivalently, by dividing the difference of the sizes of the union and the intersection of two sets by the size of the union.

$$JD = \frac{M11}{M01+M10+M11}$$

$$JD = \frac{3}{1+1+3} = \frac{3}{5} = 0.6$$

f) Columnwise bit filling

The bit stuffing of first vector will be done in such a way that it generates maximum zeroes to give maximum compression with run length based codes like Golomb, FDR or MFDR. So for such cases, the don't care bits will be replaced by zeroes. For such case, the don't care bit will be replaced by the same value of its prior bit i.e. if the prior bit is 1 then the don't care will be replaced by 1 and if the prior bit is 0 then the don't care will be replaced by 0 [6]. For the second test patterns and onwards, the don't care bit will be replaced by the same value which its upper vector has at the same position. The aim is to get the maximum zeroes in difference vector.

g) Difference vector

The Difference Vector is the difference between two successive test patterns. The Basic XOR operation is done between two continuous test patterns. The Difference vector is applied to increase the number of zeros in the test pattern which will further increase the compression ratio when Frequency Directed Runlength code is applied [7].

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Example for Difference Vector
Consider two vectors V1 and V2 and their difference vector is D2.

V1 ----- 1 0 1 1 0 0 0 0 0 0 0 0 1 0

V2 ----- 1 1 1 1 0 0 0 0 0 0 0 0 0 0

D2 ----- 0 1 0 0 0 0 0 0 0 0 0 0 1 0

h) Frequency directed run length codes

The test data will be first pre-processed by Weighted transition, Columnwise Bit Filling and Difference Vector scheme, and then FDR will be applied to the pre-processed data. The equation of compression ratio is [13]

$$\text{Compression ratio} = \frac{\text{Original bits} - \text{Compressed Bits} * 100\%}{\text{Original bits}} \quad (3)$$

Example for Frequency Directed Run Length Codes

Data stream	01	001	1	00001	000000001
Run length	1	2	0	4	8
Encoded data	01	1000	00	1010	110010

The Table-1 gives the FDR values for Runlength, an example for FDR based compression.

Table-1. 5 Frequency Directed Run length code table.

Run length	K	Group Prefix	Tail	Code word
0	1	0	0	00
1			1	01
2	2	10	00	1000
3			01	1001
4			10	1010
5			11	1011
6	3	110	000	110000
7			001	110001
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4. ALGORITHM FOR TD-WTR-CBF-DV

Step-1: A digital circuit with n scan flip-flops, p inputs, and q outputs is used to explain the algorithm.

Step-2: The test vectors with minimum number of don't care bits is selected as the first vector of the reordered test set.

Step-3: If there are more than one vector with minimum don't care bits

- MT fill technique is applied to each test vector,
- Weighted transition technique is applied for each test vector.
- The MT-filled vector with minimum weight is selected as the first vector of the reordered set.

Step-4: The Tanimoto distance of the remaining test vectors are calculated from the first vector of the reordered test vector.

Step-5: The Test vector with maximum Tanimoto distance is selected as next vector in the reordered test set.

Step-6: If there are more than one vector with maximum Tanimoto distance, then

- Columnwise bit fill technique is applied to each test vector, that is replace the don't care bit of the vector with the same position bit value of last selected vector.
- Weighted transition for each test vector is calculated and
- iii.The Columnwise bit filled vector with minimum weight is selected as the next vector of the reordered set.

Step-7: Step 6 is repeated until all the test vectors are reordered.

Step-8: Difference vector mechanism is applied to the reordered test set.

- The First vector of the reordered test set is kept unchanged.
- From the second test vector onwards, if the same position bits in last test vector and current test vector are same then its been replaced by bit 0 or 1.

Step-9: Frequency-directed run length code applied to the difference vectored test set.

5. EXAMPLE FOR THE ALGORITHM

These are the following test vectors for which algorithm is explained

1	**x**	**1**	**0**	**0**	**x**	**x**	**0**	**1**	**x**	**0**	**0**	**x**	**1**	**V1**
1	**1**	**1**	**x**	**0**	**x**	**0**	**x**	**1**	**0**	**1**	**0**	**x**	**x**	**V2**
1	**0**	**1**	**1**	**0**	**x**	**0**	**0**	**x**	**x**	**x**	**0**	**1**	**0**	**V3**
0	**x**	**X**	**0**	**x**	**x**	**1**	**0**	**x**	**x**	**x**	**0**	**x**	**x**	**V4**
1	**0**	**1**	**x**	**1**	**x**	**1**	**x**	**1**	**0**	**x**	**0**	**0**	**x**	**V5**
1	**1**	**1**	**1**	**0**	**x**	**0**	**0**	**x**	**x**	**x**	**x**	**0**	**0**	**V6**

Step-1: In the above test data, vector V3 has the minimum number of don't care bits, that is, 4. This vector is minimum transition (MT) filled as shown below.
Test vector

1 0 1 1 0 0 0 0 0 0 0 0 1 0 → V3

Weighted transition technique is applied to the MT filled Test vector V3. The weighted transition is calculated for n=14 and j is the value of the transitions which is highlighted in the test vector V3, using (1) and its corresponding weighted transition is 38.

Step-2: After placing the test vector V3 at first place and test vector V1 is shifted to the position of the test vector 3 as shown below.

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Test vectors after the first vector is reordered

1	0	1	1	0	0	0	0	0	0	0	0	1	0	R1
1	1	1	x	0	x	0	x	1	0	1	0	x	x	V2
1	X	1	0	0	x	x	0	1	x	0	0	x	1	V3
0	X	*x*	0	x	x	1	0	x	x	x	0	x	x	V4
1	0	1	x	1	x	1	x	1	0	x	0	0	x	V5
1	1	1	1	0	x	0	0	x	x	x	x	0	0	V6

Where R1 is the test vector of the reordered test set.
The Tanimoto distance of all the test vectors is calculated using R1 as the reference test vector. The Hamming distance is calculated as shown below.

1	0	1	1	0	0	0	0	0	0	0	0	1	0	R1
1	1	1	x	0	x	0	x	1	0	1	0	x	x	V2
1	X	1	0	0	x	x	0	1	x	0	0	x	1	V3
0	X	x	0	x	x	1	0	x	x	x	0	x	x	V4
1	0	1	x	1	x	1	x	1	0	x	0	0	x	V5
1	1	1	1	0	x	0	0	x	x	x	x	0	0	V6

The Tanimoto distance of the test vectors are obtained by the number of incompatible bits in each test vector compared with R1. The Tanimoto distance of the test vectors are mentioned below.

V2=0.4

V3=0.3

V4=0.0

V5=0.3

V6=0.6

The Vector V6 is having the maximum Tanimoto distance hence it is taken as the next reordered test vector R2 and V2 test vector is moved to 6th position and Columnwise bit is filled as shown below.

1	0	1	1	0	0	0	0	0	0	0	0	1	0	R1
1	1	1	1	0	0	0	0	1	0	1	0	1	0	V2

The Test vector V2 is Columnwise bit filled using R1 and the X bits in V2 are filled by the R1 values and they are underlined.

The test set after reordering of R2 is shown below

1	0	1	1	0	0	0	0	0	0	0	0	1	0	R1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	R2
1	X	1	0	0	x	x	0	1	x	0	0	x	1	V3
0	X	X	0	x	x	1	0	x	x	x	0	x	x	V4
1	0	1	x	1	x	1	x	1	0	x	0	0	x	V5
1	1	1	1	0	x	0	0	x	x	x	x	0	0	V6

The Tanimoto distance of V3, V4, V5, V6 test vectors are calculated using R2 as the reference vector.

1	0	1	1	0	0	0	0	0	0	0	0	1	0	R1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	R2
1	X	1	0	0	x	x	0	1	x	0	0	x	1	V3
0	X	X	0	x	x	1	0	x	x	x	0	x	x	V4
1	0	1	x	1	x	1	x	1	0	x	0	0	x	V5
1	1	1	1	0	x	0	0	x	x	x	x	0	0	V6

V3 =0.4

V4 =0.0

V5 =0.3

V6 =0.6

The Test vector V6 is having the highest Tanimoto distance value 0.6. Hence V6 is selected as the next test vector R3 of the reordered test set. The test vector is column wise bit filled.

1 1 1 1 0 0 0 0 0 0 0 0 0 0 R2

1 1 1 1 0 0 0 0 1 0 1 0 0 0 V6

Using R2, the X bits in V6 are Columnwise bit filled. The Test set after reordering of R3 is shown below.

1	0	1	1	0	0	0	0	0	0	0	0	1	0	R1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	R2
1	1	1	1	0	0	0	0	1	0	0	0	0	0	R3
0	x	X	0	x	x	1	0	x	x	x	0	x	x	V4
1	0	1	x	1	x	1	x	1	0	x	0	0	x	V5
1	x	1	0	0	x	x	0	1	x	0	0	x	1	V6

The Hamming distance of V4, V5, V6 test vectors are calculated using R3 as the reference vector.

V4 =0.0

V5 =0.3

V6 =0.6

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The Test vector V6 is having the highest Tanimoto distance value 0.6. Hence V6 is selected as the next test vector R3 of the reordered test set.

Step-3: The difference vector set is applied to the frequency directed run length coding**.**
Partially reordered test vectors

1	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**R1**
1	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**R2**
1	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**R3**
1	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**R4**
1	**0**	**1**	**x**	**1**	**x**	**1**	**x**	**1**	**0**	**x**	**0**	**0**	**x**	**V5**
0	**X**	**x**	**0**	**x**	**x**	**1**	**0**	**x**	**x**	**x**	**0**	**x**	**x**	**V6**

The Tanimoto Distance of the test vectors V5, V6 is calculated as shown below using R4 as the reference vector.

V5 = 0.6

V6 =0.0

The Test vector V5 is having the highest Tanimoto distance value 0.6. Hence V6 is selected as the next test vector R5of the reordered test set. The test vector is Column wise bit filled and reordered test set is shown below.

Reordered test vectors

1	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**		**0**	**0**	**0**	**1**	**0**	**R1**
1	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**		**0**	**0**	**0**	**0**	**0**	**R2**
1	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**1**		**0**	**0**	**0**	**0**	**0**	**R3**
1	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**1**		**0**	**0**	**0**	**0**	**1**	**R4**
1	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**		**0**	**0**	**0**	**0**	**1**	**R5**
0	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**1**		**0**	**0**	**0**	**0**	**1**	**R6**

Step-4: The difference vector technique is applied to the reordered test set. The difference vector set is
Difference test vectors

1	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**R1**
0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**D2**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**D3**
0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**D4**
0	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**D5**
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**D6**

6. RESULTS AND DISCUSSIONS

The proposed Algorithm working is checked using Xilinx 13.2 and it is written in Verilog and the reordering is checked using Modelsim simulator. The Test vectors with don't care bits are reordered using weighted transition, Column wise bit stuffing, Difference vector. The Reordering is done before Run length coding is applied. The compression ratio is obtained after applying Run length codes.

The Table-2 provides the compression ratio obtained with and without WTR-CBF-DV. The Compression Ratio obtained is 21%.

Table-2. Table for Comparison of compression ratio of with and without WTR-CBF-DV.

Compression Ratio.	**Run length code (FDR) Without WTR-CBF-DV.**	**Run length code (FDR) With WTR-CBF-DV.**
%	4.76	21.42

7. CONCLUSIONS

In this paper a new reordering scheme has been introduced to preprocess the test data before Compression. It includes the following techniques weighted transition based reordering, Hamming Distance, Column wise bit stuffing and difference vector. The preprocessed data is compressed using Frequency directed Run length code. The preprocessed data is used for testing the ISCAS 89 benchmark circuits. The Proposed compression technique provides higher compression.

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