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TESTING OF FAULTS IN VLSI CIRCUITS USING ONLINE BIST TECHNIQUE BASED ON WINDOW OF VECTORS

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ABSTRACT

Built in Self-Test (BIST) provides an attractive solution for testing embedded bocks and combinational circuits. It performs testing during normal operation of the circuit. There are several BIST schemes and the main parameters are the hardware overhead and time consumption. In the existing technique RAM module is used to store the test vectors. The hardware overhead is high because the size of the RAM grows proportion to the input vectors. To overcome the limitation, the RAM module is replaced by proposed module. And to reduce the time consumption, window of vectors is used. The proposed method uses online BIST technique based on window of vectors that performs testing during the normal operation of the circuit.

Keywords: VLSI, hardware overhead, time consumption, BIST.

INTRODUCTION

In the wide area of integrated chips there is a trade of in size and the complexity. Due to this trade of between size and the complexity there is a great challenge in testing these IC's. In the IC there are several functional blocks and transistors compacted in a single module. And so before placing each and every module the process of testing is necessary. A single fault in transistor and wrong connection in the wire results in faulty IC. Testing recovers these faulty IC's into fault free products. The testing process is made simple by recovering the problems of controllability and observability in the combinational circuits. These problems are reduced by using scan design techniques [20]. An alter method for the testing is the BIST (Built in Self-Test) [6]. BIST possess several advantages. There is no need of any additional circuitry for testing. BIST [6] when operates in test mode, test vectors are generated and it is fed to the testing circuit. BIST operates in on-spot testing and off-spot testing. During off-spot testing, the functioning of the testing circuit is interrupted to complete the test. Due to this interruption the response of testing circuit is disturbed. Most of the engineers use BIST for testing process for satisfying high dependability and low latency [1], [4], [12], [16]. The concept of BIST is also used in the fabrication of IC. The fabrication of IC involves several steps. After completing each and every step the need of testing is very necessary to avoid the faults. The architecture of the BIST module consists of the following blocks. They are Mode selection, testing circuit, test vector module, performance analyzer, address comparison, word decoder and decoded output module. Mode selection block is for the selection of mode either as on-spot testing and off-spot testing. Testing circuit is the combinational circuit in which the fault has been injected and tested. Test vector module generates the test vector for identifying the fault. The vectors have two parts such as address part and word part. Address comparison compares the address part of the input vector and the test vector. The word part of the input vector is decoded in the word decoder. The output of the Word decoder is stored in the decoded output module. The input vector which corresponds to the fault is called test vector. And this test vector is generated from the test vector module to the mode selection.

EXISTING SYSTEM

Built-In Self-Test (BIST) [6] techniques avoids the use of additional testing components and have high speed testing. It provide an attractive solution to test interior modules that embedded in complex integrated Circuits. There are many BIST techniques for testing process. Some of the techniques are discussed.

RAM based concurrent BIST technique

A novel input-vector monitoring concurrent BIST technique [19] for combinational circuits based on a self-testing RAM [5], [7] is used. Every existing technique compares favorably to the other concurrent BIST techniques [2], [9], [18] with regards to the hardware overhead and the numbers of cycles need to complete the test. For testing combinational circuits R-CBIST [18] is well-known technique because it uses small hardware while the normal operation of the circuit is not interrupted. The need of off-spot BIST techniques during the concurrent testing interrupts the normal operation of the testing circuit. In the same way, the need of input vector monitoring concurrent BIST techniques [2], [9], [18] for testing resides these ability to perform the test, whereas the testing circuit continues to operate normally. BIST uses a Test Vector Producer to produce the test vector which is applied to the input of the testing circuit. In off-spot testing since there is an interruption in the normal operation of the circuit, the performance of the circuit is degraded. To eliminate this performance degradation concurrent BIST techniques [10] have been proposed, in which the input vector is driven by the testing circuit during the normal operation of the circuit. The block diagram of an input vector monitoring concurrent BIST

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technique is presented in Figure-1. The testing circuit is combinational circuit that has n inputs and m outputs and tested. Hence, the test set size is $N = 2^n$. This scheme can operate in two modes, normal mode and test mode.

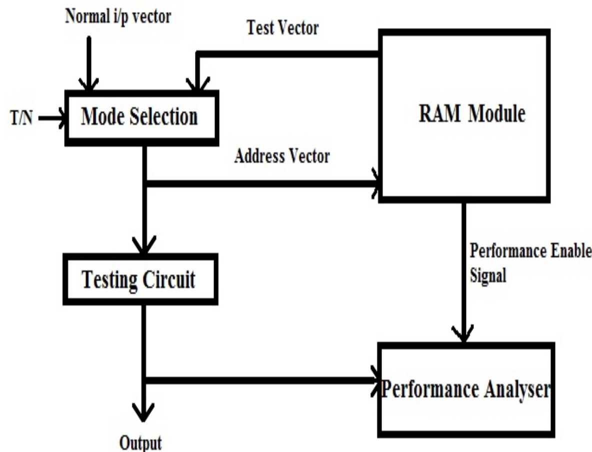

Figure-1. Block diagram of R-CBIST.

Operation of R-CBIST

It operates in two modes such as normal mode and test mode. During normal mode, the testing circuit is driven from the normal input vector. The input vector is also driven to the RAM module, in which the input vector is compared to the active test vectors. If one of the input vector matches with the active test vector, a strike has occurred. When a strike occurs the input vector is removed from the active test setand the performance analyzercaptures the response of the testing circuit. When all the input vectors have underwent a strike, the contents of the performance analyzer are verified whether a fault has occurred in the testing circuit. In case that during normal operation, the testing circuit does not receive all input vectors, the circuit may operate in test mode in order to complete the test. During test mode the testing circuit is driven by the RAM module and the performance analyzer is enabled in every testing operation to analyze the response of the testing circuit. Hence the time consumption becomes larger in order to complete the test. And so to reduce the number of cycles, the hardware is increased. The proposed method is to use windows of vectors to reduce both the hardware overhead and time consumption.

PROPOSED METHOD

The proposed system is testing of faults using online BIST technique based on window of vectors. Online BIST technique [11] detects faults during the normal operation of the circuit. And there is no need to interrupt the operation of the circuit to rectify the fault. The block diagram of proposed BIST architecture is shown in Figure-2. Here the RAM module is replaced by the proposed module. The various BIST schemes are proposed and it is evaluated based on two parameters such as hardware overhead and time consumption. The concept of window of vectors is proposed to reduce the number of cycles to complete the test [5].

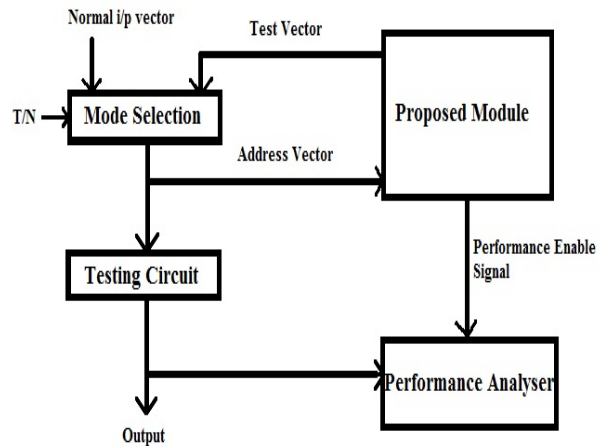

Figure-2. Block diagram of proposed method

Block diagram

The proposed module consists of Mode selection, testing circuit, performance analyzer, address comparison, word decoder, decoded output module and test vector module. The detailed block diagram of the proposed method is shown in Figure-3. In this proposed method, the hardware overhead and time consumption is reduced and fault is recovered without the need to interrupt the normal operation. The testing circuit has n inputs and m outputs and is tested exhaustively. Hence, the test set size is $N = 2^n$. [9], [18]. The scheme can operate in one of the normal or test mode, based on the value of the signal from the mode selection.

Operation of the decoder

The word decoder has PLA (Programmable Logic Array) like structure and it is controlled by two signals, namely address comparison signal and test vector signal. It has three modes of operation.

- When test vector signal is enabled, all outputs of the word decoder goes to one.
- When address comparison signal is disabled and test vector signal is not enabled, all outputs are disabled.
- When test vector signal is disabled and address comparison signal is enabled, the module operates as a normal decoding structure.

The operation of decoder is to select the particular cell with the help of sense amplifier and the test vectors are stored in the SRAM (Static Random Access Memory). When test vector signal is enabled, the test vectors are driven by the testing circuit and the module operates in the test mode. During this test mode, the test vector generated by test vector module is given to the

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testing circuit. When address comparison signal is enabled, the testing circuit is driven by the normal input vector.

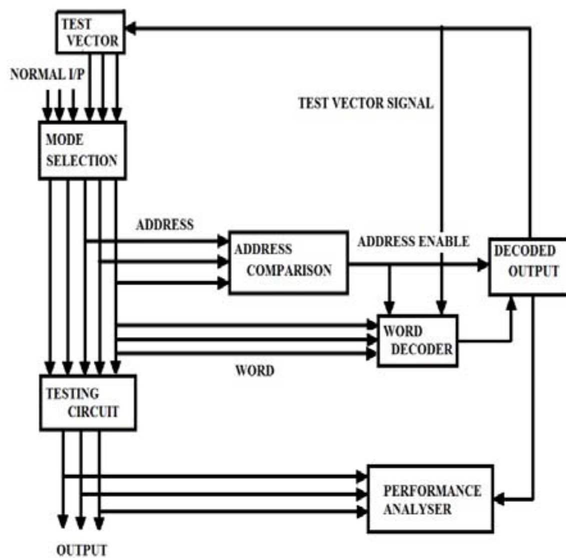

Figure-3. Proposed method.

Operation of the proposed method

- In the first step, every module is initialized to zero value. After initialization is done, the test vector signal is enabled and all the outputs of the word decoder denotes the value one.
- When the circuit operates in normal mode, the inputs to the testing circuit are driven from the normal input vector and also driven by the proposed module. The least significant bits are given to the word decoder and the highest significant bits are given to the address comparison. The word part of the input vector matches with the word part of the test vector, the address comparison signal is enabled and the corresponding output of the word decoder is enabled.
- If the incoming input vector does not match with the test vector, then the performance analyzer is not enabled and it maintains the previous value.
- When all the input vectors are arrived, then the output value is one.

Calculation of hardware overhead

The hardware overhead of the proposed scheme is calculated using the total number of gates consumed for the modules. One gate equivalent is equal to the hardware of two-input NAND gate [18]. The hardware overhead of the proposed module is shown in Table-1. The parameters that affect the hardware overhead of the proposed scheme are n (the number of testing circuit inputs), m (the number of testing circuit outputs), and w (vector size) with k = n - w and W = 2w [18].Furthermore, the accumulator-based compaction [3], [8], [15] requires only a one bit full adder (FA) and a D-type flip-flop (DFF) for each testing circuit output.

Table-1. Hardware overhead of the proposed method.

Module	Hardware overhead	Gates
n-stage multiplexer	n x MUX_{21}	3 x n
m-stage ABC	m x (DFF + FA)	18 x m
k-stage comparator	K x(XOR2) + k-stage AND	5xk
w to W decoder	2 x W	2xW + 4xw
Logic(W)	1,5xW + SA + 2xBuf + 2xDFF + 2	1,5xW + 23
TG	8xk	8xk
w-stage counter	8xw	8xw
Total	15xn + 18xm + k + 3,5xW + 23	

Simulation

In the proposed module bridge fault is injected. Bridge fault is two or more lines are coupled to vdd or ground. In the Figure-4. Simulation without fault is shown. Here a = 0 and b = 0 is given as input and it denotes the absence of fault. It operates in normal mode of operation. When all the vectors reach the CUT, the output of the decoder is one.

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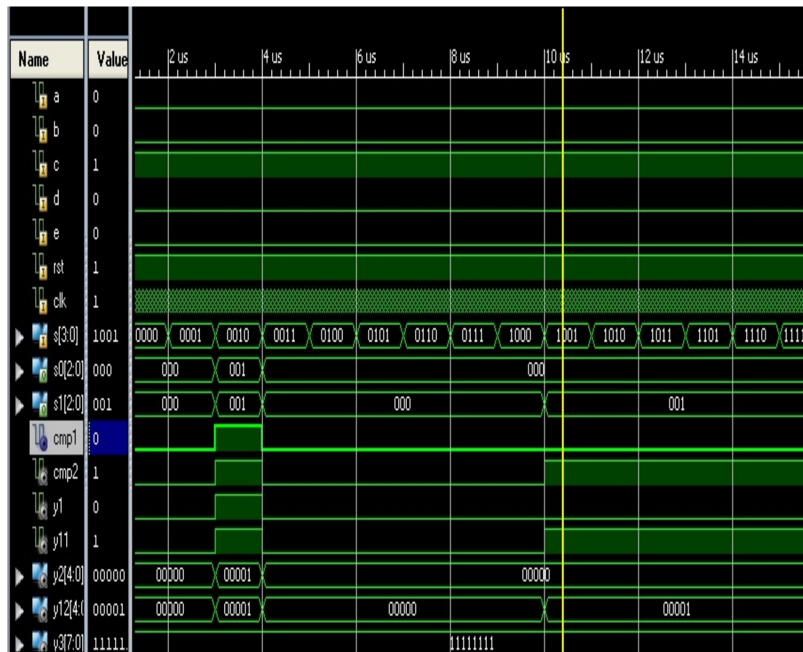

Figure-4. Simulation without fault.

The Figure-5 shows the simulation graph with fault. Here a = 1 and b = 1 is given as input and it denotes the presence of bridge fault. It operates in test mode of operation. When all the test vectors reach the CUT, the output of the decoder is one. The test vectors are 0000. 0001.

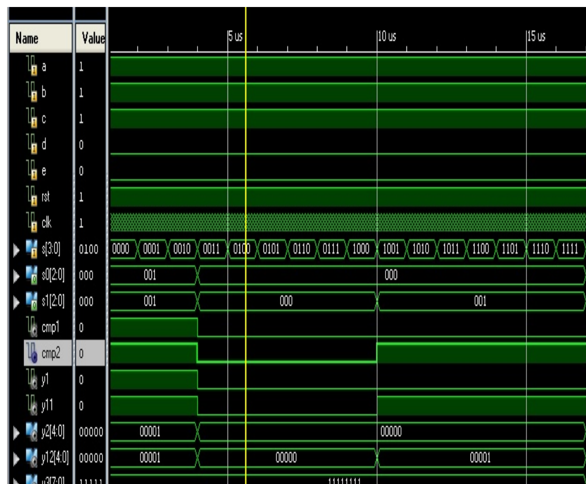

Figure-5. Simulation with fault.

The graph is shown in Figure-6. Is the comparison of the existing method with the proposed method for various values of hardware overhead and time consumption? From this graph it is clear that comparing to the existing method the proposed scheme gives the best result.

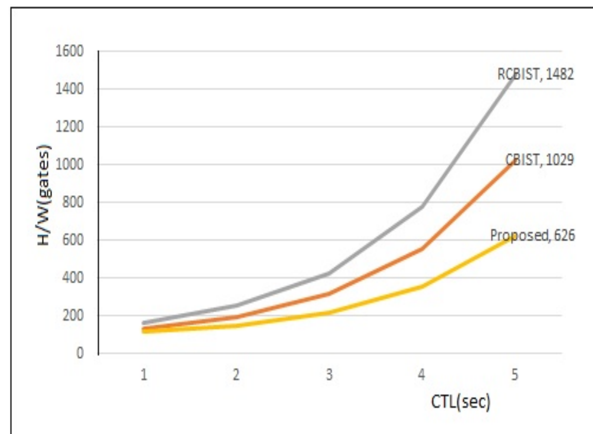

Figure-6. Hardware overhead vs time consumption.

CONCLUSION AND FUTURE WORK

Built in Self-Test (BIST) provides an attractive solution for testing embedded bocks and combinational circuits. It performs testing during normal operation of the circuit. There are several BIST schemes and the main parameters are the hardware overhead and time consumption. In the existing technique RAM module is used to store the test vectors. The hardware overhead is high because the size of the RAM grows proportion to the input vectors [13], [14]. To overcome the limitation, the RAM module is replaced by proposed module. And to reduce the time consumption, window of vectors is used. The proposed method uses online BIST technique [11] based on window of vectors that performs testing during the normal operation of the circuit. The proposed scheme

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is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques in terms of hardware overhead and time consumption. In the future, Square window Monitoring concurrent technique [17] will be used for testing of faults and performance is analyzed by comparing both of the techniques.

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