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ANALYSIS OF 16-BIT CARRY LOOK AHEAD ADDER – A SUBTHRESHOLD LEAKAGE POWER PERSPECTIVE

Amuthavalli G. and Gunasundari R.
Pondicherry Engineering College, Puducherry, India
E-Mail: amuthavalli.phd1@gmail.com

ABSTRACT

Power is an inevitable curb on digital design of emerging technologies. The down-scaling of transistor geometric paves the way for the curtailment of power consumption. Out of all the leakage components, subthreshold leakage current is the major shell out in static power dissipation. The subthreshold leakage power is analyzed in conventional circuit of 16-bit Carry Look Ahead Adder (CLA). The paper aims on a novel concept of Short Pulse Power Gated Approach (SPOGA), a leakage power reduction technique implemented particularly for low duty cycle (Example: Wireless Sensor Networks, Burst Mode type, etc.,) applications. The values of power consumption of the circuit are interpreted from the transient analysis of the circuit using 90nm technology in Cadence GPDK.

Keywords: subthreshold leakage power, carry look ahead adder (CLA), short pulse triggering, standby mode, leakage saving, 90nm technology.

1. INTRODUCTION

The emerging technologies in the micro-electronic industries become the part and parcel in the application of electronics and communication engineering concepts. Based on geometrics, the transistor is of long-channel and short-channel type. The trend of device miniaturization appreciates only short-channel transistors. But, the electrical behavior of them due to scaling of channel length and width (W/L) leads to second-order effects called Short-Channel Effects (SCE) as stated by Roy et al [1] such V_{th} roll-off, Drain Induced Barrier Lowering, Narrow Width Effect. The proportional scaling of gate oxide thickness (T_{ox}) gives leakage current due to the effects such as gate-oxide tunneling, hot carrier injection and Gate Induced Drain Lowering (GIDL). The scaling of CMOS transistor dimensions leads to increase in the off-state current (I_{off}); increases the static power consumption of CMOS digital circuits. The International Technological Roadmap for Semiconductors (ITRS) reported [11] that power scaling is one of the long term difficult challenges of Process Integration, Devices and Structures (PIDS) in front-end process. So, the I_{off} or leakage current is to be controlled to provide low static power consumption. The leakage current mechanism is reverse-bias pn junction leakage (I_{pn_diode}), subthreshold leakage (I_{sub_leak}), gate-oxide tunneling current (I_{oxide_tunnel}), hot-carrier injection gate current (I_{gate_hot}), GIDL (I_{gidl}) and channel punch through current (I_{punch_thr}). As inferred by Roy et al [1], all the six leakage current components are based on off-state of the transistor; whereas I_{pn_diode} & I_{oxide_tunnel} (also on on-state dependent) and I_{gate_hot} (transition state dependent). The focus of the paper is on only I_{off}, as it aims on standby mode of the digital circuits.

Generally, the reduction of I_{off} is possible by both process-level and circuit-level. Since the process-level technique is out of the scope of the research, only circuit-level technique is to be done by varying any of the terminal voltages of transistors. In the off-state currents [1], I_{pn_diode} (doping profile), I_{oxide_tunnel}, I_{gidl} & I_{gate_hot} (fabrication dependent) and I_{punch_thr} (ion implantation), only Subthreshold Leakage Current (I_{sub_leak}) is circuit-dependent i.e., depends on the operating region of transistor. The reduction of subthreshold leakage power becomes prominently mandatory with down scaling of CMOS technology. Obviously, the sensor node operates in active state for shorter duration and in sleep state for longer time. Such a low duty cycle applications requires only contextual leakage reduction techniques; but almost all the leakage power reduction techniques are applicable to high duty cycle applications. So, a novel concept of very low duty cycle short pulse is used as a triggering signal in high threshold voltage transistors or sleep transistors. The proposed subthreshold leakage power reduction technique is called Short Pulse Power Gated Approach (SPOGA).The analysis of CMOS digital circuits (Carry Look Ahead Adder as test bench circuit) in perspective of I_{sub_leak} to provide low static power consumption is researched as two categories: 1) conventional 16-bit CLA; 2) proposed SPOGA- based 16-bit CLA.

The Section 1 introduced the focus of the paper. The Section 2 discusses the literature review of subthreshold leakage current and power & its related works. The Section 3 explains the analysis of subthreshold leakage power in conventional 16-bit CLA. The Section 4 describes the proposed SPOGA technique and its reduction of subthreshold leakage power in 16-bit CLA. The Section 5 discusses the simulation, comparison of subthreshold leakage power of two 16-bit CLA circuits. The Section 6 concludes the paper.

2. LITERATURE REVIEW AND RELATED WORKS

The two principal components of static power consumption are subthreshold leakage current (a weak-inversion current across the device) and gate leakage

current (a tunneling current through the gate-oxide insulation) [2]. The development of high-K dielectric gate insulators neglects the gate leakage current, whereas the subthreshold leakage current (I_{sub_leak}) is strongly dependent on the threshold voltage and the supply voltage [3]. The P_{sub_leak} is almost equal to the static power in the standby mode and it can be calculated [1] [2] as in Equation(1) and Equation(2):

$$P_{sub\_leak} = I_{sub\_leak} \times V_{dd} \quad (1)$$

$$I_{sub\_leak} = K_1 W e^{-\frac{V_{th}}{nV_T}} \left[1 - e^{-\frac{V_{dd}}{V_T}}\right] \quad (2)$$

where W is the gate width, V_T is the thermal voltage, K_1 and n are the experimentally derived constants, V_{dd} is the supply voltage and V_{th} is the threshold voltage. The I_{sub_leak} can be reduced either by turning off the supply voltage (i.e., V_{dd}=0) and/or increasing the threshold voltage (i.e., using high V_{th} transistors) [4].

Uma Nirmal *et al*. [5] discussed the high performance and low power consumption of 4-bit Carry look ahead adder of 180nm technology using MTCMOS technique, which reduces 50-53% of total power consumption compared to 4-bit carry look ahead adder of traditional circuit. Jas leen Chaudhary et al. [8] analyzed the performance of carry skip, carry select, carry increment and carry ahead adder. J. B. Kim [9] compared the conventional circuit design and proposed triple-threshold circuit design of 16-bit carry look ahead adder, from which 14.71% of power is reduced with design limitations. Jagannath Samanta *et al*. [10] analyzed the carry look ahead adder using different logic styles such as Standard CMOS, DCVS Pseudo NMOS, PTL & Domino logic style. Out of all logic styles, the power consumption of standard CMOS is 20.75uW. After a thorough review of relevant information, Static CMOS logic style is chosen for the design of 16-bit CLA.

3. CONVENTIONAL CARRY LOOK AHEAD ADDER (16-BIT CLA_CONV)

The CLA is one of the high speed adders, which solves the problem of low speed adders (such as Ripple Carry Adder) by pre-calculating the carry bits using the input bits [5]. The conventional circuit of static CMOS logic style of 16-bit CLA as given in Figure-1 is used as benchmark circuit.

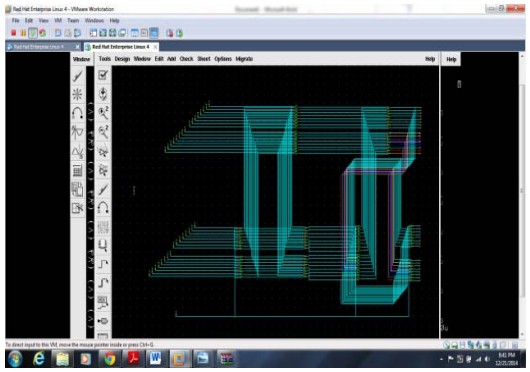

Figure-1. Schematic diagram of 16-bit CLA_CONV.

The circuit is analyzed with the inputs of A0 B0 to A15 B15 are given as all 1's or all 0's. When all the inputs A0 B0 – A15 B15 are set as 1V and carry input C0 is 0V, the sum outputs S0 – S15 and the carry bits C0 – C15 are approximately 1V. This has been achieved by transient analysis of 16-bit CLA_CONV circuit as in the transient response Figure-2, Figure-3, Figure-4 and Figure-5 of the circuit.

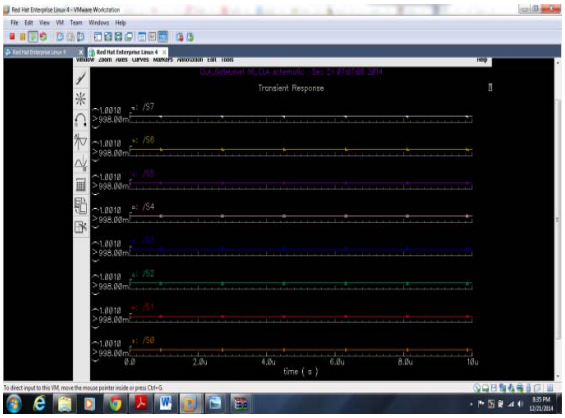

Figure-2. Transient response - output sum (S0 to S7) bits.

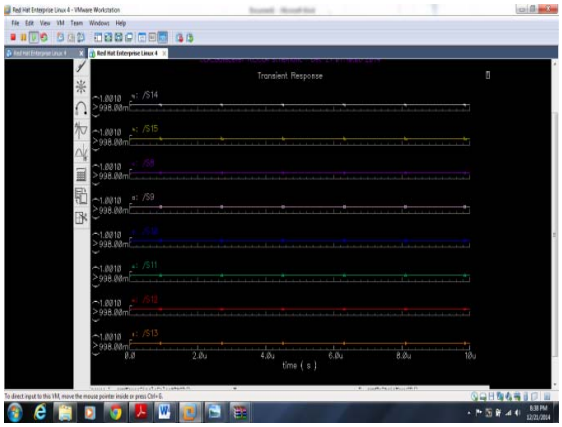

Figure-3. Transient response - output sum (s8 to s14) bits.

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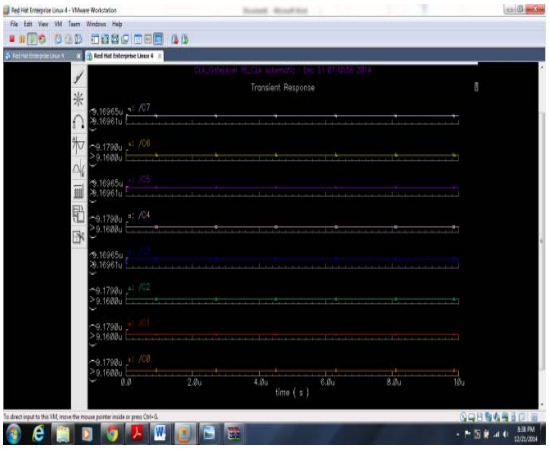

Figure-4. Transient response - output carry (c0 to c7) bits.

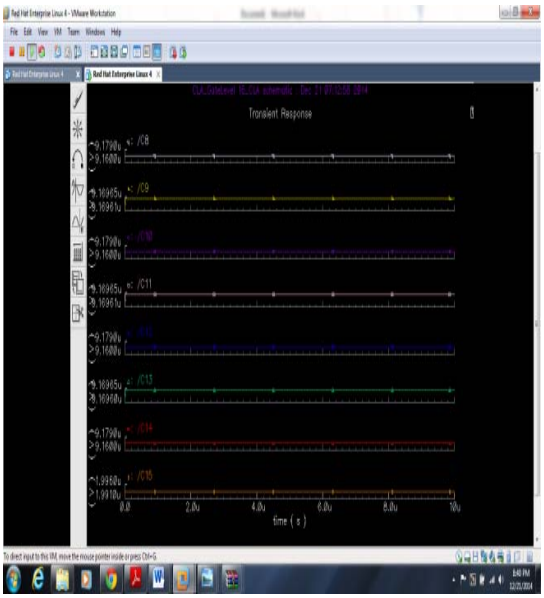

Figure-5. Transient response - output carry (c0 to c7) bits.

As subthreshold leakage power (P_{sub_leak}) is the dominant component of the leakage power, the off-state transistors are analyzed. The transistors operated in the region R_3, called as subthreshold region or the weak-inversion region. The input state impacts on the power consumption. Table-1 discusses the power consumption of 16-bit CLA_CONV with high inputs. The static and the subthreshold leakage power is 3.284µW.

Table-1. Power Consumption of 16-bit CLA_CONV with input A0B0 to A15 B15 = 1V.

Gates	No. of transistors	Transistors in R_3	P_{sub_leak} (µW)	P static (µW)
EXOR_1	96	NM0, NM3, PM2	808.16	808.32
EXOR_2	96	NM0, NM3, PM2	808.16	808.32
EXOR_3	96	NM0, NM3, PM2	808.16	808.16
AND_1	96	NM0, NM1, PM2	25.44	25.44
AND_2	96	NM0, NM1, PM2	25.44	25.44
OR	96	NM0, NM1, PM2	807.84	808.16
TOTAL	576	288	3283.2	3283.84

The main focus of the paper is on the power consumption of the circuit in standby mode. The inputs A0B0 to A15B15 = 0V are applied to the 16-bit CLA_CONV with supply voltage of 1V, results in a power consumption as given in Table-2. Since more transistors are operated in subthreshold region in this case than 1V input condition, it consumes approximately 84 µW of P_{sub_leak}.

Table-2. Power Consumption of 16-bit CLA_CONV with input A0B0 to A15B15 = 0V.

Gates	No. of transistors	Transistors in R_3	P_{sub_leak} (µW)	P static (µW)
EXOR_1	96	NM1	1.6	325.28
EXOR_2	96	NM1, NM3, PM2, PM3	55.52	175.36
EXOR_3	96	NM0, NM1, NM3, PM0, PM2	10.37	19.81
AND_1	96	NM1, NM3, PM1, PM2	5.12	8.48
AND_2	96	NM1, NM3, PM1, PM2	5.12	6.23
OR	96	NM0, NM1,NM2, PM1, PM2	6.24	6.24
TOTAL	576	367	83.97	541.4

From the analysis of 16-bit CLA_CONV in the perspective of subthreshold leakage power, it clearly specifies the need for the leakage power reduction in standby mode.

4. CARRY LOOK AHEAD ADDER (16-BIT CLA_SPOGA) USING SPOGA TECHNIQUE

4.1 Short pulse power gated approach (SPOGA)

The substantial increase in the subthreshold leakage power of digital subsystems in standby mode, due to scaling down of the CMOS technology paves the way to design an efficient subthreshold leakage power reduction technique suitable for WSN applications, is called Short Pulse Power Gated Approach (SPOGA). In this approach, the hybrid concept of Multi Threshold CMOS (MTCMOS) and Power Gating, in which the high threshold voltage (high-V_{th}) sleep transistors are incorporated. The hybrid approach is implemented by many researchers [5]; but applicable only for high duty cycle applications. Since WSN is a low duty cycle application, the hybrid approach results in poor leakage reduction. So, a novel concept of low duty cycle [6] short pulse is used to trigger the sleep transistors which are used in the global power gating of the circuit.

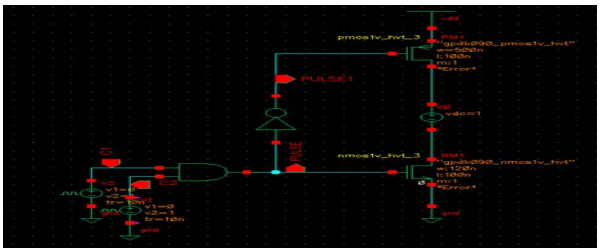

Figure-6. SPOGA circuit.

In SPOGA technique, the combinational circuits and high-V_t transistors are used with the supply voltage of 1V as given in Figure-6. The two clock pulses with different delay times are applied to AND gate, which gives low duty cycle short pulse as output. The short pulses with true and complemented form as in Figure-7 are used to trigger the high- V_t transistors NMOS and PMOS respectively. The Short Pulse (SP) has very shorted T_{on} period i.e., SP_Active mode and longer T_{off} period i.e., SP_Sleep mode with 5% duty cycle. In WSN, the sensor device activates only for shorter duration and enters into sleep state unto the arrival of next desired signal [7]. So, the concept of short pulse triggered power gating technique is more suitable for the leakage-aware circuit design techniques in the architectures of WSN applications.

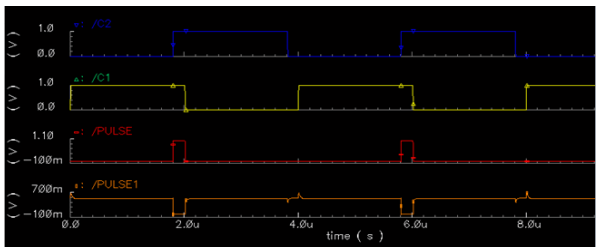

Figure-7. Low duty cycle short pulse.

4.2 Subthreshold leakage power of 16-bit cla_spoga

The proposed SPOGA circuit is implemented in the conventional design of 16-bit CLA to reduce the subthreshold leakage power. The circuit is activated in the ON time of short pulse called as active mode and deactivated in the OFF time of the pulse called as sleep mode. The circuit 16-bit CLA_SPOGA is analyzed in the sleep mode or standby mode as given in Table-3, which results in the very low power consumption. Only 4% of subthreshold leakage power influences the static power consumption in standby mode.

Table-3. Power consumption of 16-bit CLA_SPOGA in standby mode.

Gates	No. of transistors	Transistors in R_3	Psub_leak (zW)	Pstatic (zW)
EXOR_1	96	NM0, NM1, NM3	30.4	1168
EXOR_2	96	NM0, NM1, NM3	30.4	1168
EXOR_3	96	NM0, NM1, NM3	30.4	1153.3
AND_1	96	NM0, NM1, NM3	73.6	1154.56
AND_2	96	NM0, NM1, NM3	73.6	1154.56
OR	96	NM0, NM1, NM2	20.8	748.32
TOTAL	576	288	259.2	6546.74

5. SIMULATION RESULTS AND DISCUSSIONS

The Carry look ahead adder is designed using Cadence Virtuoso and the simulation is done using Cadence Spectre of 90nm technology node. The supply voltages of 1V, temperature of 27˚C and simulation time for transient analysis of 10µs are used. In 16-bit CLA_CONV, AND, EXOR and OR gates are connected and their overall static power is 541.4µW and subthreshold power is 83.97µW. The reduction of subthreshold leakage power could be done by varying the width of the transistors, threshold voltage, drain-to-source voltage, bulk current and so on as in its basic equation 2. As this paper focuses on circuit-level reduction techniques, only threshold voltage variation is used except other parameters, which are fab-dependent. Using the technique SPOGA, the static power consumption of 16-bit CLA is reduced to 6546.74zW or 6.54674 X 10^{-12}µW and the subthreshold leakage power is reduced to 259.2zW or 2.592 X 10^{-13}µW. The percentage of leakage saving of 16-bit CLA_CONV using SPOGA technique is approximately closer to 100%.

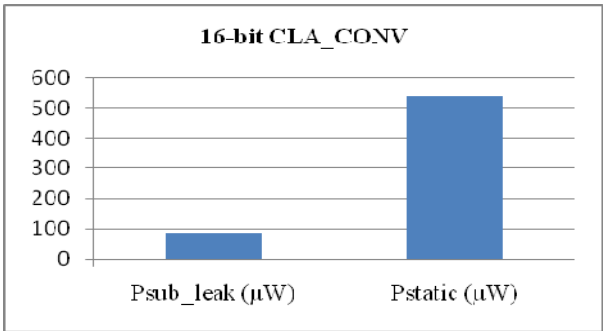

Figure-8. Subthreshold leakage power of 16-bit CLA_CONV.

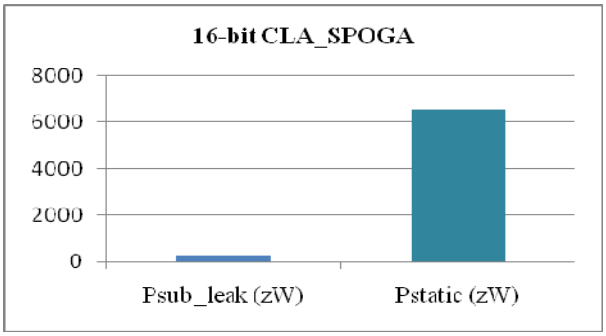

Figure-9. Subthreshold leakage power of 16-bit CLA_SPOGA.

From the analysis as given in Figure-8 and Figure-9 of conventional and proposed SPOGA circuit of 16-bit CLA, it is well understood that the SPOGA technique outperforms the conventional circuit.

6. CONCLUSIONS

The power-aware circuits are inevitable in WSN applications, as it operates in standby mode for most of the duration of targeted application. The short pulse activated the logic block only for needed short-duration, thereby reduced the unnecessary power consumption. Even though the circuit had been consumed low power, the area and the individual power consumption of the proposed leakage reduction circuit was more. However, this could be compromised for larger circuits, which would be very negligible for high-end applications.

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