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ANALYSIS OF CARBON NANO STRUCTURES FOR ON-CHIP INTERCONNECT APPLICATION

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ABSTRACT

This paper proposes the carbon nano structures particularly Carbon nanotube (CNT), Graphene Nanoribbon (GNR), with excellent electrical, thermal and mechanical properties making them an emerging alternative for future on-chip interconnect applications. Analysis of CNT and GNR as on- chip interconnect has been performed with the help of existing equivalent circuit model. Performance metrics such as delay, bandwidth, power delay product (PDP) have been considered. Performances of carbon nano structures (CNT and GNR) are better than Cu interconnect at all levels of interconnect, even when the technology scales below 22nm. The Single Layer GNR and Single Walled CNT exhibit only 0.5% and 0.7% of the delay observed in copper interconnects respectively. Extreme reduction in power dissipation has also been justified with the results. Thus it obeys Moore's law even when technology scales into tens of nanometer.

Keywords: carbon nanotube (CNT), single walled CNT (SWCNT), graphene nanoribbon (GNR), single layer GNR (SLGNR), power delay product (PDP), bandwidth.

INTRODUCTION

Advancement in VLSI technology is mainly due to the continuous reduction in the feature size of VLSI devices. Feature size is the minimum length of the transistor channel. All VLSI circuits contain millions of devices and components like transistor. These are linked electrically by the metal wires which are called as interconnect. As the technology scales down it improves transistor performance and degrades the interconnect performance in deep sub-micron technology node. In deep sub- micron technology node interconnect play critical role. Earlier only gate delay was consider for timing charteristics, but now interconnect delay dominate the gate delay. This is because in deep sub-micron technologies, more no of interconnections are used to connect the millions of devices. Thus resistance of wire increase significantly giving rise to propagation delay. In early 90's the shrinking of device dimensions caused Al interconnects to suffer from high electromigration resistance. Copper was considering as alternative material for Al interconnect due to the low resistivity and current carrying capability of copper is much higher than Al. At deep sub-micron technology node, copper interconnect meet serious issues such as electromigration, surface and grain boundary scattering of electron. It causes higher propagation delay thus degrading system performance of VLSI circuit. These are the most important shortcomings which limits the efficiency of Cu interconnects in deep sub-micron technology. So, the researchers are forced to find an alternative material to improve interconnect performance in ultra-deep sub-micron technology node. According to the Interconnect technology road map (ITRS) 2011, Carbon Nano materials like Carbon Nanotube (CNT), Graphene Nanoribbon (GNR), Carbon Nanowire and optical interconnects have emerged as the most promising candidates for future interconnect technology. Both CNT and GNR have good ballistic transport and large current carrying capability than copper without any electromigration problem. When compare to copper, GNR and CNT have large mean free path, promising thermal and electrical conductivity. Graphene nano structures has a high melting point compared to copper hence, it can with stand for high temperature.

This paper organized as follows: Section II shows the On-chip interconnects. Section III presents the results and compares the performances of Cu and Carbon nano structures interconnect through simulation. Section IV presents conclusions.

ON-CHIP INTERCONNECTS

Copper interconnect

The shrinkage in the feature size of Cu interconnects limit the interconnect performance and reliability in terms of delay, power and bandwidth. To analyse these parameter by using HSPICE simulator. Figure-1. Shows the equivalent RLC model for copper interconnect.

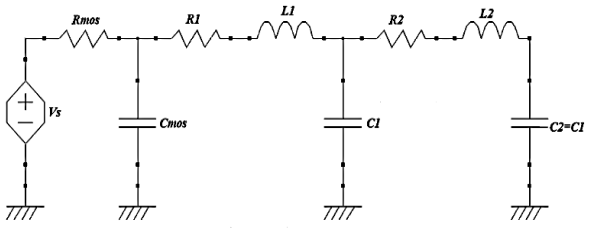

Figure-1. Equivalent RLC circuit model for copper interconnect.

Based on the demonstrated model, interconnect resistance R, capacitance C and inductance L can be calculated for various technology nodes.

$$R = \frac{\rho l}{wt} \quad (1)$$

$$C = \varepsilon\left[\frac{w}{h} + \left\{2.2\left(\frac{s}{s+0.7h}\right)^{3.19}\right\} + 1.2\left(\frac{s}{s+1.5h}\right)^{0.76}\left(\frac{t}{t+4.5h}\right)^{0.12}\right] \quad (2)$$

$$L = \mu l \Big/ 2\pi\left[\ln\left(\frac{2l}{w+t} + \frac{1}{2} + \frac{0.22(w+t)}{l}\right)\right] \quad (3)$$

$$M = \mu \frac{l}{2\pi\left[\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right]} \quad (4)$$

$$\varepsilon = \varepsilon_r \times \varepsilon_0 \quad (5)$$

Where R-resistance, ρ-resistivity, l-length of theinterconnect, w-width of the interconnect, t-thickness (thickness is determined by t=AR*W), s-spacing, L-inductance, C-capacitance, ε_r- relative dielectric permittivity of copper, ε_0- dielectric permittivity, d-distance between two layers, μ-permeability. Due to the high density interconnect the pitch (spacing between interconnects) s is assumed equal to the width of the interconnect i.e s=w. Hence the distance between layers of interconnect d is assumed equal to be twice the interconnect width.

CNT interconnect

Carbon Nanotubes (CNTs) are graphene sheets rolled up into cylinders with diameter in the order of nanometer [2]. Depending on the direction in which CNTs are rolled (chirality), they exhibit either metallic or semi-conducting properties [5] [6] [7]. The graphene sheet can be rolled in many possible ways such as Armchair, Zigzag are shown in Figure-2. According to the number of concentrically rolled up tubes, CNT can be classified as single walled CNT (SWCNT) and multi-walled CNT (MWCNT).

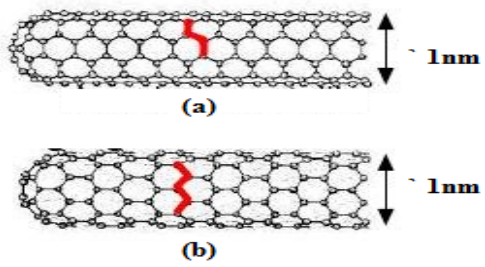

Figure-2. Structure of CNT (a) armchair (b) zigzag.

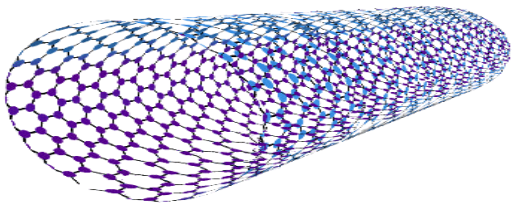

Figure-3. Structure of SWCNT.

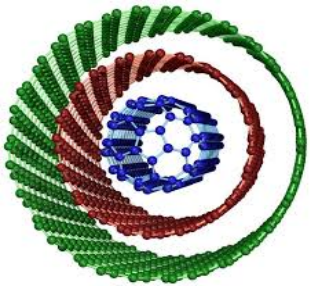

Figure-4. Structure of MWCNT.

SWCNT interconnect

SWCNT consists of a single layer of graphene sheet purely wrapped into a cylindrical tube. SWCNTs have only one layer of graphene sheet with diameters of 0.7 to 10nm [11]. Using this model, interconnect resistance *R*, capacitance *C* and inductance *L* were calculated for various length are calculated, the equivalent circuit model for SWCNT is shown in Figure-5. Using this model interconnect resistance (R), inductance (L) and capacitance (C) were calculated for various length from (6)-(7) [1],[5].

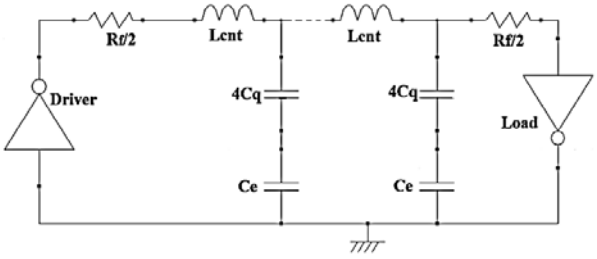

Figure-5. Equivalent circuit model of SWCNT.

$$R_f = \frac{h}{4e^2} \quad (6)$$

$$C_e = 2\pi \in \frac{1}{\ln\left(\frac{y}{d}\right)} \quad (7)$$

$$C_q = \frac{2e^2}{h v_f} \quad (8)$$

$$L_m = \frac{\mu}{2\pi} \ln\left(\frac{y}{d}\right) \quad (9)$$

$$L_k = \frac{h}{2e^2 v_f} \quad (10)$$

where,R_f-fundamental resistance, C_e-electrostatic capacitance, C_q-quantum capacitance, L_m- magnetic inductance, L_k- kinetic inductance, h- Planck's constant, ε-electric field, y- distance away from the ground, d-diameter, e- electron charge, v_f- Fermi velocity[5].

GNR interconnect

Graphene Nanoribbon (GNRs) can be constructed from unzipping of carbon nanotubes, So GNR own properties are similar to carbon nanotubes [8] [9]. GNR are classified as armchair and zigzag GNRs depending upon their termination style. Figure-6 shows the structure of armchair and zigzag GNRs [3].

The width of the armchair GNR decided by number of hexagonal rings or dimer lines (Na) across the ribbon. Similarly the width of the zigzag GNR is dependent on the number of the zigzag chains (Nz) across the ribbon. GNR can be classified as either metallic or semiconducting GNR based on the chirality and geometry. The armchair GNR again can be classified as metallic and semiconducting based on the number hexagonal rings (Na) while zigzag GNR always metallic [4].

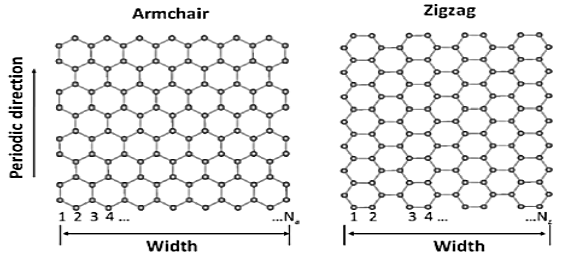

Figure-6. Structure of GNR (a) Armchair (b) Zigzag.

The GNR interconnects can be classified as single layer GNR (SLGNR) and multi-layer GNR (MLGNR) depending upon number of layers formed by hexagonal ring of carbon atoms. Figure-7. shows structure of single and multi-layer GNR [3], [6].

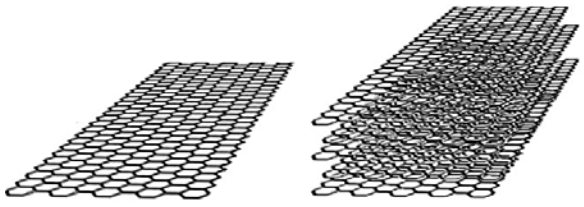

Figure-7. (a) Structure of SLGNR (b) Structure of MLGNR.

SLGNR interconnect

The interconnect behaviour of single layer GNR has been modelled as transmission line with RLC model as explained by authors in [4].Equivalent circuit model of isolated single layer GNR (SLGNR) is used for simulation because it is more convenient than multi-layer GNR (MLGNR). The equivalent circuit model of single layer GNR (SLGNR) shown in Figure-7.a. The equivalent circuit parameters are calculated using (11)-(17) [3] [6].

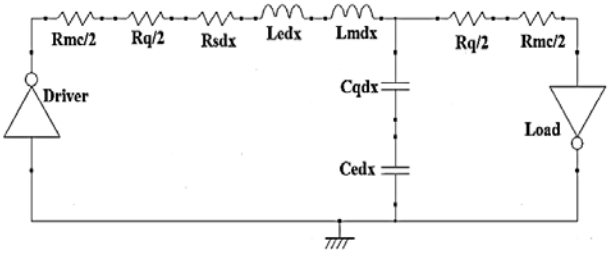

Figure-8. Equivalent RLC circuit model for SLGNR.

$$R_q = \frac{h}{2e^2 N_{ch}} \quad (11)$$

$$r_s = \frac{h}{2e^2 N_{ch}} \times \frac{l}{\lambda} \quad (12)$$

$$L_k = \frac{h}{4e^2 v_f N_{ch}} \quad (13)$$

$$L_e = \frac{\mu_0 d}{w} \quad (14)$$

$$C_q = \frac{4e^2 N_{ch}}{h v_f} \quad (15)$$

$$C_e = \frac{\varepsilon w}{d} \quad (16)$$

$$N_{ch} = \sum \left[1 + \exp\left(\frac{E_i - E_F}{K_B T} \right) \right]^{-1} + \sum \left[1 + \exp\left(\frac{E_i + E_F}{K_B T} \right) \right]^{-1} \quad (17)$$

Where R_q- quantum resistance, r_s- per unit length resistance, R_{mc}- contact resistance (in this paper we assumed R_{mc}-20KΩ), h-plank's constant, λ_{MFP}- mean free path(mean free path for SLGNR 450w), e-electronic charge, l-length of the interconnect, d-distance from ground plane, v_f -Fermi velocity, w- interconnect width, μ_0- permeability of free space, ε-permittivity, N_{ch}- number of conducting channels in one layer [1] [13], E_F- Fermi energy, $E_i=\Delta E|i+\beta|$ ($\beta=0$ for metallic GNR and $\beta=1/3$ for semiconducting ones) and $\Delta E=hv_f/2w$ is the band gap between subbands in GNRs [4].

PERFORMANCE ANALYSIS

The test circuit is used for evaluation of carbon nano structures as in interconnect shown in Figure-9. In that, interconnect is implemented with transmission line equivalent circuits of Cu, SWCNT, SLGNR is shown Fig (1, 5, 8). Equivalent circuits are implemented with RLC values of SWCNT and SLGNR which are calculated numerically by using its respective equations from (1-17).

Simulation results have done in HSPICE for 32nm, 22nm and 14nm technology node. The performance metrics such as delay, bandwidth and power delay product have measured from simulation results for various lengths of the interconnects. Performance comparisons have been made between copper and carbon nano structures.

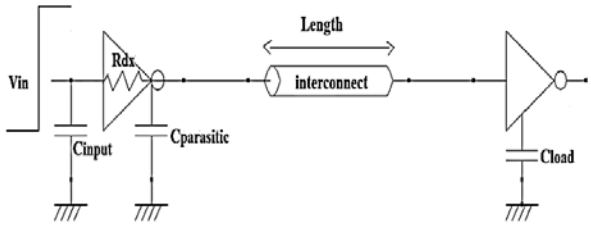

Figure-9. Performance test circuit.

Delay comparisons

Figure-10 shows the comparison of delay in copper interconnect, SWCNT and SLGNR in various technology nodes (32nm, 22nm and 14nm). The scale of the delay axis is taken in logarithmic measurement. With the increase in the length of the interconnect carbon nano structures outperform the Copper interconnects. At the local and intermediate level, both SWCNT and SLGNR delay performance over the Cu interconnect. Deep analysis of the results obtained in 22nm technology node, explains that, SLGNR minimal delay compared to Cu and SWCNT. Below 22nm, Cu interconnect produces a huge delay which is unacceptable. The ballistic transport property and large mean free path make the SLGNR and SWCNT exhibit only 0.5% and 0.7% of the delay observed in copper interconnects respectively. From Plot it is revealed that when technology scales down from 22nm to 14nm delay also reduces which shows that carbon nano structures conform the Moore's law for future technology nodes.

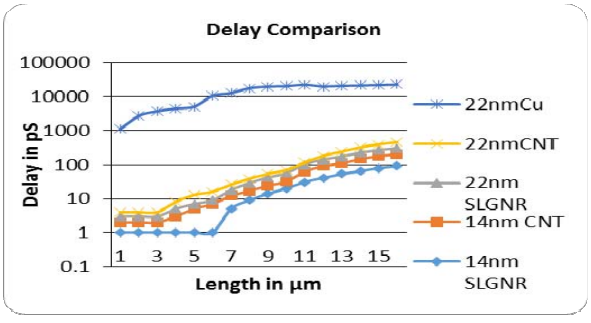

Figure-10. Delay comparison between Cu, SWCNT and SLGNR in 22nm and 14nm technology nodes.

Power delay product (PDP)

Table-1 shows that PDP comparison of Copper, SWCNT and SLGNR. It has been observed that carbon nano structures have very less power delay product almost 1000 times lesser than copper due to its excellent thermal conductivity and large conductance to the electric current flow.

Figure-11 shows the PDP Comparison of SWCNT and SLGNR. Simulation results shows that SWCNT has lower PDP when compared to SLGNR by a factor of 10 at the global interconnect level. SWCNT approximately constant PDP in local, semi global and global interconnect levels.

Table-1. Comparison of PDP

Interconnect level	22nm SLGNR	22nm SWCNT	22nm Cu
Local	53.4 aJ	4.04 aJ	1.44 pJ
Semi-global	66.3 aJ	4.836 aJ	1.8 pJ
Global	80.25 aJ	6.24 aJ	2.1 pJ

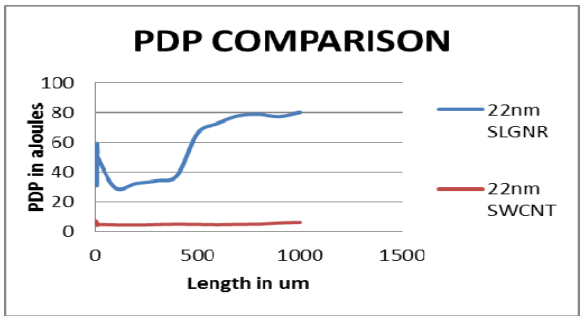

Figure-11. Comparison of power delay product of SWCNT and SLGNR

Bandwidth

Bandwidth comparison of copper, SWCNT and SLGNR for 22nm and 14nm technology nodes is shown in Table-2. Bandwidth is calculated by 0.35/rise time. SLGNR have wide bandwidth compare to copper and SWCNT interconnect. SLGNR is more suitable candidate for high speed operation for future interconnects technology.

Table-2. Comparison of Bandwidth

Technology nodes		Interconnect level (in µm)		
		Local	Semi-global	Global
22nm	Copper	32MHz	8MHz	7.5MHz
	SWCNT	735MHz	302MHz	54MHz
	SLGNR	58GHz	8GHz	3GHz
14nm	Copper	29MHz	-	-
	SWCNT	736MHz	302MHz	54MHz
	SLGNR	70GHz	9GHz	3.4GHz

CONCULSIONS

In this paper, we have compared the performance of carbon nano structures (such as SWCNT and SLGNR) with Cu interconnect for on-chip interconnects applications. Carbon nano structures have less delay and more bandwidth when compared to Cu. SLGNR and SWCNT produces only 0.5% and 0.7% of copper delay in global interconnect level. Carbon nano structures have much higher energy efficiency approximately 1000 times better than copper due to its ballistic transport and excellent thermal and electrical conductivity has less power dissipation compared than Cu. from this, it has been concluded that Carbon nano structures are suitable candidate to replace copper on-chip interconnect to hold the Moore's law for future technology nodes.

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