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DESIGN OF AUTO-GATED FLIP -FLOPS BASED ON SELF GATED MECHANISM

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ABSTRACT

Radiation hardening by design has become a necessary practice when creating circuits to operate within radiated environments. While employing RHBD techniques has tradeoffs between size, speed and power, novel designs help to minimize these penalties. Space radiation is the primary source of radiation errors in circuits and two types of single event effects, single event upsets, and single event transients are increasingly becoming a concern. While numerous methods currently exist to nullify SEUs and SETs, special consideration to the techniques of temporal hardening and interlocking are explored in this work. Temporal hardening mitigates both SEUs and SETs by spacing critical nodes through the use of delay elements, thus allowing collected charge to be removed. Interlocking creates redundant nodes to rectify charge collection on one single node. In this paper presents an innovative, D Flip-Flop in CMOS design. TheFlip-Flop physical design is laid out in the nm process in the form of an interleaved multi-bit cell and the circuitry necessary for the Flip-Flop to be hardened against SETs and SEUs is analysed with simulations verifying these claims. Comparisonare made to an unhardened D Flip-Flop through speed, size, and power consumption depicting how our technique used increases all three over an unhardened Flip-Flop. Finally, the blocks from both hardened and unhardened Flip-Flop being placed in work and run in 4-bit counter design flows which are compared through size and speed to show the effects of using the high density multi-bit layout.

Keywords: D-Flip-Flop, counter, clock gating, low power.

INTRODUCTION

Flip-Flops and latches are used as data storage elements. Such data storage can be used for storage of state, and such a circuit is described as sequential logic when used in a finite –state machine, the output and the next state depend not only on its current state (and hence previous input). It can also be used for counting of pulses and for synchronizing variably –timed input signals to some reference timing signals. Flip-Flop can be either simple (transparent or opaque) or clocked (synchronous or edge triggered).

Flip-Flops and latches are a fundamental building block of digital electronics systems used in computers, communication and many other types of systems , such a circuit is described as sequential logic. For this low power process D-Flip-Flop is used. The D-Flip-Flop also known as “data” or “delay” Flip-Flop. The term Flip-Flop has historically referred generically to both simple and clocked circuits; in modern usage it is common to reserve the term flip-flop exclusively for discussing clocked circuits: the simple ones are commonly called” Latches”.

In recent trends microprocessor incorporates the functions of a computer’s central processing unit (CPU) on a signal integrated circuits (IC), all modern CPUs are microprocessors making the micro-prefix redundant. The microprocessor is a multipurpose programmable device that accepts digital data as input, processes it according to instructions stored in its memory, and provides results as output it is an example of sequential digital logic, as it has internal memory. Microprocessors operate on numbers and symbols represented in the binary numeral system.

PULSE TRIGGERING FLIP- FLOP

In Existing system, they proposed the design of Flip-Flop based on pulse triggering. Triggering is classified as pulse triggering and edge triggering. That means the pulse generator circuit Figure-1 is combined with D-Flip-Flop circuit for triggered input pulse. Hence the Existing design called as P-FF (Pulse triggered Flip-Flop).the whole design is based on CMOS technology.

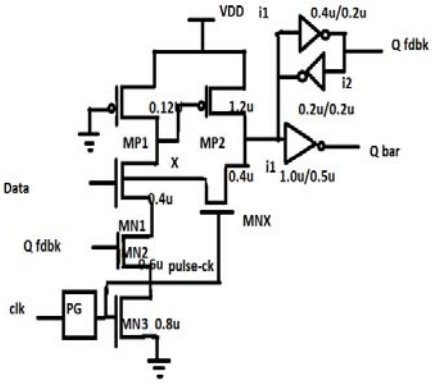

Figure-1. Pulse triggered Flip-Flop circuit.

The pulse triggered method means that the data entered in to the Flip-Flop on the rising edge of the clock pulse, but the output does not reflect the input state until the falling edge of the clock pulse. And also that they applied signal feed through scheme used to reduce the delay transition during data transmission. Then, they are conditional discharging method was focused. Here, they

propose a design of low power Flip-Flop using CMOS technology.

EXISTING SYSTEM

In the Existing design they designed D flip flop, based on pulse triggering. That means the Pulse generator circuit is combined with D flip flop circuit for Triggered input Pulse. Hence the Existing Design Called as P-FF (Pulse-triggered Flip flop). The whole design is based on CMOS technology.

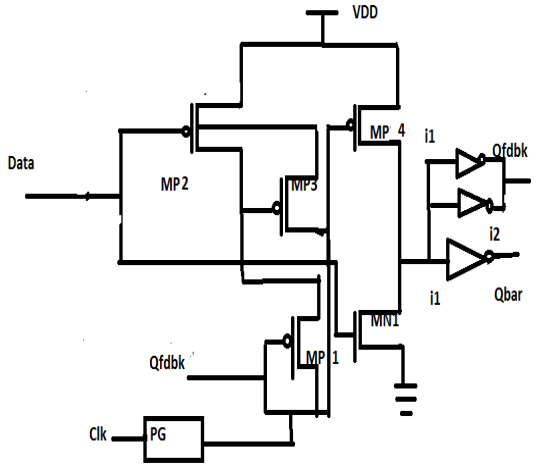

Figure- 2. Existing circuit.

The pulse-triggered method means that the data entered into the Flip-Flop on the rising edge of the clock pulse, but the output does not reflect the input state until the falling edge of the clock pulse. And also there they applied Signal feed through scheme used to reduce the delay transition during data transmission. Then, there the conditional discharging method was focused. Here, we propose a design of low power Flip-Flop using CMOS technology. As the drawbacks, more number of transistor was used in existing design, which consumes amount of power. And requires relatively high write energy to Flip-Flop. Since in this system, thereis more number of inverter gates are used in triggering Flip-Flops. This may consume power.

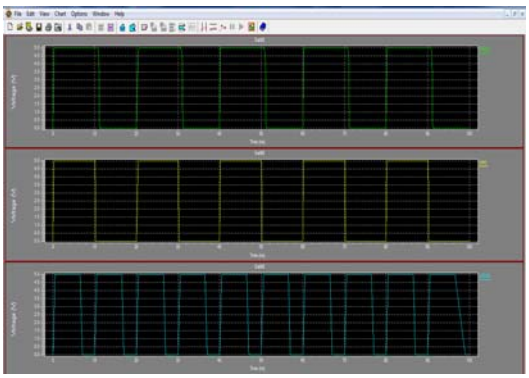

Figure-3. Output wave form for existing circuit.

PROPOSED SYSTEM

In our proposed work, we implement reduction of CMOS design in DFF with the help of virtual grounded NMOS design to reduce delay level in 4-bit counter circuit.

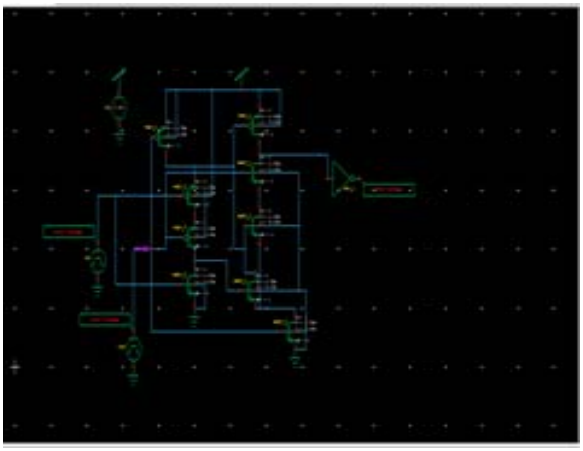

Figure-4.DML Shift Registers in a D Flip-Flop memory.

Flip-Flops, like latches, provide synchronous data transfer and storage. However, unlike latch elements, a only copies the data from the input pin to the output once per clock period and does not allow Flip-Flop multiple logic values to be passed in a clock cycle.

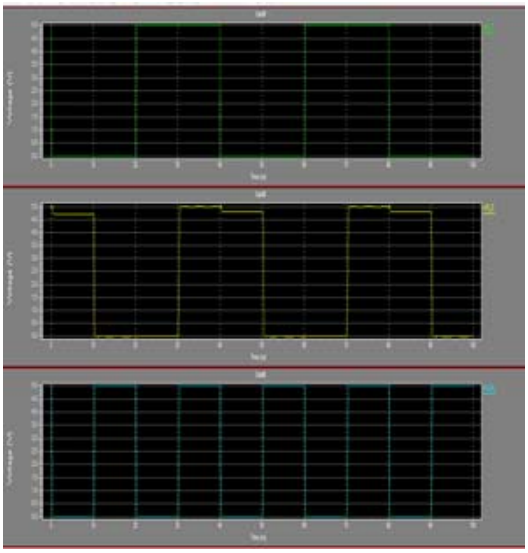

Figure-5. Output Waveform for DML Shift Register in a D Flip-Flop memory.

Data is transferred at either the rising or the falling clock edge, depending on the flip-flop configuration. The flip-flop only changes state by capturing D values at the two rising clock. This is compared to the combinational timing, where data can pass freely through the block regardless of clock phase.

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In a master slave Flip-Flop, this behaviour is produced by a circuit combining two latches in series with opposite clock polarities. For example, a transparent high master latch followed by a transparent low slave latch will create a negative pulse triggered Flip-Flop. Complementary clock signals are needed in all Flip-Flop designs to insure that the master and slave latches are not transparent at the same moment and are usually generated locally within the cell. In the event that clock edges do not rise or fall quickly, Flip-Flops have the possibility of failing to regulate data flow if both latches are transparent at the same time.

Truth Table-1. D Flip-Flop.

Clock	Din	Out
0	X	No change
1	0	0
1	1	1

Delay: 70 to 100p

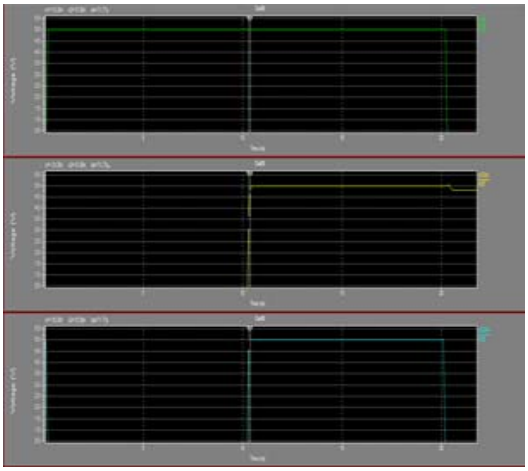

Figure-6. Output waveform for delay In 70 To 100p.

Comparison table for delay.

Parameter	Existing	Proposed
Delay	158 p	70 to 110p

As the advantage, of the proposed system, we proposed new form of D-Flip-Flop by using edge triggering Flip-Flop with virtual ground architecture using edge triggering Flip-Flop with virtual ground architecture which may reduce power consumption than in existing system. This reduces the number of CMOS in D-Flip-Flop and also reduce delay rate of Flip-Flop.

Design 4-Bit counter

From the circuit implemented in the D- Flip Flop using Proposed DDFF structure in CMOS design, we further use the D-Flip-Flop structure in 4-bit counter design.

In this we further note the combinational circuit and we can eliminate the components which are not needed and which may consume more space. Figure-7 shows 4-bit counter design of proposed DFF.

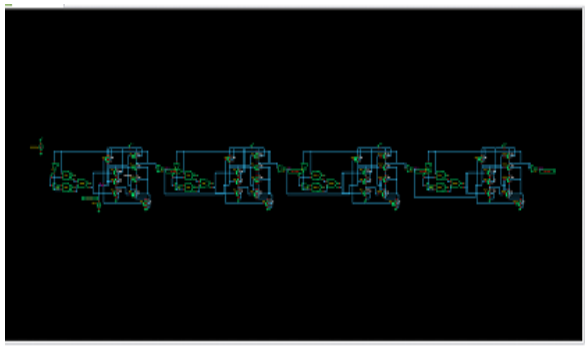

Figure-7. 4-Bit counter design.

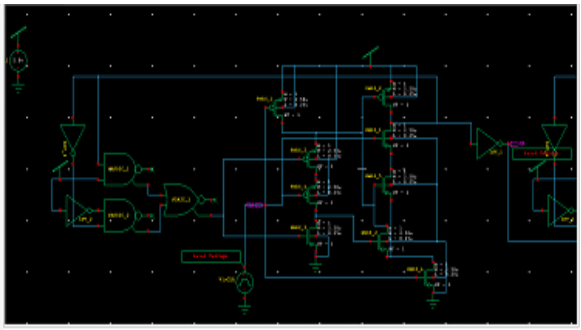

Figure-8. Single bit counter design.

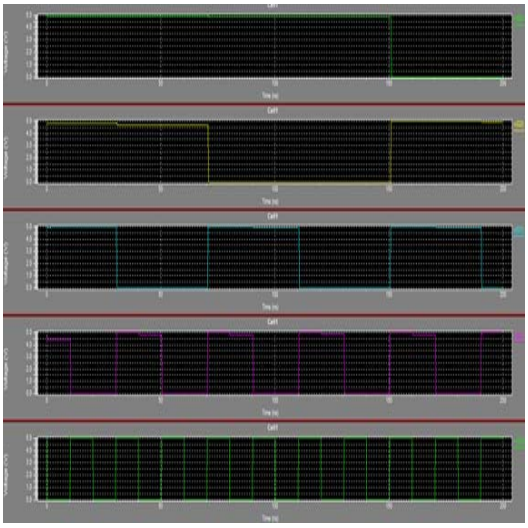

Figure-9. Output waveform for single bit counter design.

Truth Table-2. 4-Bit counter design.

Q0	Q1	Q2	Q3
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

SYSTEM REQUIREMENTS

Hardware requirements

- Pentium IV – 2.7 GHz
- 1GB DDR RAM
- 250Gb Hard Disk

Software requirements

- Operating System : Windows XP
- Tool : Tanner EDA 13.0

Block diagram

MODULE DESCRIPTION

CMOS design

Complementary metal oxide semiconductor (CMOS is a technology for constructing integrated circuits).CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor),data converters, and highly integrated transceivers for many types of communication. Two important characteristics of CMOS devices are high noise immunity and low static power consumption.

TRIGGERING

Basically the triggering methods are pulse triggering and edge triggering. an edge-triggered Flip-Flop changes states either at the positive edge(rising edge)or at the negative edge(falling edge) of the clock pulse on the control input. The term pulse triggered means that data are entered in to the flip-flop on the rising edge of the clock pulse, but the output does not reflect the input state until the falling edge of the clock pulse.

Clock gating

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic circuit to pure clock tree.

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic circuit to pure clock tree. Purring the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states.

Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred.

D-FLIP-FLOP

In electronics, a Flip –Flop or latch is a circuit that has two stable states and can be store state information. The D-Flip-Flop is widely used and it is also known as a "DATA" or "DELAY" Flip-Flop. The D-Flip-Flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock pulse) that captured value becomes the Q output. at other times, the output Q does not change. The D-flip-flop can be viewed as a memory cell.

Design 4-Bit Counter

From the circuit implemented in the D- Flip Flop using Proposed DDFF structure in CMOS design, we further use the D-Flip-Flop structure in 4-bit counter design. In this we further note the combinational circuit and we can eliminate the components which are not needed and which may consume more space. Fig shows 4-bit counter design of proposed D-Flip-Flop.

DESIGN

Construct CMOS design

In this module, we construct the design of CMOS architecture with PMOS and NMOS. This provide dynamic mode Flip-Flop to construct 4-bit counter.

Construct NAND gate

In first step, we design NAND gate architecture with CMOS technology to construct a Flip Flop. This combination gives reduced design of traditional CMOS architecture.

Construct 4 - bit counter

In this stage, we construct final design of 4-bit counter using 4-Flip-Flop of our proposed D Flip-Flop architecture. This design was finally compare to existing CMOS architecture with 4-bit counter.

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RESULTS

Parameter	Existing system	By swapped MOS design	By D-Flip-Flop
Number of transistors in flip-flop	12	11	11
Layout area	69.13mm2	63.39mm2	69.13mm2
Average minimum running time	--	1.4s	1.2s
Delay	109ps	90ps	85ps

DISCUSSIONS

In existing system, they proposed design of D-Flip-Flop based on Swapped MOS design. The pulse trigger method that the data entered in to the Flip-Flop on the rising edge of the clock pulse, but the output does not reflect the input state until the falling edge of the clock pulse. And also they are applied signal feed through scheme used to reduce the delay transition during data transmission. Since the power consumption and delay, area will be reduced.

For this low power process, D-Flip-Flop is used. It also used to implement the tanner tools to achieve the better power, delay, area and speed.

In particular digital design nowadays often adopt intensive pipelining techniques and First In- First Out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements is as high as 50%of the total system power. Flip-Flops thus contribute a significant portion of the chip area and power consumption to the overall systems. Pulse triggered Flip-Flop, because of its single latch structure is more popular than the conventional transmission gate and Master –slave based FFs in high speed application. By the proposed design provides promising result than existing system and using 4-bit counter application and clocking gate. Our work concentrated on reduction of power and reduced area consumption, and also area efficiency, by reducing number of transistors. Thus from the overall parameters we have achieved better performance than the existing design of Flip-Flop.

CONCLUSIONS

In this paper, thus from existing design D Flip-Flop is proposed in our work with dual dynamic CMOS technology. In the existing design they proposed the conventional D Flip-Flop that was designed for the purpose of power reduction and also it concentrates in some other factors. In our previous work also we designed based on swapped MOS design. By this proposed design provides promising result than existing system. Even though it produce power reduction and reduced area consumption, and also area efficiency, by reducing number of transistors. Thus from the overall parameters we achieved better performance than the existing design of Flip-Flop. For this design of proposals designed in CMOS design methodology and used in Tanner EDA 13.0 as simulation tool to show the performance analysis of our work.

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