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A DESIGN OF SRAM STRUCTURE FOR LOW POWER USING HETEROJUNCTION CMOS WITH SINGLE BIT LINE

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ABSTRACT

The Present day workstations, low-power processors, computers and super computers are using fast Static Random Access Memory (SRAMs) and will require, in the future, larger density memories with faster access time and minimum power consumption. Acknowledging the intense requirements for power, in current high performance memories of computing devices, the circuit designers have developed a number of power optimizing techniques which target several sources of energy dissipation in an SRAM. The total power dissipated in a typical SRAM architecture is the active and standby power. The access to the memory cell is performed through word line and bit line. The hetero junction concept of SRAM was simulated. The single bit line for a 16 SRAM cell was implemented in an array fashion and the power results are computed and compared with multiple individual SRAM cell structures .The results show that single bit line results in 2.5 times reduction of power. The simulation results are obtained from tanner 14.1 environments.

Keywords: SRAM, single bit line, hetero junction.

INTRODUCTION

In the domination of digital VLSI designs, on chip memory is more essential. Technology scaling leads to increase in dynamic power and leakage with each generation due to integration of more functions in die. Most portable devices rely in power consumption as they relate to battery life. One of the most effective ways to reduce the power is by scaling the voltage and frequency. The two major sources of power dissipation include the static and dynamic power dissipation. In the SRAM cell, the operation is enabled by the Word Line (WL) which controls the two access transistors which, in turn, control whether the cell should be connected to the Bit Lines (BL). They are used to transfer data for both read and write operations. Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply. Thus, the term adiabatic is used in low-power VLSI circuits which implements reversible logic. The concept of hetero junction reduces the power consumption as the number of interconnects are decreased. The individual cell uses separate access transistors connected to the bit lines. This causes increase in capacitance effect. This effect can be eliminated by the single bit line approach. This paper discusses about the existing literatures followed by operational principles of SRAM proceeded with proposed hetero junction technique and finally the implementation of single bit line approach and the results compared with conventional method simulated using tanner tool.

STATE OF ART

Low power plays a key role in VLSI designs. There exist many designs for energy efficient SRAM cell such as sleep, stack, sleepy stack and leakage feedback approaches. S. Nakata proposes adiabatic SRAM [1] that changes the memory-cell power line or memory-cell ground line (MCGL) gradually during write operation to solve the VT (Threshold Voltage) variation problem. It further proposes that the single-BL SRAM has a larger Static Noise Margin (SNM) than the two-BL SRAM and that the BL pre charge voltage can be the lower value in the range of VDD/2 to 3VDD/4 instead of VDD. It discusses on a sense amplifier (SA) that does not need medium reference voltage between the low BL level and the high one. During write mode, word divided architecture is implemented in lower BL state to maintain the SNM of unwritten blocks. The discussion in [2] shows that how a combinational and sequential adiabatic switching logic circuits may be constructed with the timing restrictions required for adiabatic operation. With increased device variability in nanometer scale technologies, SRAM becomes increasingly vulnerable to noise sources. The wider spread of local mismatch leads to reduction in SRAM reliability. For the demand of minimizing power consumption during active operation, supply voltage scaling is often used. However, SRAM reliability is even more suspect at lower voltages. VCC_{min} is the minimum supply voltage for an SRAM array to read and write safely. Static Noise Margins (SNMs) are widely used as the criteria for stability. SNM is defined as the minimum DC noise voltage needed to flip the state of the cell, and is used to quantify the stability of a SRAM cell using a static approach.

The stability problem [3] can be eliminated by separate read and write word lines and can accommodate dual-port operation with separate read and write bit lines. Without read disturbs, the worst-case stability condition for an 8T cell is that for two cross-coupled inverters, which provides a significantly larger SNM. The leakage energy reduction is performed in [4] by activating the sleep mode of an SRAM cell by gating the supply voltage of the cell through two NMOS transistors. This allows

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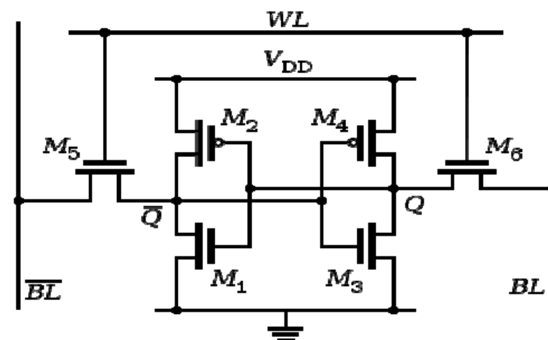
reducing the standby leakage current without introducing extra circuitry, auxiliary signals, or capacitive loads on the conventional SRAM peripheral circuits, such as the word line driver, the sense amplifiers, or the pre charge circuits. This structure establishes when to enter and to exit the sleep mode, on the basis of the data stored in it, without introducing time and energy penalties with respect to the conventional 6-T cell. Consequently, this approach does not introduce time and dynamic energy overhead over the basic 6-T SRAM cell.

The enhanced boost logic [5] uses four supply levels and adopts the Logic stage which drives the dual-rail output conventionally with sub threshold-level energy consumption in the first half of each clock cycle. Subsequently, during the second half of each cycle, the Boost stage amplifies the near-threshold voltage between the two outputs to full rail using the two complementary clock phases to design a FIR filter. The methodology in [6] proposes a very low cost Design-for-Diagnosis (DfD) solution for design of write driver circuit and to improve access time in write operation, in which two decoders and one sense amplifier are used in each column of 10T Static Random Access Memory (SRAM) cell. The idea [7] differentiates conventional SRAM that uses two pre charged BLs for reading. The problem is that the low-voltage node of an FF increases from 0 V. In contrast, a single-BL SRAM which uses only one BL for reading. When $V1 = 1$ and $V2 = 0$, $V2$ is not connected to the pre charged BL and it remains at a low level. Therefore, a single-BL SRAM has a larger SNM than one with two BLs.

The target on high speed, low leakage, low active energy applications is focused on [8] by dividing the bit lines to improve dynamic cell stability while at the same time decreasing active energy consumption. To limit unnecessary activity, word lines are divided on a word-by-word basis. Local write sense amplifiers make it possible to use low swing signaling on the global bit lines. A distributed decoder is used to control this architecture. The use of dual swing data links on the global bit lines limits the impact of local write sense amplifier offset on the overall energy consumption. Using high threshold transistors in the memory cell reduces static power consumption and improves the cell's read stability. D.Ho discusses [9] about the leakage reduction achieved by supply voltage scaling and high threshold transistors. The leakage can be reduced due to smaller voltage differences between drain, source and body of a transistor and sizing above the minimum gate length. Thus the memory cell with minimum power is the key goal of the emerging work.

STATIC RANDOM ACCESS MEMORY

Static Random Access Memories are read/write (R/W) memory circuits which permit the modification of data bits stored in memory cells as well as their retrieval on demand. The term static means that as long as sufficient power supply voltage is provided, the stored data is retained indefinitely. The word Random access indicates that the access time is independent of the physical location of the data to be stored/read in the memory array. SRAM features high speed and therefore is used for the main memory in super computers or cache memory of mainframe computers. The data storage cell, i.e., the one bit memory cell in the static RAM arrays, invariably consists of simple latch circuit with two stable operating points. Depending on the preserved state of the two inverter latch circuit, the data being held in the memory cell will be interpreted either as logic '0' or as logic '1'.To access the data contained in the memory cell via a Bit Line (BL), we need at least one switch, which is controlled by the corresponding Word Line (WL).



WL= Word Line, BL = Bit Line

Figure-1. 6T Static RAM.

The increase in memory size in recent RAM technologies causes an un avoidable increase in word line length, which eventually increases the physical capacitance and power consumption, and thus leading to speed degradation. The bit line capacitance is mainly composed of the drain capacitance of pass transistors in each SRAM cell and the metal capacitance of the bit lines. Another effective approach to reduce active power consumption is to shorten the duration of the active duty cycle, which is provided when read/write operation can be performed after the arrival of the address signals.

There exist two states in the active SRAM cell. 'Reading' is the state when the data has been requested and 'Writing' is state when the data is being updated. In order to write a logic '0', set BL to '0' and BL' to '1'and the word lines are made high (transistor's M_5 and M_6 turns ON). The logic '0' in the bit lines enters to the first cross coupled inverter and turns ON transistor M_2 and turns OFF transistor M_1 and hence V_{DD} flows through M_2 and remains high. As shown in Figure-1, BL' is made logic '1' then transistor M_3 turns ON and M_4 goes OFF, thereby keeping Q as '0'. Similarly to write logic '1'Set BL to '1' and BL' to '0'and the word lines are made high (transistor's M_5 and M_6 turns ON). The logic '1' in the bit lines enters to the first cross coupled inverter and turns ON transistor M_1 and turns OFF transistor M_2 and hence BL' is connected to ground via transistor M_1. On the other hand, when BL' is made logic '0' transistor M_4 is ON and M_3 is OFF, thereby V_{DD} keeps BL at logic '1' through transistor M_4 .

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In the read mode to perform the read operation of logic'0', the bit lines BL and BL' are pre charged to '1'. The word lines are made high (transistors M_5 and M_6 turns ON). M_2 and M_3 are ON and M_1 and M_4 are OFF. Hence V_{DD} flows to the bit line BL' through M_5 and M_2 keeping it in logic state '1'. The bit line BL is connected to ground through the transistors M_6 and M_3 making it into logic state '0'.In the same way to read a logic '1', the bit lines BL and BL' are pre charged to '1'. The word lines are made high (transistors M_5 and M_6 turns ON). M_1 and M_4 are ON and M_2 and M_3 are OFF. Hence bit line BL' is connected to V_{SS} making it into '0'. On the other hand the bit line BL is connected to V_{DD} through the transistors M_6 and M_4 keeping it in logic state '1'.

A Conventional 6T SRAM cell with two bit lines is shown in Figure-2. The Read, write and hold operations in 6T SRAM, with generic 250 nm technology is shown below.

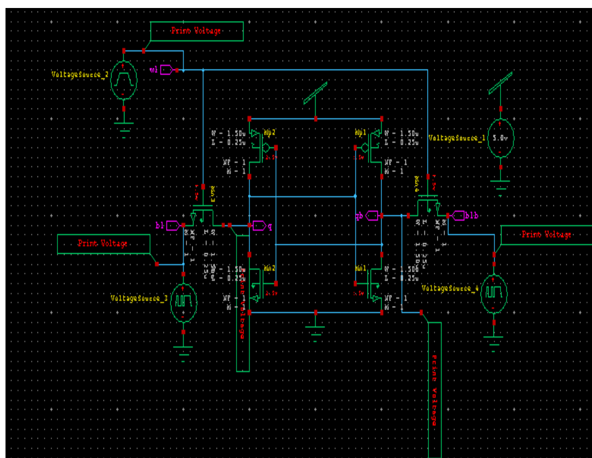

Figure-2. 6T SRAM using 250nm technology.

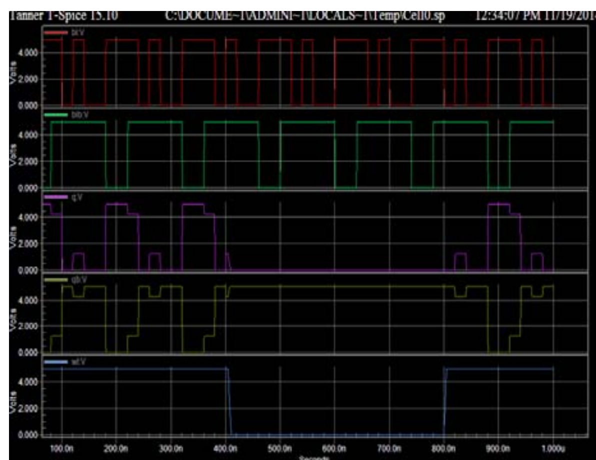

Figure-3. Write, Read and standby operating modes.

Figure-3 represents the standby, read and write mode of operations for a 6TSRAM where a word line, bit line and bit line bar are raised high for reading. The total power consumed for the above simulation is 2.46 milli watts.

ADIABATIC CIRCUITS

Adiabatic is the term given to low-power electronic circuits that implement reversible logic. The term comes from the fact that an adiabatic process is one in which the total heat or energy in the system remains constant. Research in this area has mainly been fueled by the fact that as circuits get smaller and faster, their energy dissipation greatly increases, this is a problem that adiabatic circuits promises to solve. Most methods have focused on building adiabatic logic out of CMOS. However, current CMOS technology, though fairly energy efficient compared to similar technologies, dissipate energy as heat, during switching. In order to solve this problem, the two fundamental rules CMOS adiabatic circuit follows, is never to turn on a transistor when there is a voltage difference between the drain and source and never to turn off a transistor that has current flowing through it.

The switching activity in [9] causes power dissipation in CMOS transistors. The main part of this dissipation is due to charging and discharging of the gate capacitance C through a component that has some resistivity R. The energy dissipated when one charging of the gate is $E = (RC/T)*CV^2$ Where T is the time taken for the gate to charge or discharge. In non-reversible circuits, the charging time T is proportional to RC. Reversible logic uses the fact that a single clock cycle is much longer than RC and thus attempts to spread the charging of the gate over the whole cycle and thus reduces the energy dissipated. In order to extend the charging time of the gate, the transistor should not be turned on when a potential difference exist between source and drain, and furthermore, once the transistor is turned on, energy flows through it in a gradual and controlled manner. The other rule that adiabatic circuits [10] is never to be turn off a transistor when there is current flowing through it, because transistors are not perfect switches going from on to off instantly. Instead, it gradually changes from on to off when the gate voltage changes. Furthermore, the change is proportional to the speed at which the gate voltage changes. A fact that when combined with the previous constraint, implies that the transistor is in an "in between" state for a long period of time. During this time, the voltage drop across the transistor greatly increases, yet the resistance is not high enough to bring power dissipation to zero.

SINGLE BIT LINE APPROACH

The single bit line comprises of array of SRAM cells. The 16 cells are connected to the BL. The BL is connected to the Global Bit Line (GBL) via the write and read ports. These are activated by WPSW (Write Port Switch Signal) and RPSW (Read Port Switch Signal). The RWL goes high during reading. While both Read Word line and Write Word Line goes high during writing. For reading, the RPSW is kept low and when V1 is low, the

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GBL changes from pre charge voltage to read port supply voltage. When V1 is high, GBL does not change. It uses read port to reduce the bit line capacitances. In general, when access transistors are individually connected to the bit line, the capacitance effect increases. This can be overcome by combining the SRAM cells and sharing a single bit line approach. This methodology reduces the capacitance effect and thus decreasing the power consumption.

HETERO JUNCTION CMOS

The proposed idea of hetero junction is that there exists a junction between two different nodes; which functions as a diode. Hetero structure uses gate-controlled modulation and fully compatible with current MOSFET. In MOSFETs, the source and Drain are interchangeable, with the distinction only determined by the voltages during operation. Our proposal is designing low-power SRAM architecture based on hetero junction CMOS Mechanism that can be applied in Wireless Sensor Networks. The Conventional SRAM structure has two pre-charged BL whereas a Single BL SRAM uses only one Bit-Line for read operation. In [6] adiabatic circuits are used to conserve energy using Single Bit line scheme with an objective to have a larger Static noise margin than Two-BL SRAM. In the proposed methodology a Single BL SRAM design based on hetero CMOS design provides less power consumption. The implemented results show that the part of Hetero junction CMOS circuit makes the read operation with reduced power consumption.

Static Random Access Memory (SRAM or static RAM) is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. So the Read/Write operation updates the data per every refresh. Bit-line and word-lines are used for the process of SRAM. In MOSFETs, the source and drain are interchangeable, with the distinction only determined by the voltages during operation.

The proposed technique implemented using CMOS circuits are constructed in such a way that, all PMOS transistors must have either an input from the voltage source or from another PMOS transistor. Similarly, all NMOS transistors must have either an input from ground or from another NMOS transistor. The composition of a PMOS transistor creates low resistance between its source and drain contacts when a low gate voltage is applied and high resistance when a high gate voltage is applied. On the other hand, the composition of an NMOS transistor creates high resistance between source and drain when a low gate voltage is applied and low resistance when a high gate voltage is applied.

Bit-lines are perpendicular to the word lines and are physically connected to the source/drains of the cell-transistors. In other words, the bit-lines are the lines through which information is written/read to/from the memory cells. The voltage of each word-line is raised (transistor ON) and lowered (transistor OFF) whereas the columns are named bit-lines. Physically the word-lines are represented by the so called "gate-contact lines" (GC-lines).

They are connecting the gates of all transistors of a certain raw in the array-segment. Thus, when activating / deactivating a word-line, i.e. increasing/decreasing the voltage on/from it, all transistors which are on this raw of the array-segment will open or correspondingly close.

RESULTS AND DISCUSSIONS

The Figure-4 below is the simulated SRAM array with four SRAM cells using the single bit line with hetero junction. The circuit held in CMOS design methodology uses Tanner EDA 14.1 as simulation tool to show the performance analysis.

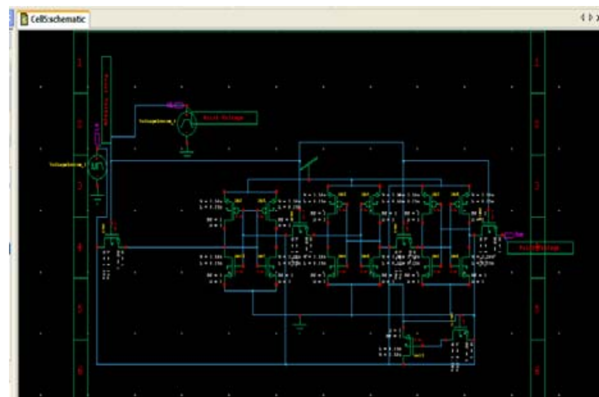

Figure-4. Hetero junction SRAM structure.

The simulation result shows the input and output. The signals in bit line, word line and the corresponding output are shown below in Figure-5.

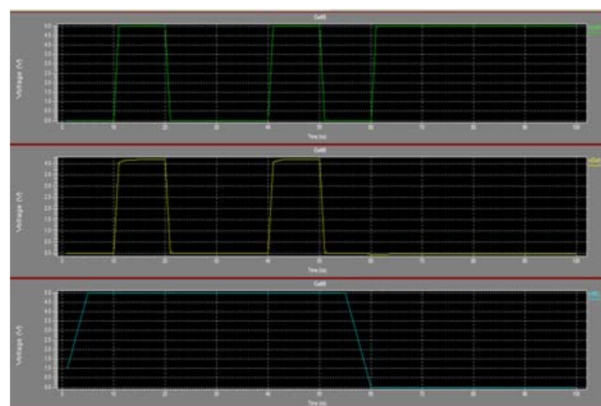

Figure-5. Operation of Hetero junction SRAM.

The power in Figure-6 is measured at the output for the simulation time of 1000ns and the maximum power is found to be 150 microwatts.

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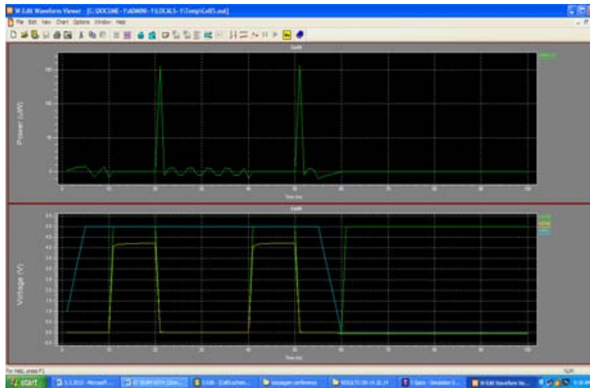

Figure-6. Power measurement in hetero junction SRAM structure.

The single bit line structure for an array of 16 SRAM cells is shown below

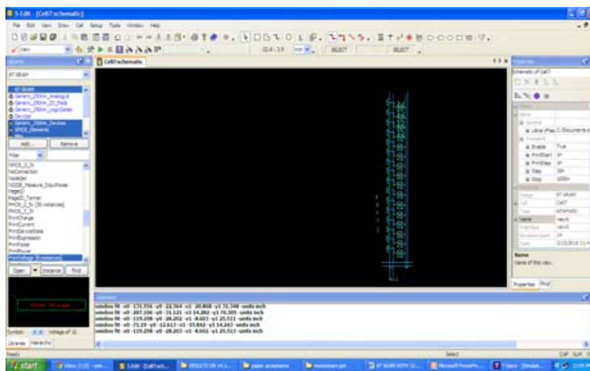

Figure-7. Single BL SRAM array.

In the array structure Figure-8 shows the zoomed view of a single SRAM cell in the SRAM array.

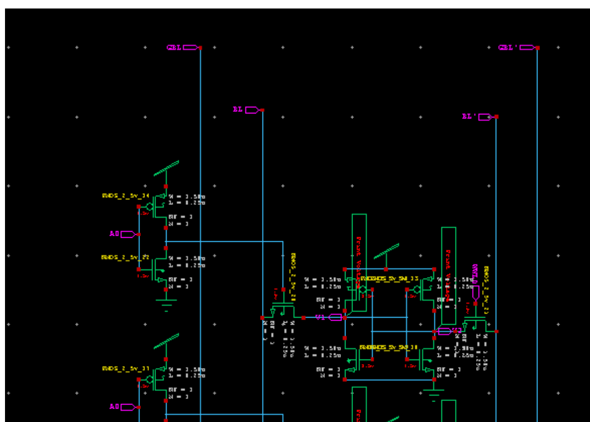

Figure-8. Single SRAM view in an array.

The simulation result for the single BL SRAM array is shown in Figure-9. The results for transient response at nodes V1, V2 for the SRAM cell and the power consumed by the structure for the simulation time of 1 micro second is found to be 15 milli watts.

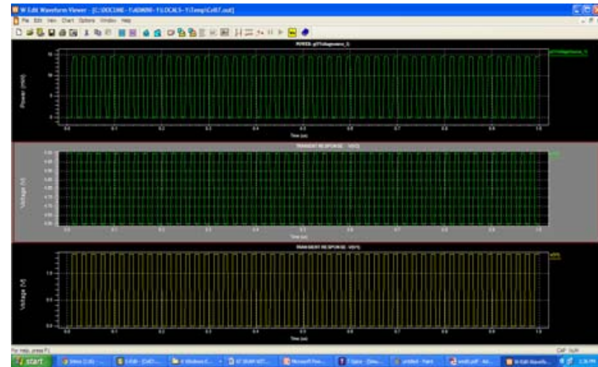

Figure-9. Transient responses and power results.

Thus the comparison results for 16 conventional 6T SRAM cells ,and single bit line approach for the SRAM array of 16 cells shows that the former results in 39.36 milli watts where as the later consumed 15 milli watts of power, which is approximately 2.5 times reduction in power.

CONCLUSION AND FUTURE SCOPE

Thus designing a SRAM array with energy efficient SRAM cells has been most often used in the VLSI design. Power dissipation of memory circuits has been the focus of many research efforts during recent years. This paper discusses single BL, hetero junction to achieve power reduction and compares the result with conventional approach.

In future this technique can be analyzed by scaling down the device. Another factor is that the supply voltage scaling can be enhanced in a bit cell that works down till 0.7-0.5V. The voltage adaptability can be achieved for negative bit line write assist technique enabling easier write operation, especially at lower voltages. When scaling below 45 nm, the leakage issues dominates the power consumption. Thus special techniques could be enhanced for these SRAM cells to achieve power reduction. The Portable devices adopted with this SRAM cell could have better battery backup.

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