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TESTING OF STUCK AT FAULTS IN REVERSIBLE SEQUENTIAL CIRCUITS USING VERILOG HDL

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ABSTRACT

Conservative logic is one of the best nano technologies to design digital circuits. This paper proposes testable reversible sequential circuits based on conservative logic. Any sequential circuit can be tested for classical unidirectional stuck at faults 1's using only two test vectors. The completely testable sequential circuits design based on conservative logic gates using fault leeway model is proposed here. The proposing fault leeway model consist of two test vectors all 0's and 1's. The proposing design of D latch, master slave flip-flop, DET flip-flop is done with the help of conservative logic gate (Fredkin gate). This results in reduction of testing time. With that result the proposed work takes some advantages such as reduced number of gates, reduced power consumption and reduced delay time.

Keywords: conservative logic, classical unidirectional stuck at faults, fredkin gate.

INTRODUCTION

Energy dissipation is one of the major issues in present day technology. According to principle of Landauer's, the one bit of information is dissipate as kTln2 joules of energy where k is the Boltzmann's constant and T is the absolute temperature. In order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits. The reversible circuits can generate a unique output vector from each input vector and vice versa that is, there is one-to-one mapping between input and output vectors. Reversible sequential circuits are considered as significant memory block for their ultra-low power consumption.

Conservative logic is called by reversible conservative logic when there is a one-to-one mapping between the inputs and the outputs vectors along with the property that there are equal numbers of 1s in the outputs as in the inputs. The reversible gates used to design the conventional logic are so chosen to minimize the number of reversible gates used. The class of reversible elements that can be modeled as binary-valued logic circuits will be called classical reversible logic elements is the aim of the paper. The design can be completely testable for any unidirectional stuck-at faults by only two test vectors. In the theory of digital circuit, sequential logic is a type of logic circuit whose output depends not only on the present value of its input signals but on the past history of its inputs. The sequential logic has state (memory). In synchronic consecutive circuits, the state of the device changes only at discrete times in reaction to a clock signal.

PROPOSED METHODOLOGY

The objectives need to satisfy the reversible circuit. There are more number of gates present here; the design minimize the number of garbage outputs and Synthesis. In this, the design of two vectors testable sequential circuits based on conservative logic gates are proposed. The sequential circuits based on conservative logic gates outperform the sequential circuits implemented in classical gates in terms of testability is proposed here. Any sequential circuit based on conservative logic gates can be tested for classical unidirectional stuck-at faults using only two test vectors, that are all 1s and all 0s. It's for the designs of latches, master- slave flip-flops and flip-flops are presented. The DET significance of the proposed work lies in the fact that it provides the design of reversible sequential circuits completely testable for any stuck- at fault by all 0s and 1s, so the need for any type of scan-path access to internal memory cells is eliminated. New reversible logic gates are introduced using Boolean expansion but the designs of reversible sequential circuits using Fredkin gate are introduced to minimize the testing time and delay number of garbage outputs.

DESIGN OF FREDKIN GATE

The Fredkin gate is the three-bit gate that swaps the last two bits if the first bit is 1. The basic Fredkin gate is a controlled swap gates that maps three inputs (C, I1, I2) onto three outputs (C, O1, O2).

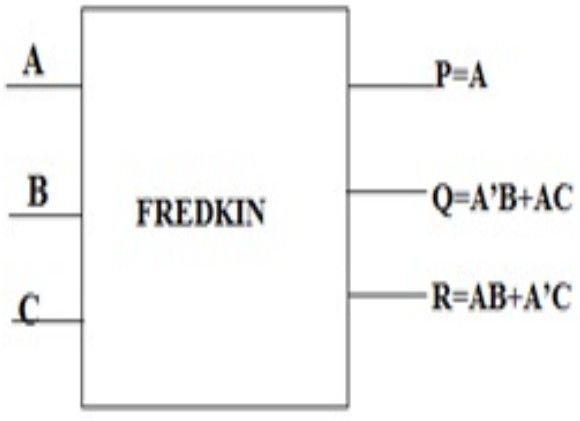

Figure-1. Fredkin gate.

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The C input is mapped directly to the C output. If C = 0, no swap is performed; first input maps to first output, and second input maps to O2. If not, the outputs are swapped. So that first input will map on to second output and second input will map on to first output.

Table-1. Truth for Fredkin gate.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1

a) Design of testable reversible D latch using Fredkin Gate

It has two modes of operation that are normal mode and test mode. In Normal mode, when C1=0 and C2=1 the latch can work as a D latch In Test mode, when C1C2=00, the output T1=0 resulting in making it testable with all zeros input vectors. So stuck-at-1 fault can be detected. When C1C2=11, the output T1=1 resulting in making it testable with all one's input vectors. So stuck-at-0 fault can be detected.

(i) Fredkin gate based D Latch in normal mode: C1 = 0 and C2 = 1

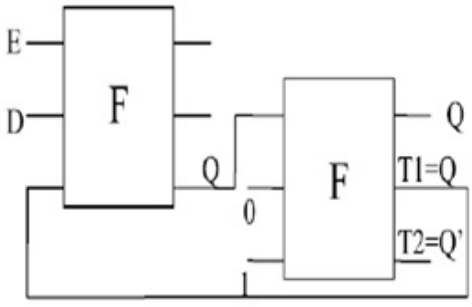

Figure-2. C1 = 0 and C2 = 1.

(ii) Fredkin gate based D latch in test mode for stuck-at-0 fault: C1 = 1 and C2 =1

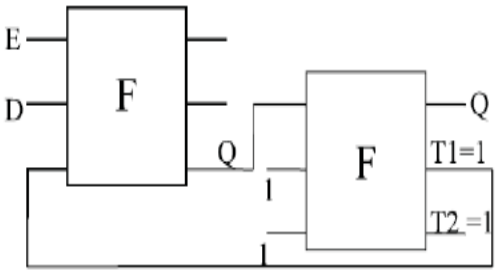

Figure-3. C1 = 1 and C2 =1.

(iii) Fredkin gate based D latch in test mode for stuck-at-1 fault: C1 = 0 and C2 =0

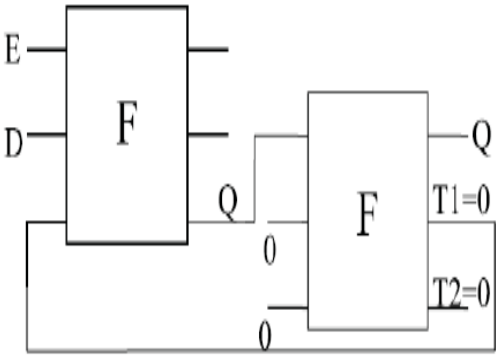

Figure-4. C1 = 0 and C2 = 0.

Table-2. Truth for Fredkin gate based D latch.

E	D	Q
0	D	D
1	D	Previous data

b) Design of testable reversible master-slave flip-flops

The master-slave strategy uses one latch as a master and the other latch as a slave is used to design the reversible flip-flops but the proposed design of testable flip-flops using the master slave strategy that can be tested for any stuck-at faults using only two test vectors, all 0s and all 1s.

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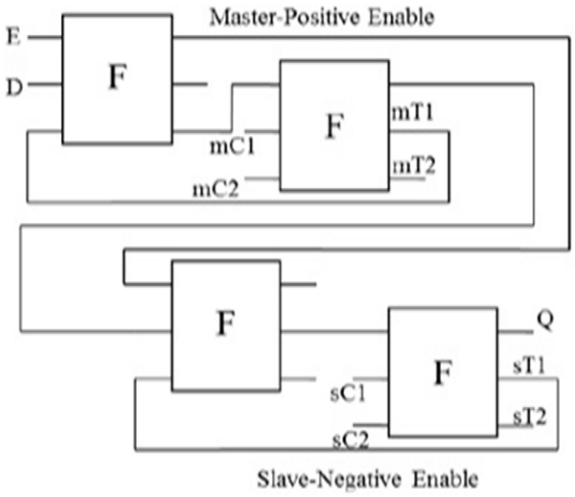


Figure-5. Fredkin gate based reversible master slave flip-flop.

Table-3. Truth for Fredkin gate based reversible master-slave flip-flops.

Truth Table			
Input		Output	
E	D	Q	Not Q
x	0	No Change	No Change
x	1	No Change	No Change
1	0	1	0
1	1	0	1

c) Design of testable double edge triggered flipflop

The DET flip-flop is a computing circuit that samples and stores the input data at both the edges that is at both the rising and the falling edge of the clock. The most popular way of designing the flip flop is the master slave strategy. E refers to the clock and is used interchangeably in place of clock here. In the negative edge triggered master-slave flip-flop when E = 1 (the clock is high), the master passes the input data where the slave maintains the previous state. When E = 0 (the clock is low), the master latch is storage state, at that time the slave latch passes the output of the master latch to its output.

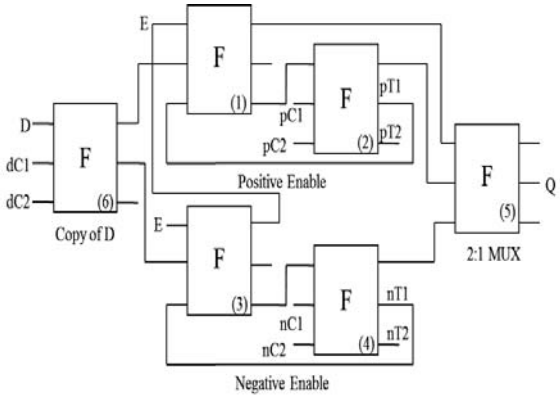


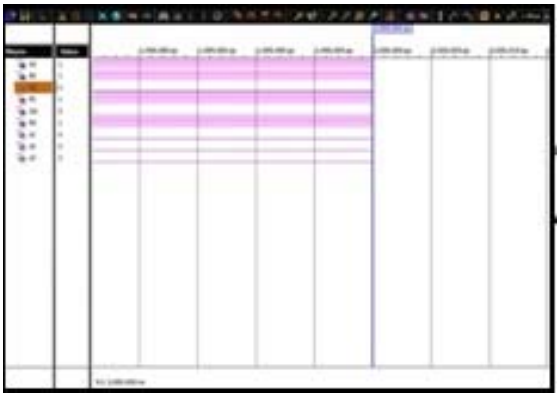
Figure-6. Fredkin gate based reversible det flip-flop.

Table-4. Truth for Fredkin gate based reversible master-slave flip-flops.

Truth Table		
Input		Output
E	D	Q
1	1	1
1	0	0
0	0	No Change 0
0	1	No Change 0

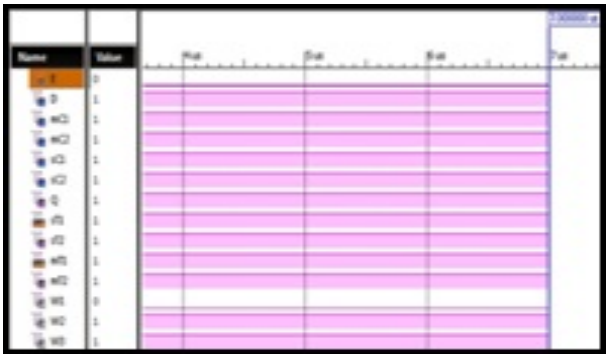
RESULTS FOR PROPOSED SYSTEM SIMULATION

Result for Fredkin gate



Simulation result for fredkin gate based D latch

Simulation result for fredkin gate based master slave flip flop



Simulation result for fredkin gate based det flip flop

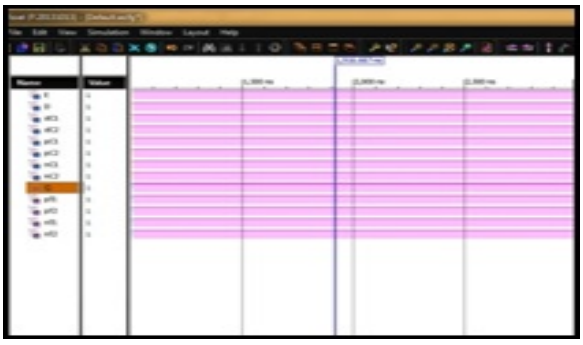


Table-5. Comparison result.

Type	No of Gates		No of constant inputs		No of garbage outputs		Result	
	Existed	Proposed	Existed	Proposed	Existed	Proposed	Existed	Proposed
Master slave DFF	7	4	24	4	14	2	63%	84%
D latch	5	2	20	2	8	2	70%	88%
DETFF	8	6	28	3	19	3	62.5%	85%

CONCLUSIONS

The design of conservative reversible sequential circuit using Fredkin gate is designed. The design is tested using the two test vectors all zeros and all ones. The testing of conservative reversible sequential circuits like Fredkin gate based D latch, Fredkin gate based Master Slave D flip flop can be tested using the test vectors of all zeros and all ones but the double edge triggered flip flop cannot. Due to the faulty parts which are present in the DET flip flop the 100% result is achieved and also the coverage of stuck at zero fault and stuck at 1 fault using two test vectors as all zeros and all ones is achieved for Master Slave D-Flip Flop and D-Latch.

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