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# LEAKAGE REDUCTION USING POWER GATING TECHNIQUES IN SRAM SENSE AMPLIFIERS

Deepak Mittal and Vigneswaran T.
VIT University, Chennai, India
E-Mail: deepak.mittal2013@vit.ac.in

**ABSTRACT**

Now-a-days leakage power is an important issue in microprocessor's and hardware's. In modern computer systems memory components covers 70 to 80 percent of total area of microprocessors that means memory contains more number of transistors. Generally leakage power dissipation proportional to the number of transistors. So the leakage power dissipation is more in the memories. In high performance memories systems sense amplifiers are very important part for sensing the output. In this paper we are focusing on memory leakage power reduction particularly in sense amplifiers using Fine Grain Power Gating (FGPG), Variable Body Biasing Technique (VBBT), Proposed Different Footer Dual Stack Technique (FDST) based both PMOS, one PMOS and one NMOS, both NMOS and Proposed PMOS Footer Triple Stack Technique (PFTST), PMOS Footer Four Stack technique (FFST) in Current Sense Amplifier (CSA), Charge Transfer Sense Amplifier (CTSA) and High Speed Sense Amplifier (HSSA).Variable Body Biasing Technique and PMOS Footer Triple Stack Technique are proposed techniques. We are applying these techniques in Different Sense Amplifiers. Proposed Variable body biasing leakage power dissipation in Current Sense Amplifier 1.5 times less than compare to Sleep Stack, Sleepy Keeper and 0.73 percent less than Forced Stack technique and this technique is much power efficient than other existing techniques. Second proposed Triple stack technique leakage power dissipation in Current sense amplifier is 2 to 3 times less than other techniques and total power dissipation almost 99 percent less than other existing techniques. Proposed techniques are also much efficient for other sense amplifiers.

**Keywords:** SRAM, sense amplifier (SA), charge transfer sense amplifier (CTSA), current sense amplifier (CSA), fine grain power gating (FGPG), footer dual stack technique (FDST), high speed sense amplifier (HSSA), PMOS footer triple stack technique (PFTST), variable body biasing technique (VBBT).

## 1. INTRODUCTION

In modern computer systems, there are many memory components inside one system such as main memories, cache memories and register files etc. When we will focus on higher performance capacity of these systems becomes larger. As CMOS feature sizes shrinking International Technology Roadmap for Semiconductors (ITRS) reports that leakage power become dominated in total power dissipation. There are many reasons for which leakage power dissipation occurs such as Sub-threshold leakage (weak inversion current), Gate oxide leakage (Tunnelling current), Channel Punch through and Drain induced barrier lowering.

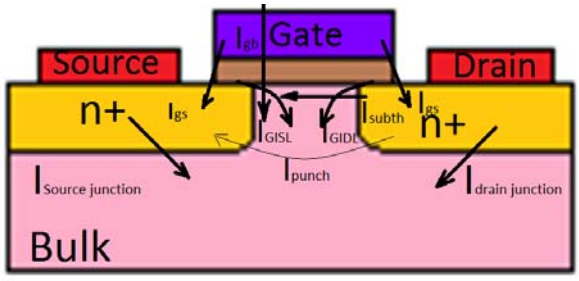


**Figure-1.** Conventional MOSFET with leakage paths.

One of the main reasons of leakage power dissipation is increase of Sub-threshold leakage power. The Sub-threshold conduction or Sub–threshold leakage current is the current that flow between the Source and drain of MOSFET when the transistor is in Sub-threshold region that means gate to source voltage below threshold voltage. When the technology features size scale down, supply voltage and threshold voltage scale down in the same proportion and Sub-threshold leakage power increases when the threshold voltage decreases.

For increasing the performance and channel conductivity when the gate oxide (insulating layer between the gate and channel) made thinner the barrier voltage of oxide changes. For the positive gate voltage some positive charge stuck on gate oxide so current flows that is tunnelling current or gate oxide leakage. Channel punch through effect is the special case of channel length modulation. When the depletion layers around the source and drain merge into single depletion layer causes a rapidly increasing current with increasing drain to source voltage which increases the output conductance which limits the operating voltage which is undesirable.

Next effect is the Drain induced barrier lowering. When the drain voltage higher the charge present on the gate attract more charge carriers for charge balancing which decreases the threshold voltage. A well Known Power Gating technique named as Sleep transistor technique we used for reducing the leakage power dissipation. In this technique cut-off the direct connection supply voltage and/or ground for saving leakage power dissipation. We already know common sleep transistor approaches are Sleepy stack and sleepy keeper. These approaches helps the retaining state faster when the system in inactive states. But these techniques has some

disadvantages, it has delay penalty and area requirement also high. Our motive is to trade-off these disadvantage and limitations with new proposed techniques [1, 2].

## 2. RESEARCH MOTIVATION

CMOS technology is the base of VLSI Design. In above 180nm technology dynamic power dissipation is main factor of total power. But when technology scales down leakage power is dominating on dynamic power. In base technique there is no method for leakage reduction but it saves area and delay. So designers proposed some techniques for reducing leakage. Sleep transistor is the one of the most common method for ultra low leakage reduction but it is not retain the state when the transistor is in inactive state also increase the area and delay penalty. Forced stack technique is another method which retains the state but we cannot use high $V_{th}$ without incurring delay. By combining these two techniques sleepy stack technique is proposed which is saves logic state and leakage power [3]. Generally in conventional CMOS we uses aspect ratio W/L= 3 for NMOS transistor and W/L=6 for PMOS transistor. But in all the techniques we are using here in all transistors aspect ratio W/L =1 for both the NMOS and PMOS because by using minimum aspect ratio the sub-threshold current reduces.

## 3. LITERATURE SURVEY

Stack transistor can reduce leakage so it is stack effect. When the stack transistor is turned off then leakage power reduces.

In this section we will see briefly the previous approaches which are similar to our research. Here previous technique for leakage reduction can be grouped into two categories State saving and state destructive. Previous approaches that are adopted in VLSI design are:

### a) Sleep Transistor techniques (ST)

State-destructive techniques interrupt both PMOS and/or NMOS transistors networks from supply voltage or ground by sleep transistors. These varieties of techniques are referred to as gated Vdd and gated-GND (note that a gated clock is mostly used for dynamic power reduction). Mutoh et al. proposed a method called Multi-Threshold Voltage CMOS (MTCMOS) that adds high-$V_{th}$ sleep transistors between pull-up networks and $V_{dd}$ and between pull-down networks and ground as shown in Figure whereas logic circuits use low-$V_{th}$ transistors so as to take care of logic switch speeds.

The sleep transistors are turned off once the logic circuits don't seem to be in use. By uninflected the logic networks exploitation sleep transistors, the sleep semiconductor devices technique dramatically reduces discharge power throughout sleep mode. However, the extra sleep transistors increase area and delay. The pull-up and pull-down networks have floating values and so can lose state throughout sleep mode. These floating values considerably impact the wakeup time and energy of the sleep technique because of necessarily to recharge transistors that lost state at the time of sleep.

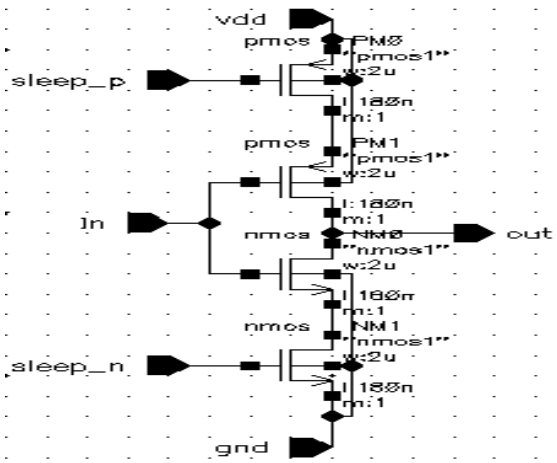


**Figure-2.** Structure of sleep transistor technique.

### b) Forced Stack approach (FS)

This second technique reduces leakage power by using stack the transistors. Figure-3 shows a forced stack inverter. The impact of stacking the semiconductor device leads to the reduction of sub-threshold leakage current when two or more transistors are unit turned off along. Forced stack electrical converter the stacking impact may be understood from the forced stack electrical inverter shown in Figure-3. Here just in case of forced stack inverter two pull up transistors and two pull down transistors area unit used. All inputs share constant input within the forced stack circuit. If applied input is zero then both transistor will turned off.

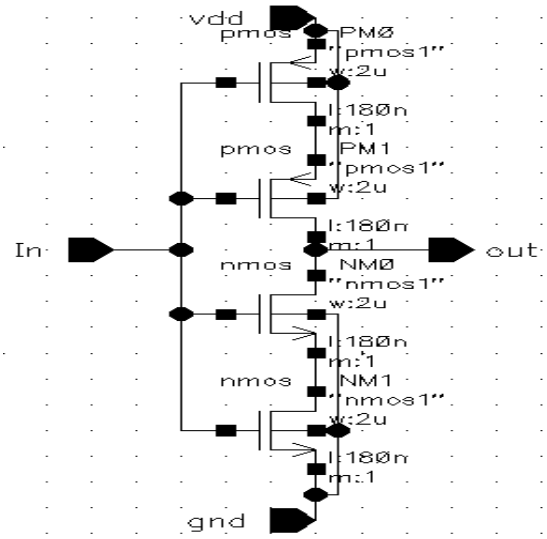


**Figure-3.** Structure of Forced Stack technique.

Here the transistor $NM_0$ has a reduced drain to source voltage $V_{gs}$ because of intermediate node voltage $V_{x,}$ which generates because of voltage difference due to internal resistance of transistor NM1 and this effect reduces drain induced barrier lowering (DIBL) effect and

this technique saves the state. Which means when the transistor is in off state it saves the current state.

We cannot use high $V_{th}$ this is the main disadvantage of this technique because when we will use high $V_{th}$ then delay will increase drastically which will be much more than conventional method.

**c) Sleepy Stack approach (SS)**

In Sleepy Stack Technique we combine Sleep transistor technique and forced stack technique named as Sleepy Stack. Figure-4 of Sleepy Stack inverter circuit is given below.

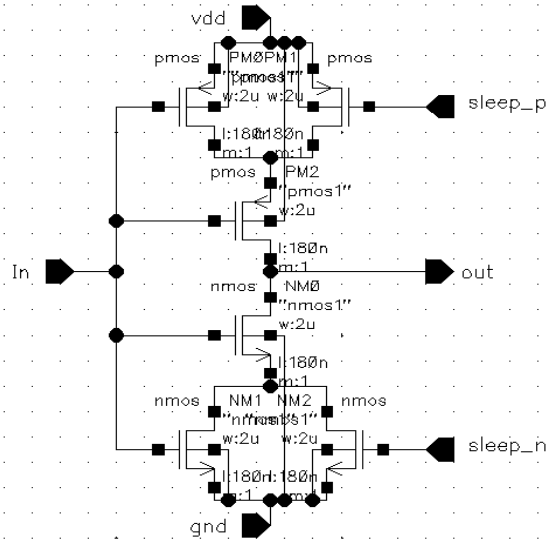


**Figure-4.** Structure of Sleepy Stack technique.

Sleep transistors turned off during sleep mode and turned on during active mode. The functionality of Sleep transistor in Sleepy stack is same as the in Sleep transistor technique. Sleepy stack reduces the delay in circuit in many ways. First when the sleep transistor always is turned on then always the current flow in the circuit so the switching speed increase then delay of the circuit decreases [4, 5, 6].

High $V_{th}$ Sleep transistor without increasing decreases the leakage current in the circuit. Ultra low leakage power consumption during sleep mode we achieve in this technique. But this technique has one drawback that its increase the area.

**d) Sleepy Keeper approach (SK)**

In conventional CMOS method we know that PMOS transistors are placed at pull up network and NMOS transistors are placed at pull down network because PMOS and NMOS transistor are not efficient to passing GND and $V_{dd}$ respectively.

For maintain the output value "1" in sleep mode the sleepy keeper circuit uses this output value and NMOS transistor maintain this value which has been already calculated.

For pull network NMOS has the only source of $V_{dd}$ since the sleep transistor is OFF mode.

An extra transistor is added in parallel to pull-down for connecting to ground in sleep mode. Same as for pull down PMOS is the only option to connecting the GND in sleep mode. This method has advantage that its delay is less than over other methods. But this method has drawback that its dynamic power dissipation has some more than sleepy stack method.

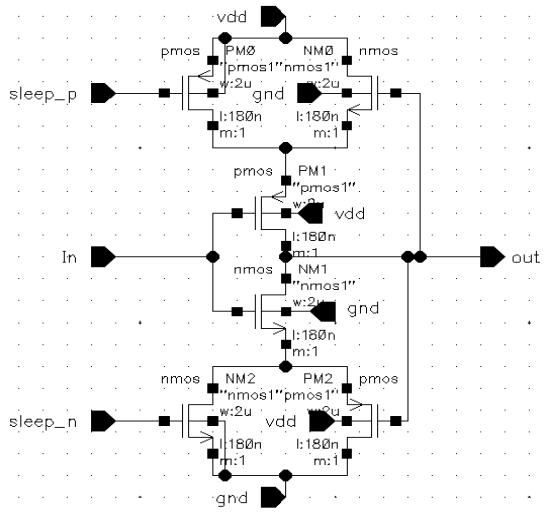


**Figure-5.** Structure of Sleepy Keeper approach.

**e) Dual Sleep method (DS)**

In Dual Sleep Approach we use two transistors PMOS and NMOS. One transistor use turn on in on state mode and another transistor use turn on in off state mode. In off state also its take both PMOS and NMOS for reducing the leakage power.

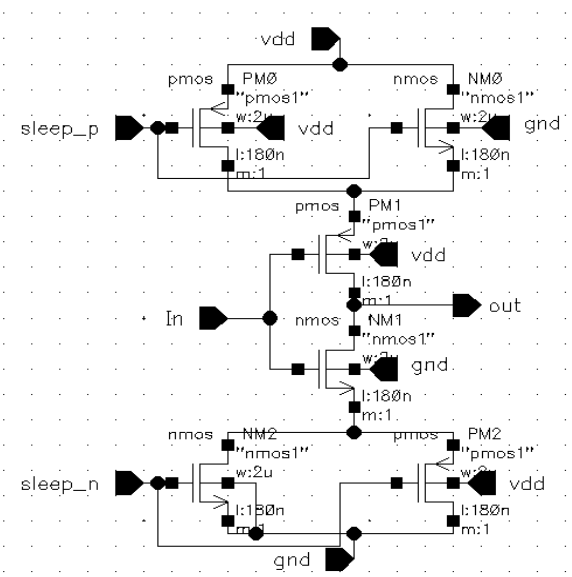


**Figure-6.** Structure of Dual Sleep technique.

In Dual Sleep approach we can apply dual threshold voltage supply for reducing the leakage power dissipation. In Dual sleep approach we use two extra pull-up and pull-down transistors in the circuit for on state and off state mode. It means its response time is less that means its speed is more. When sleep_n =1 the NMOS transistor is on and when sleep_n =0 the PMOS transistor is on state. In off state sleep_n forced to "0" so the PMOS transistor becomes on and NMOS transistor becomes off. So in off condition PMOS is in series with the NMOS hence both in pull-up and pull-down circuit reduces power [7].

## 4. PROPOSED TECHNIQUES

### a) Variable Body Biasing technique (VBB)

In this technique we use two parallel connected Sleep transistors near $V_{dd}$ and two parallel transistors near ground. The source of First PMOS sleep transistor is directly connected to the body of second PMOS sleep transistor this effect is called body biasing effect. Similarly the source of first NMOS sleep transistor is directly connected to the body of second NMOS sleep transistor for generate the same effect as for PMOS sleep transistors. So in this technique leakage reduction occur in two ways first one is the sleep transistor effect and second one is the Variable body biasing effect.

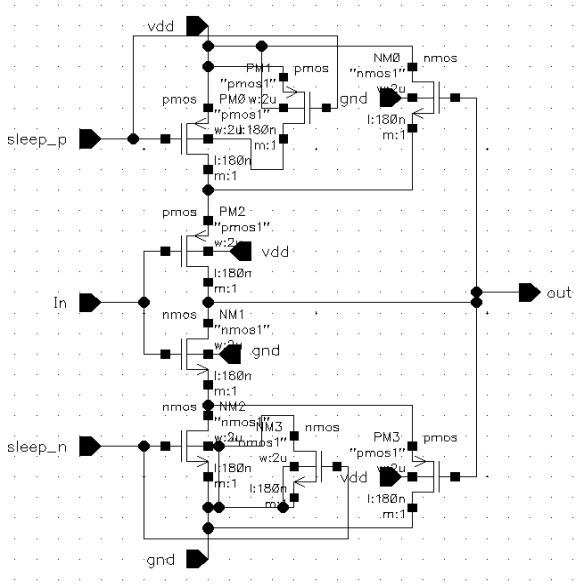


**Figure-7.** Structure of Variable body biasing technique.

As we know that PMOS is not efficient to passing ground same as NMOS is not efficient to passing $V_{dd}$. But in this Variable body biasing technique we use NMOS transistor in $V_{dd}$ and PMOS transistor in ground. Both are in parallel to the sleep transistor for maintaining exact logic state in sleep mode.

### b) Single stack technique, dual stack technique ( One Pmos, One Nmos), Pmos Footer Triple Stack Technique (Ts) and Pmos Footer Four Stack Technique (PFFST)

In single stack technique we use only one PMOS transistor in Footer side place of Dual stack. This technique is not much effective to reduce leakage power which reduces leakage little less compare to Dual stack technique but it reduces the area effectively. One modified approach we use in Dual stack technique is that we replace the one PMOS transistor to one NMOS transistor and the remaining operation is same. In this technique operating speed is somewhat more and area consumption is less than normal Dual stack technique because W/L ratio of NMOS transistor is half of the PMOS transistor.

In PMOS footer triple stack technique (PFTST) as the name suggest we use three PMOS transistor in footer place of two transistors. This technique reduces the leakage power more than Dual Stack technique but the drawback of this technique is it requires more area than Dual stack. But this technique reduces the total power dissipation in huge amount. As when we further modified this technique, when we add one more transistor in footer leakage power dissipation further reduces.

## 5. DESIGN CONSIDERATION

Previous techniques are Sleep transistor, Forced Stack, Sleepy Stack, Sleepy Keeper, Dual Sleep and proposed techniques are Variable body biasing technique, single Stack, Modified Dual stack and Triple stack techniques applying on three different Sense Amplifiers are Current Sense Amplifier, Charge transfer Sense Amplifier and High Speed Sense Amplifier.

Sense amplifier we use in memory components for detecting the very small differential voltage then we can get output logic 1 when the sense amplifier difference voltage becomes high and logic 0 when the sense amplifier difference voltage becomes low.

### a) Current sense amplifier

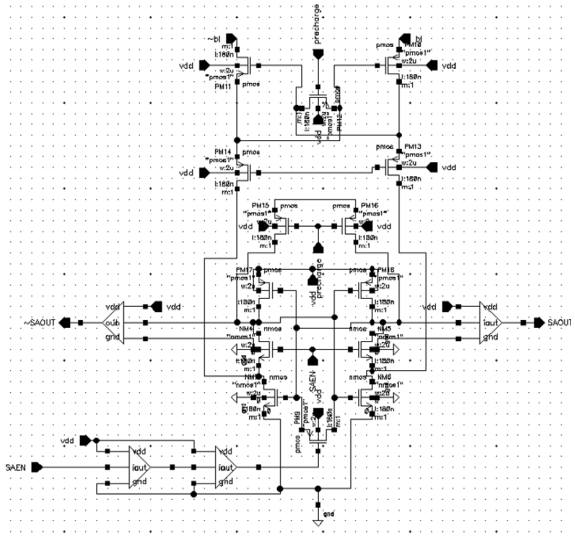


**Figure-8.** Structure of current sense amplifier with MTCMOS.

In operation of Current Sense Amplifier initially Bit-line and Bit-bar line and sense amplifier output is precharged to $V_{dd}$ and by setting up precharge to $V_{ss}$ and $Y_{select}$ to $V_{dd}$. SAOUT and ~SAOUT are the output nodes which are initially precharged high before generates the full swing differential voltage [8] .

**b) Charge transfer sense amplifier**

n the operation of Charge Transfer Sense Amplifier, in precharge phase bit-line, bit-bar line and $Y_{select}$ are pulled high to $V_{dd}$ while the precharge pull down up to $V_{ss}$ and in evaluation phase precharge is pulled up and $Y_{select}$ is pulled down. Structure of Charge Transfer Sense Amplifier is given below with multi threshold CMOS design.

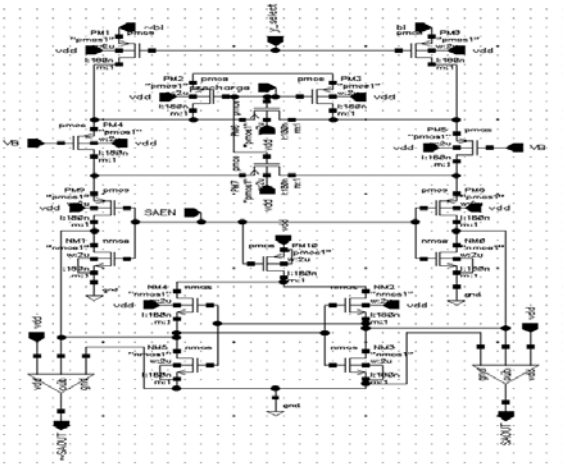

**Figure-9.** Structure of charge transfer sense amplifier.

**c) HIGH SPEED SENSE AMPLIFIER**

In operation of High Speed Sense Amplifier, in precharge phase SAEN is pull down to $V_{ss}$ because of this OUT and ~OUT set to $V_{dd}$. In sensing mode, SAEN pull up to $V_{dd}$.

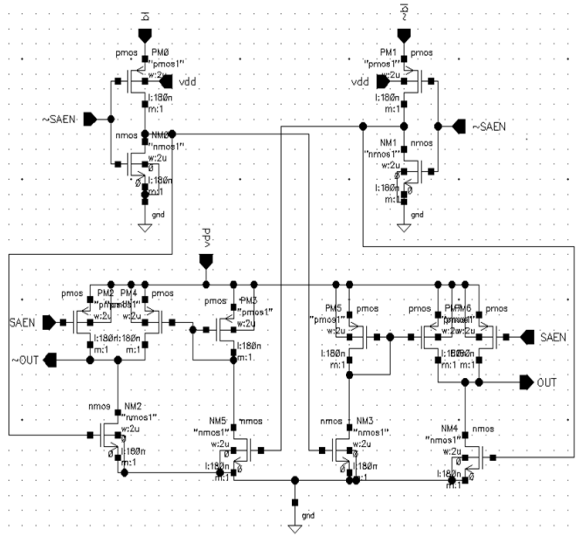

**Figure-10.** Structure of high speed sense amplifier.

## 6. RESULTS AND DISCUSSIONS

Current Sense Amplifier in Active mode provides output in higher Speed Compare to In Saturation mode condition And Modified output providing the glitches so its power dissipation is also less than previous output.

**Table-1.** Different sense amplifiers and its power calculation.

| **Sense amplifiers** | **Power dissipation** (In µW) |
|---|---|
| Current Sense Amplifier | 378.7 |
| Charge Transfer Sense Amplifier | 2396 |
| High Speed Sense Amplifier | 912 |

Current Sense Amplifier Power dissipation is 84.2 and 58.48 percent less than Charge Transfer Sense Amplifier and High Speed Sense Amplifier respectively.

**Table-2.** Leakage power and total power calculation for current sense amplifier.

| **Techniques** | **Leakage power** (In pW) | **Total power dissipation** (In µW ) |
|---|---|---|
| Sleep Transistor | 24.09 | 284.0 |
| Forced stack | 63.54 | 84.49 |
| Sleepy stack | 85.28 | 278.5 |
| Sleepy keeper | 85.28 | 81.59 |
| Dual sleep | 63.07 | 272.3 |
| Variable body biasing | 63.07 | 8.046 |
| Triple stack | 24.16 | 0.06659 |

Proposed Variable Body Biasing Technique 0.73 percent less leakage power dissipative than Forced Stack technique, 26.04 percent less leakage power dissipative than Sleepy Stack and Sleepy Keeper Approach but it leakage power is 61.08 percent more than Sleep Transistor Technique. Other proposed Triple Stack Technique is 61.97 percent less leakage power dissipative than Forced Stack Technique, 72.52 percent less power dissipative than Sleepy Stack and Sleepy Keeper Approach and 61.69 percent less leakage power dissipative than Dual Sleep and Variable Body Biasing Technique.

Proposed Variable Body Biasing Technique is 97.16 percent and 90.47 percent less power dissipative than Sleep Transistor and Forced Stack technique respectively, 97.11 percent and 90.138 percent less power dissipative than Sleepy Stack Technique and Sleepy Keeper Technique respectively, 97 percent less power dissipative than Dual Sleep Technique. Other proposed Triple Stack Technique is much less power dissipative than other techniques.

**Table-3.** Leakage power and total power calculation for charge transfer sense amplifier.

| **Techniques** | **Leakage power** (In pW) | **Total power dissipation** (In μW ) |
|---|---|---|
| Sleep Transistor | 1448E-6 | 2390 |
| Forced stack | 753.5E-6 | 133.4 |
| Sleepy stack | 218.3 | 26.08 |
| Sleepy keeper | 25.89 | 44.51 |
| Dual sleep | 25.89 | 1160 |
| Variable body biasing | 27.06 | 44.52 |
| Triple stack | 39.06E-6 | 79.81 |

Proposed Variable Body Biasing Technique 87.60 percent less leakage power dissipative than Sleepy Stack and 4.32 percent more power dissipative than Sleepy Keeper and Dual Sleep Approach. Other proposed Triple Stack Technique is 94percent less leakage power dissipative than Forced Stack Technique and much less power dissipative than Sleepy Stack and Sleepy Keeper, Dual Sleep Approach and Variable Body Biasing Technique.

Proposed Variable Body Biasing Technique is 98.13 percent and 66.62 percent less power dissipative than Sleep Transistor and Forced Stack technique respectively, 41.41 percent more power dissipative than Sleepy Stack Technique and 90.138 percent less power dissipative than Sleepy Keeper Technique. 96.16 percent less power dissipative than Dual Sleep Technique. Other proposed Triple Stack Technique is same as Variable body biasing technique much less power dissipative than other techniques.

**Table-4.** Leakage power and total power calculation for high speed sense amplifier.

| **Techniques** | **Leakage power** (In pW) | **Total power dissipation** (In μW ) |
|---|---|---|
| Sleep transistor | 147.02 | 912.0 |
| Forced stack | 7.876 | 596.1 |
| Sleepy stack | 16.01 | 697.2 |
| Sleepy keeper | 112.1 | 596.1 |
| Dual sleep | 21.51 | 596.1 |
| Variable body biasing | 179.1 | 0.324 |
| Triple stack | 8.753 | 596.1 |

Proposed Triple Stack Technique 94.04 percent less leakage power dissipative than Sleep Transistor and 10.01 percent more leakage power dissipative than Forced Stack technique respectively,45.32 percent and 92.1 less leakage power dissipative than Sleepy Stack and Sleepy Keeper Approach. Other proposed Variable body biasing Technique is more leakage power dissipative than other techniques. Proposed Variable Body Biasing Technique is much more power efficient than other techniques. Other proposed Triple Stack Technique is 2 to 3 times less power dissipative than other techniques except Variable body biasing technique.

## 7. CONCLUSIONS

Modified Current Sense Amplifier Power dissipation is 2.5 times and 6.32 times less than High Speed Sense Amplifier and Charge Transfer Sense Amplifier respectively. Proposed Variable body biasing leakage power reduction in Current Sense Amplifier 1.5 times less than compare to Sleep Stack, Sleepy Keeper and 0.73 percent less than Forced Stack technique and this technique is much power efficient than other existing techniques. Other Triple Stack Technique leakage reduction is 2 to 3 times less than other existing techniques and it is much more power efficient compare to other techniques.

Proposed Variable body biasing technique and triple stack technique reduce leakage in Charge Transfer Sense Amplifier also is efficient to reduce leakage power and power dissipation. But in High Speed Sense Amplifier variable body biasing technique is not efficient to reduce leakage but it is much more efficient to reduce total power dissipation. Second proposed Triple Stack Technique is 2 to 15 times efficient to reduce leakage power and but this technique is not much efficient to reduce total power dissipation.

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