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EFFECT OF LEAKAGE POWER REDUCTION TECHNIQUES ON COMBINATIONAL

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ABSTRACT

This paper deals with power dissipation in digital circuits. Effect of leakage power reduction techniques are deal with digital circuit design. Analyses of these techniques are done in MICROWIND environment. Power dissipation of these techniques is calculated and compared with conventional design. The layouts are designedusing Microwind. The simulation outputs are taken and observed. Power dissipation of the circuits are tabulated and compared.

Keywords: leakage, power dissipation, short circuit current, threshold voltage.

1. INTRODUCTION

Power dissipation in digital circuits is classified into two types. They are static power dissipation and dynamic power dissipation. Static power dissipation is due to two main factors steady state current, leakage current that is sub threshold leakage current. This sub threshold leakage current is caused by sub threshold conduction. Dynamic power dissipation is due to switching activity of circuit, short circuit current

2. POWER REDUCTION TECHNIQUES

1. Sleepy transistor
2. Sleep forced nmos stack
3. Drain gating
4. Power gating
5. Zigzag approach
6. Leakage feedback

a) Sleep transistor

In this technique two sleep transistor are inserted. One is placed between vdd and pull up network and another transistor is inserted between pull down and ground [1]. In this the exact output is taken and the power is reduced when compared to basic design. The sleep transistors are turned off if the logic circuit is not used. It isolate the logic networks using sleep transistors, the sleep transistor technique intensely reduces leakage power during sleep mode [9, 11]. Sleep transistor method provides good reduction in leakage power

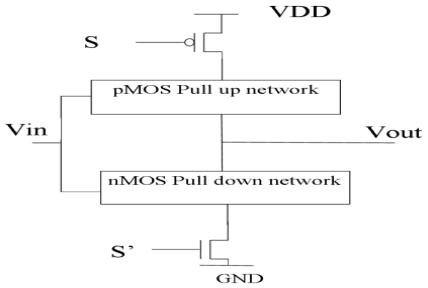


Figure-1. Sleep transistor technique.

b) Lector technique

LECTOR technique uses two extra transistors (a p-type and an n-type) called leakage control transistors (LCTs) inserted in series between pull-up network and pull- down network in each CMOS gate. In this arrangement, one of the LCTs is always "near its cutoff voltage" for any input combination. The resistance of the path from Vdd to ground is increased; thereby decrease in leakage currents [3]. The noteworthy feature of LECTOR is that it works effectively in both active and idle states of the circuit, so there is improved leakage reduction. We get the exact zero and exact one. So it is effective than sleep transistor approach [5].

c) Drain gating

It reduces the leakage current by inserting extra sleep transistors between pull-up and pull-down networks. A PMOS sleep transistor (**S**) is engaged between pull-up network and network output and an NMOS sleep transistor(**S'**) is placed between network output and pull-down network. During active mode, both sleep transistors are turned on so resistance of conducting paths is reduce, thus reducing performance degradation. During standby mode, both sleep transistors are turned off mode, and produce stacking effect which reduces leakage current by increasing resistance of the path from power supply to ground [8]. Two turned-on sleep transistors are placed in active mode; drain gating produces exact logic levels due to less resistance of the path from Vdd to ground [3].

d) Power gating

There are three combinations of Power Gating, Drain Header and Power Footer Gating technique (DHPF) and Drain Footer and Power Header Gating technique (DFPH) [2, 7].

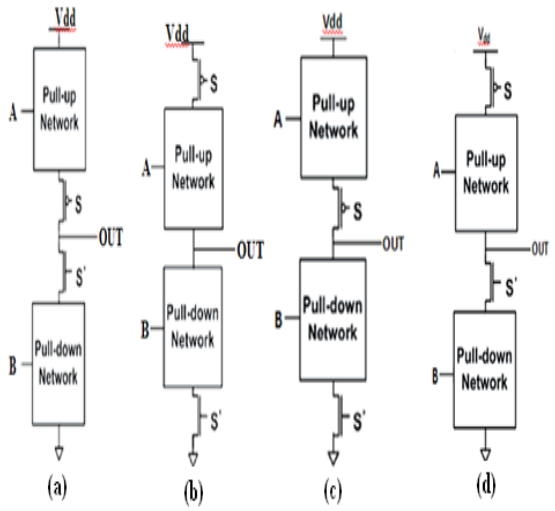


Figure-2. Power gating types.

e) Forced NMOS stack

In this technique has been shown which sleep transistor approach with NMOS, PMOS is and NMOS sleep transistors are used for leakage power reduction and an extra NMOS is added. Because sleep transistor technique is a state destructive technique, to hold the state NMOS is used here in this proposed technique [6]. High Vth is given to the Sleep a transistor that is multi-threshold technique is used here.

f) Leakage feedback

The leakage feedback approach is based on the sleep transistor approach.Here two additional transistors are used to maintain logic state all through sleep mode, and the two transistors are pushed by the output of an inverter which is driven by output of the circuit implemented utilizing leakage feedback concept, a PMOS transistor is positioned in parallel to the sleep transistor (S) and a NMOS transistor is placed in parallel to the sleep transistor (S') [8, 10].

g) Zigzag approach

In this technique the sleep transistor is used alternatively for two circuits. Pull-down sleep transistor are applied for the first stage and pull-up sleep transistor for the second stage.[4] To reduce the wake-up cost of the sleep transistor a technique is used which is named as the zigzag technique.

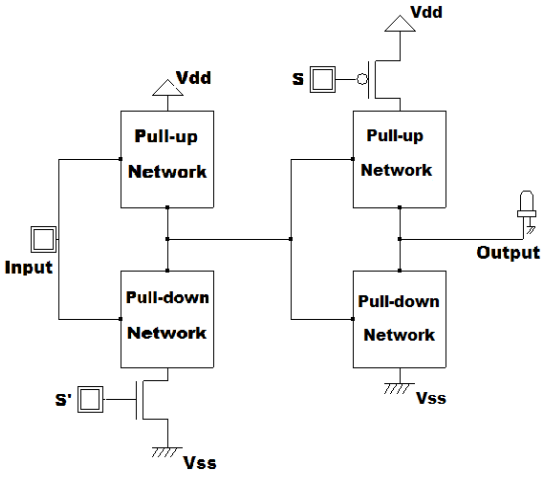


Figure-3. Zigzag approach.

3. LAYOUT DESIGN AND SIMULATION OUTPUT

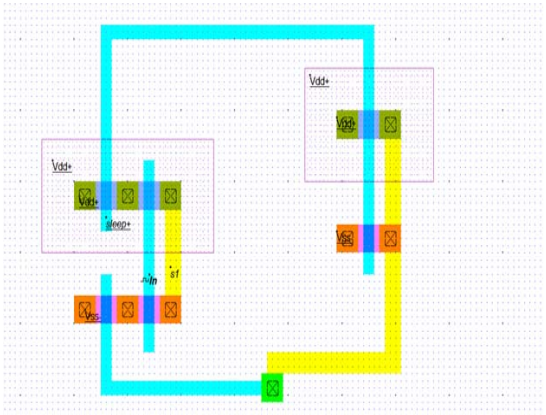


Figure-4. Layout design of inverter using sleep transistor technique.

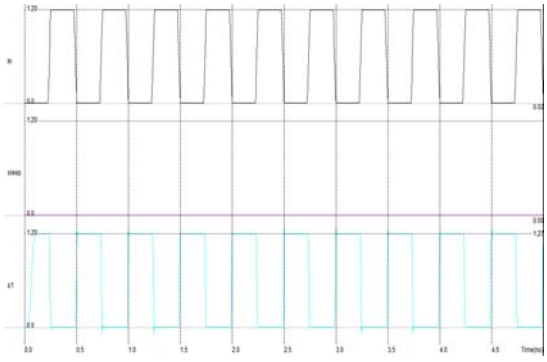


Figure-5. Transient analysis of inverter using sleep transistor technique.

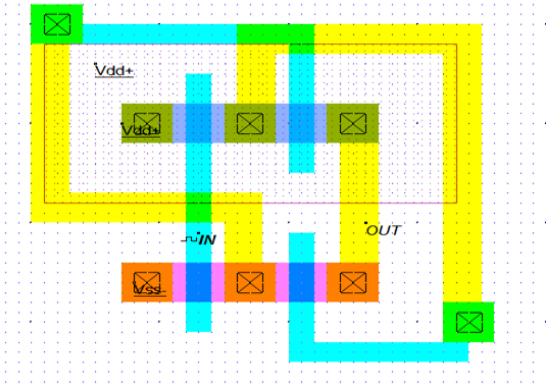


Figure-6. Layout design of inverter using lector technique.

Figure-7. Transient analysis of inverter using lector technique.

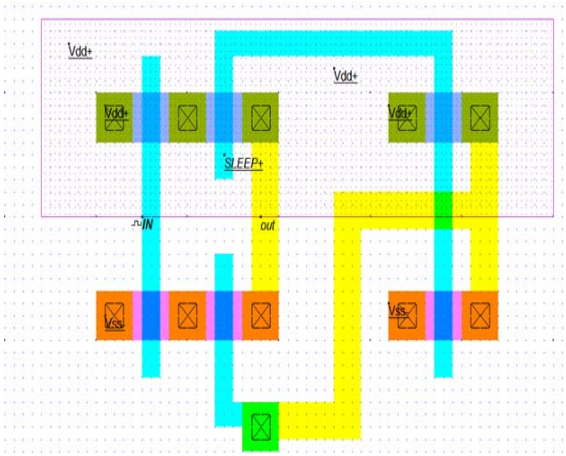


Figure-8. Layout design of inverter using drain gating.

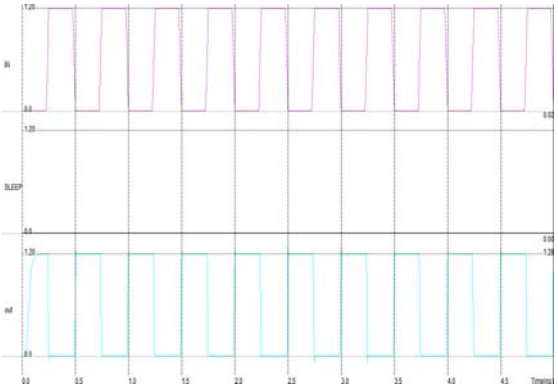


Figure-9. Transient analysis of inverter using drain gating.

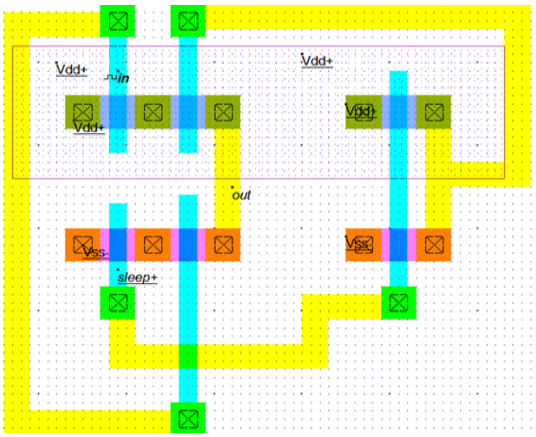


Figure-10. Layout design of inverter using DHPF.

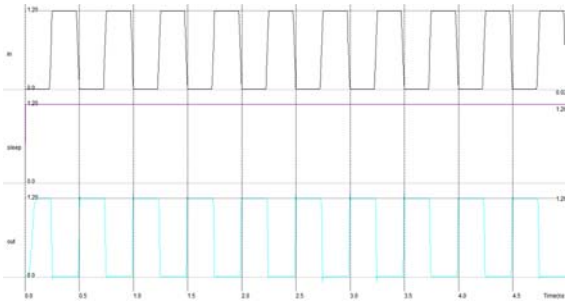


Figure-11. Transient analysis of inverter using DHPF.

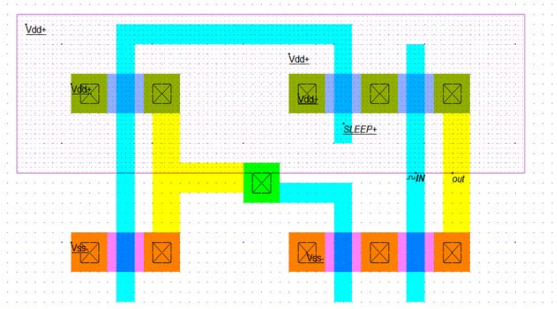


Figure-12. Layout design of inverter using power gating.

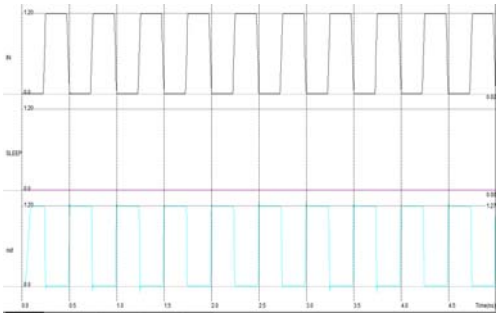


Figure-13. Transient analysis of inverter using power gating technique.

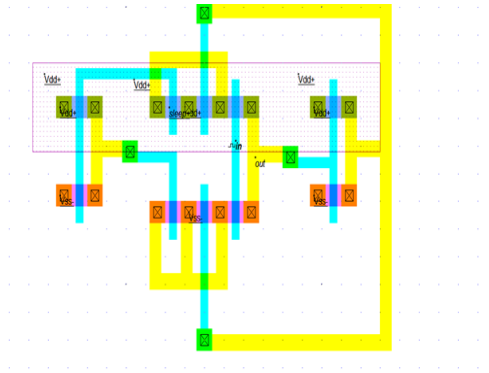


Figure-14. Layout design of inverter using leakage feedback technique.

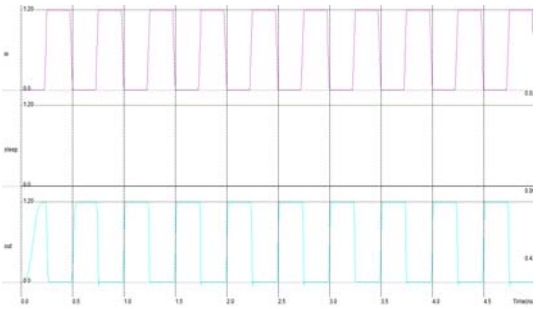


Figure-15. Transient analysis of inverter using leakage feedback technique.

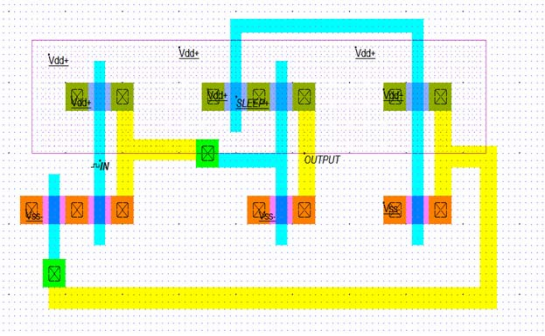


Figure-16. Layout design of inverter using zigzag technique.

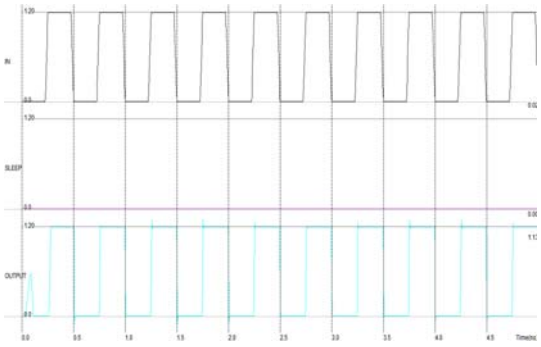
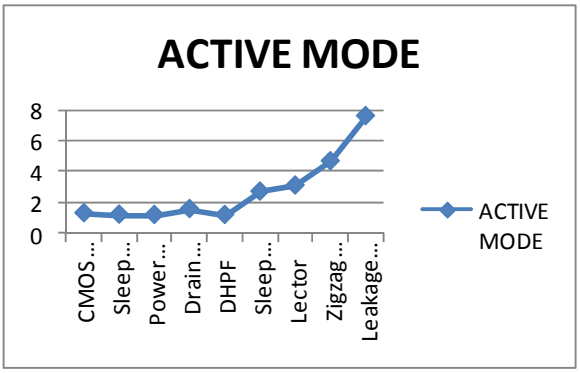


Figure-17. Transient analysis of inverter usingzigzag technique.

Table-1. Comparison and analysis.

S. No.	Technique name	Active mode	Technique mode
1	CMOS logic	1.32 µW	-
2	Sleep transistor	1.23µW	0.12 µW
3	Power gating	1.208 µW	0.16 µW
4	Drain gating	1.588 µW	0.028 µW
5	DHPF	1.205 µW	0.263 µW
6	Sleep forced nmos stack	2.719 µW	-
7	Lector	3.106 µW	-
8	Zigzag approach	4.681 µW	0.317 µW
9	Leakage feedback	7.593 µW	0.513 µW



4. CONCLUSIONS

Power dissipation of various power reduction techniques are discussed here. When relating all techniques we can differentiate the power dissipation of circuits. Some techniques have sleep concept which is good worthy. This paper concentrates on the leakage power. There are some other techniques which deal with threshold voltage of the devices. All these techniques are analyzed. Simulation results of these techniques are obtained. The performance is equated.

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