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DESIGN AND IMPLEMENTATION OF VEDIC MULTIPLIER USING EFFICIENT CHARGE RECOVERY ADIABATIC LOGIC

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ABSTRACT

Now a day it is indeed to design and implement an adiabatic logic in Vedic multiplier. Normally the power consumption was the main thing to remember before designing and implementing. So, the main aim to concentrate on the power consumption is very important. Here the proposed adiabatic logic is efficient charge recovery adiabatic logic based design. Compare with other multiplier the Vedic multiplier consume very less power, here combining with this adiabatic logic the power consumption is dramatically reduced. The tool used here was tanner EDA to designing the Vedic multiplier using efficient charge recovery adiabatic logic.

Keywords: efficient charge recovery adiabatic, low power, and Vedic multiplier.

1. INTRODUCTION

In arithmetic operations the multiplication plays a one of the most important functional function. Multipliers are the one the key components of every ALU. In VLSI design, it concern the power consumption is a major part. The dominant role in designing of digital circuits is high speed multiplier. Digital multipliers are the critical arithmetic functional units in many applications, such as the Fourier transformation, discrete cosine and sine transform, and digital filters. The throughput of these applications depends on the multipliers. The multipliers are too slow; it reduces the overall performance of the circuit. Here concluding that the overall performance of the system depends on the throughput of the multiplier. Digital multipliers are the core material of all the digital signal processor (DSP) and the speed of the DSP is largely depends on the multipliers. They are many types of multipliers like array multiplier, Wallace tree multiplier and booth multiplier. The array and booth multiplier, consist of number of cycles and large exponential area [7]. Here, the Vedic mathematics which proposes the simple approaches, towards the normal mathematical operations. The word "Vedic" is derived from the word "Veda" which means the store house of the knowledge. Vedic mathematics is the ancient methodology of the Indian mathematics. It has the unique technique of calculation based on the 16 sutras (formulae). It covers several modern mathematical terms including arithmetic, geometry, trigonometry, quadratic equations, factorization and even calculus. In this paper, urdhva tiryakbhyam is used to develop digital multiplier architecture. This multiplier architecture is based on the vertical and crosswise algorithm. The idea of humble power demand, the adiabatic logic is used. Adiabatic logic are also called has the energy conserve [2, 7].

This paper organized as follows. II. A brief explanation about Vedic multiplier. III. This section is about efficient charge recovery adiabatic logic. IV. Existing method and its drawbacks. V. Proposed design of Vedic Multiplier using efficient charge adiabatic logic in tanner EDA tool. VI. Comparison result and discussions. VII. Conclusion. VIII. References.

2. VEDIC MULTIPLIER

The use of Vedic multiplication is used to reduce the typical calculations to simple one. It is based on the Vedic formulae, the formulae which consist of the 16 sutras. Here in the proposed method Urdhva Tiryakbhyam is introduced [2].

a) Urdhva Tiryakbhyam

Urdhva tiryakbhyam sutra (formulae) is used in the proposed method. Sutra has been used for multiplication of two numbers in the decimal number system. It is nothing but vertical and crosswise. This formula is generalized for n x n bit numbers. The procedure for urdhva tiryabhyam is given below:
Multiply 101 by 101.

- First take the right-hand digits and multiply this give the LSB digit answer.
- Secondly multiply LSB of the top number with the second bit LSB of the bottom number and add them together.
- Multiply the LSB digit of the bottom number by the MSB digit of the top number, then LSB digit of the top number with the MSB digit of the bottom one and multiply the bit after that add all together.
- Move one place to left, multiply the second digit of one number with the MSB of the other number.
- Finally, multiply the LSB of both the numbers together and get the result. [8, 9].

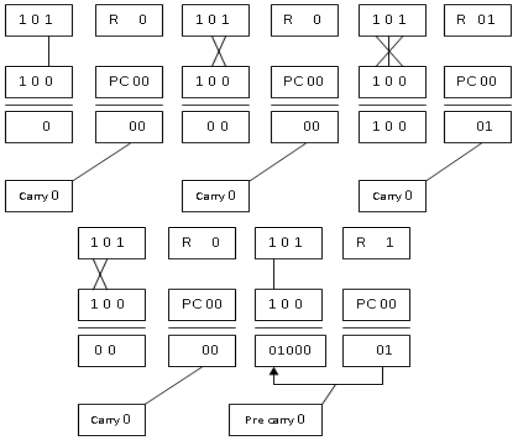


Figure-1. Urdhva Tiryakbhyam operation.

The 2 x 2 Vedic multiplier operations are shown in Figure-1. From Figure-2 which consists of three steps is as follows:

Step-1: Vertical multiplication
First step to multiply a0 x b0 which gives s0.

Step-2: The Cross multiplication
Second step to multiply crosswise.

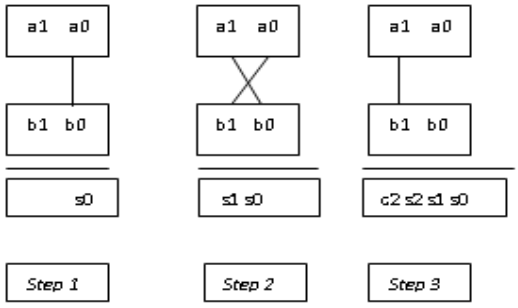


Figure-2. 2x2 Vedic multiplier operation.

Step-1: Vertical multiplication
The third step again vertical multiplication a1 x b1 which gives s2 and c2.

Block diagram of 2 x 2 which is shown in the Figure-3. Here two half adders are used in the 2 x 2 Vedic multiplier. Half adders it consist of one AND gate and OR gate. The Gate level structure shows in the Figure-4.

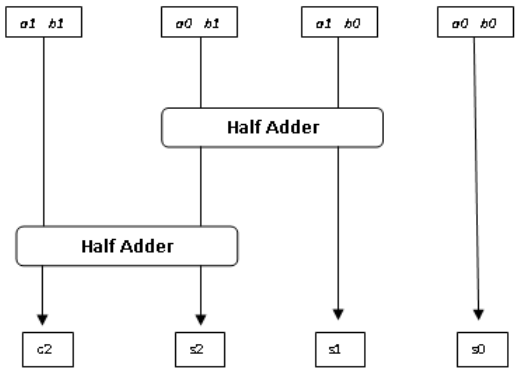


Figure-3. Block diagram of 2x2 Vedic multiplier

Here the inputs are a0, a1, b0, b1 the proceeding outputs are s0, s1, s2 and also the carry c2.

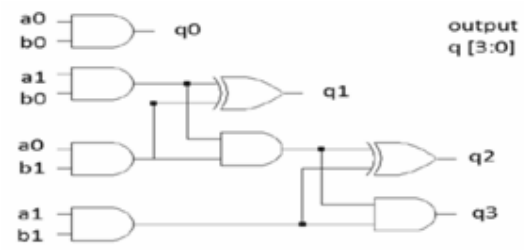


Figure-4. Gate level 2x2 Vedic multiplier.

3. ECR ADIABATIC LOGIC

ECR adiabatic logic its expansion is efficient charge recovery adiabatic logic. It consists of two NMOS and two PMOS. The adiabatic logic is, the pmos2 and the nmos2 will act as the MOSFET diode. It is used to recycle charges from the output node which is to improve the discharging speed of internal signal nodes [1, 2].
According to the law of energy conservation, dissipated energy is equal to the total energy injected into the circuit and the energy received back from the circuit. Hence the energy is recovered by the MOSFET diodes. It is shown in the Figure-5. [3, 10, 6].

The Parameters of the Vedic multiplier with and without using efficient charge recovery adiabatic logic is
For PMOS,

M=1
W=2.50u
L=0.15u
NP=1

For PMOS,

M=1
W=2.50u
L=0.55u
NP=1

These are the parameters used for designing Vedic multiplier using efficient charge recovery adiabatic logic.

It is also suitable for the efficient charge recovery adiabatic logic.

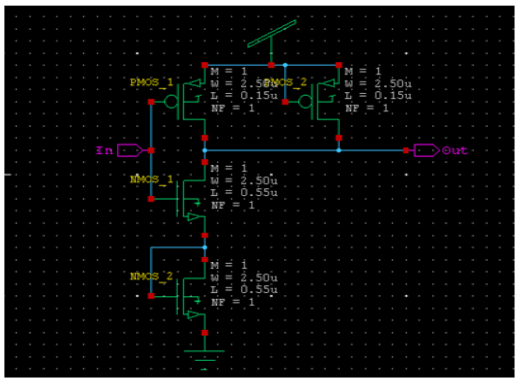


Figure-5. Efficient charge recovery adiabatic logic.

4. EXISTING METHOD AND ITS DRAWBACK

In the existing method, 4×4-bit array 2PASCL multiplier utilizing CMOS technology using a new 2PASCL 2XOR. The low-power dissipation analysis in adiabatic charging and discharging using constant voltage value and ramp-wave voltage is carried. The technology applied to low power digital devices operated at low frequencies, such as radio-frequencies, smart cards, and sensors.

The Figure-6 shows the block diagram of 4x4 array multiplier. Using the array multiplier it consists of large area and large power consumption. To reduce the power consumption and also the area instead of using array multiplier, Vedic multiplier is used. Hence, in the proposed method Vedic multiplier with using efficient charge recovery adiabatic logic is used.

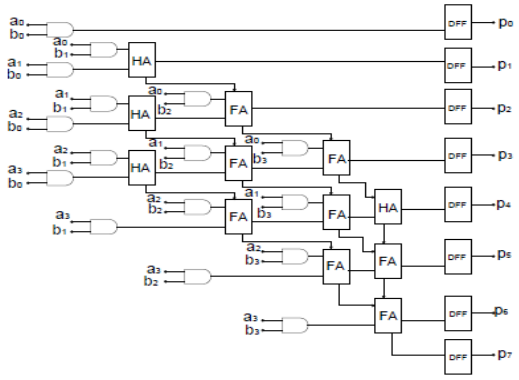


Figure-6. Array Multiplier.

5. PROPOSED METHOD OF VEDIC MULTIPLIER USING ECRAL

By using four 2x2 bit Vedic multiplier the 4x4 multiplications is formed, the inputs are A= A3 A2 A1 A0 and B= B3 B2 B1 B0 and the output for the multiplication result is S7 S6 S5 S4 S3 S2 S1 S0.

In the proposed method it is divided into two cases

- Vedic multiplier without using efficient charge recovery adiabatic logic.
- Vedic multiplier with using efficient charge recovery adiabatic logic.

From the above two cases, the power results are compared using the tanner EDA tool version 13.

- Vedic multiplier without using ecral

The Vedic multiplier without using efficient charge recovery adiabatic logic and the block diagram and the output waveform are given below: The Figure-7 consists of four 2 x 2 bit Vedic Multiplier and the ripple carry adder.

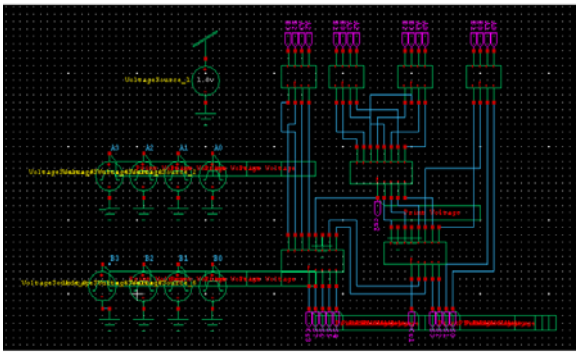
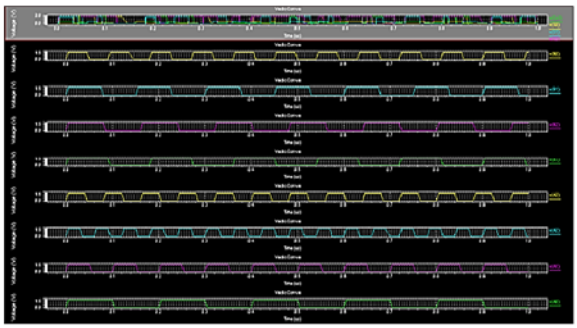


Figure-7. Vedic multiplier without using ECRAL.



Figugre-8. Generated waveform.

Hence the circuit consumes 1.610953e-003 power.

- Vedic multiplier using ecral

The Vedic multiplier without using efficient charge recovery adiabatic logic and the block diagram and the output waveform are given below:

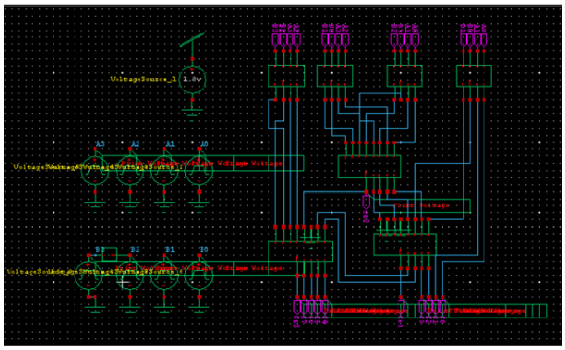


Figure-9. Vedic Multiplier using ECRAL.

Figure-7 shows the efficient charge recovery adiabatic logic is connected in any two of the input nodes. The generated waveform for the above circuit is given in Figure-10.

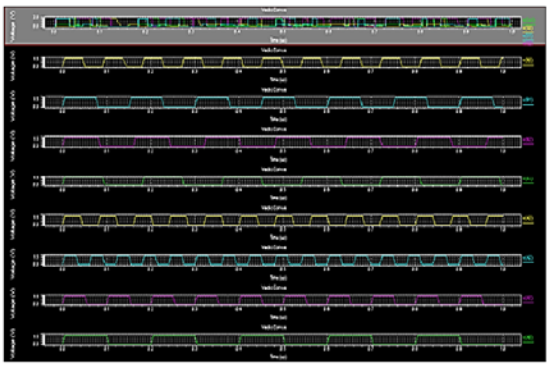


Figure-10. Generated Output.

Here the circuit consumes 1.020050e-011 power. Compare to without using ECRAL it consumes less power. The net list also generated using the tanner EDA tool.

6. POWER RESULT COMPARISON

The power result comparison of vedic multiplier with and without using Efficient Charge Recovery Adiabatic Logic is given below:

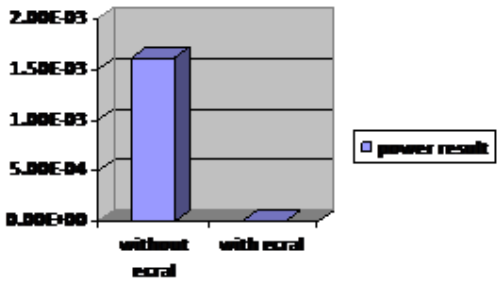


Figure-11. Power comparison chart.

The power comparison chart clearly shows that the power is reduced while using Efficient Charge Recovery Adiabatic Logic.

7. CONCLUSIONS AND FUTURE WORK

Array multiplier is used for computation in processors but it consumes more power. To overcome that, Vedic multiplier associated with efficient charge recovery adiabatic logic is introduced in proposed system. Here it is divided into two cases; implement of Vedic multiplier without and with efficient charge recovery adiabatic logic. Hence, the Power results are compared using the simulation results using the tanner EDA tool version 13. Further, Vedic multiplier using with efficient charge recovery adiabatic logic is designed in ALU circuit for consuming low power and also implemented in hardware also.

REFERENCES

[1] Anu priya and Amritha Rai. 2014. "Adiabatic Technique for Power Efficient logic Circuit Design" IJECT, Vol. 5, Issue Spl-1.

[2] Aruna. M. and Usharani. G. 2014. "Simulation & Implementation of Complex Multiplier using Vedic Mathematics" IJETST, volume 1,| issue 05.

[3] Deebika R. and karunambiga R. 2014. "Design and Analysis of Multipliers Using Energy Recovery Adiabatic Logics" International Journal of Emerging Research in Management &Technology ISSN: 2278-9359, Vol. 3, Issue-3, pp.159 – 160..

[4] Ing-Chao Lin, Yu-Hung Cho, and Yi-Ming Yang. 2014. "Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic" IEEE transactions on very large scale integration (vlsi) systems.

[5] Navya Rajput, Ankit Jindal and Sahil Saroha. 2013. "A Novel and High Performance Implementation of 8x8 Multiplier based on Vedic Mathematics using 90nm Hybrid PTL /CMOS Logic" International Journal of Computer Applications (0975 – 8887) Vol. 69, No.27, pp. 29 - 30.

[6] Mukesh Tiwari, Jai karan Singh and Yashasvi Vaidhya. 2012. "Adiabatic Positive Feedback Charge Recovery Logic for low power CMOS Design" International Journal of Computer Technology and Electronics Engineering (IJCTEE) Vol. 2, Issue 5.

[7] Pushpalata Verma and K. K. Mehta. 2012. "Implementation of an Efficient Multiplier based on Vedic Mathematics Using EDA Tool" International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Vol. 1, Issue-5.

[8] Rakshith Saligram and Rakshith T. R. 2013. "Optimized Reversible Vedic Multipliers for High Speed Low Power Operations" IEEE Conference on Information and Communication Technologies (ICT 2013).

[9] Richa singh. 2013. "Power Efficient Design of Multiplexer Based Compressor using Adiabatic logic" International Journal of Computer Applications, pp. 0975-8887. Vol. 81- No 10.