VOL. 10, NO. 7, APRIL 2015 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences


www.arpnjournals.com

GENETIC ALGORITHM BASED ROUTERS ARRANGEMENT IN NETWORK ON CHIP USING THE UNION MULTIPROCESSOR

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ABSTRACT

System On Chip is a complete integrated system because it consists of several different microprocessor subsystems together with memories and I/O interfaces. So the connection between these IP's components are the major issue and the Network On Chip (NOC) plays an important role in connecting these IP's. The adaptive XY routing never runs into deadlock or live lock therefore it consumes more power and it also passes the data through fault path. In the proposed, a new Network On Chip use Genetic Algorithm which is an optimization algorithm used to find the shortest path and critical path analysis by routing the router on four sides so this algorithm is free from live lock and deadlock problem thereby it consumes less power. It also finds fault part of NOC components by using fault analysis process to identify the damaged router in NOC chip architecture. The experimental results shows reduction in power with 20% and delay can be reduced with 40% on average compared to adaptive router architecture for network on chip.

Keywords: intellectual properties, network on chip, dynamic NOC, adaptive routing, genetic algorithm.

1. INTRODUCTION

In general, a system on a chip is an Integrated Circuit that integrates all new components into a single chip. Due to increase in number of transistors on a single chip will provide complex system. To reduce the system complexity, integrated system on chip in a system, it forms a Network On chip. Network On Chip is a communication subsystem which is typically between IP cores in a System On a Chip. NOC improves the scalability and the power efficiency of complex SOC compared to other design.

Unified Inter/Intra chip Optical Network (UNION) for Chip Multiprocessors. It will separate interchip communication traffic from intra chip because it employs in the hierarchical optical network it also connect multiple chip multiprocessor in a system.

The network controller [15] on each chip multiprocessor (CMPs) manages both intra chip and interchip communications then it also yield better solution. [1] If the required components are available, then uses the rules of the *XY* algorithm to route data packets into the network in the *XY*-based adaptive routing algorithm so in some cases, components are not present that time a specific routing path is temporally taken to bypass its position. By using the routing error detection algorithm, it will check the data form by previous node routing decision.

A dynamic network on-chip [12], the DYNOC place the components dynamically for communicates it also able to pass data in obstacle path. In this architecture long or more interconnection is avoided because the processing element placed very close to each other. The fixed NOCs are not supporting a dynamically changing network on chip. In the unavailable region and faulty node are not able to pass the information in the system. In CUNOC [7], the XY algorithm is suitable for fixed NOCs network. If the number of faults increases the rate error detection becomes increases. The detection of error presence on the same row and on the same side will prevent the detection second.

Network on chip (NOC) to be maintained by allowing the throughput and network load if it locates accurate error. For detecting the router error with the help routing algorithm which is also connected with a mesh structure. The performance NOC router is low by fault analysis operation.

2. DATA TRANSMISSION BASED ON ROUTER ARRANGEMENT IN NOC

The VLSI technology mainly focused by the SOC and NOC chip processors. By optimizing the processing time and area in SOC technology, then performance should be good. In NOC technology, data transmission process can be performed in wire or wireless technology. The block diagram for data transmissions is shown in Figure-1.

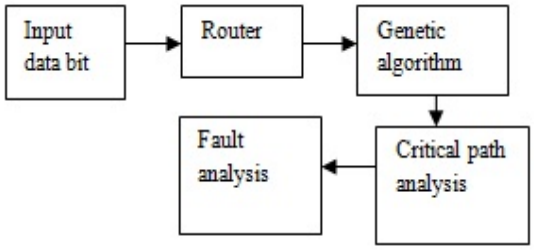

Figure-1. Block diagram of data transmission process.

To improve the transmission data accuracy level by using NOC technology, then it also reduces the transmission time. So the SOC chip consists the more no of router architecture in mesh topology connection.

The router architecture used to increase the data signal strength. And the mesh topology connection applies to the SOC router arrangements. The router process has some problem due to the data transmission time [1]. So need to find the shortest path analysis in internal router data transmission process. So we use the GENETIC algorithm in SOC architecture.

This algorithm [9] used to find the minimum node selection process and to find the critical path analysis also. This GENETIC algorithm used to find the shortest path data transmission due to the SOC router architecture. This algorithm used to improve the transmission time and reduce the power consumption level due to the transmission time. The router used to transmit the data bits into one source to another destination level and to send the data bit level do not change. The routers arrangement to mainly important section on NOC chip architecture and the routers are connected to the mesh topology connection.

The genetic algorithm mainly used to the minimum node selection process and to develop the data transmission process and to improve the data bit strength level. The algorithm used to modify the router allocation and find the data path effectively and to optimize the routers arrangements. The network routing technique used to optimize the genetic process and to calculate the fitness process for router node representation. The genetic algorithm to enhance the fitness process for the router mesh topology interconnection placement levels.

The critical path analysis section process is the main parameter for the NOC chip architecture for the wireless communication process. The path information is mainly used to find the shortest path. This method used to very fast data transmission source to the destination and to reduce the path delay and increase the speed of NOC process. The critical path section to find the path allegation level in shortest path compared to the critical path.

The fault analysis process to identify the damaged routers in the NOC chip architecture and to reject the path for required damaged router. The damaged router to block the input bit data for the transmission process and to modify the routers arrangement in the NOC. The router faults identification process mainly used to missing the input data bits from source to destination section.

3. OPERATION

The operation of genetic algorithm can be performed with the help of genetic operators. Here they consider three basic operators are crossover, mutation, fitness function. Fitness proportionate selection, Boltzmann selection, Rank selection is the method for selection of chromosomes. Mutation is a genetic operator which is a process taken from one generation of a population of genetic algorithm chromosomes to the next generation of population due to maintain the genetic diversity. It changes one or more gene values in a chromosome from its initial state.

To find shortest path analysis by using a fitness function with the help of crossover, encoder, mutation. The fitness function must not only correlate closely with the particular value, it must be computed quickly. When clock and enable becomes high and reset as 0 it produce a resulted data as output.

The advantage of Genetic Algorithm is applied for solving the problem of faulty module prediction. GA is also finds the most important attribute for fault occurrence. The system finding the most important attribute for fault prediction and calculate the critical path and find the shortest path. The designer can specify a maximum length of the physical link that permits the single clock cycle data transfer.

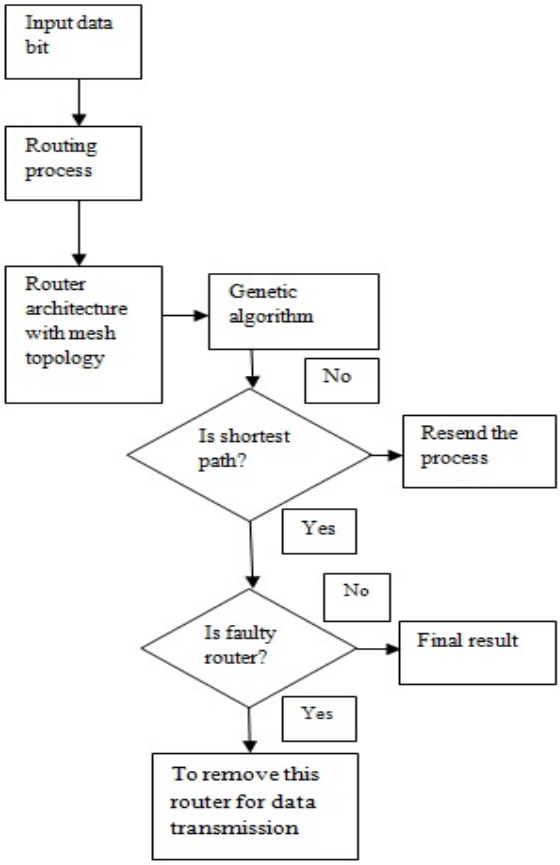

Figure-2. Flow diagram process to transmit the data.

From Figure-2, the diagram of the data transmission process it first assigns the input bit data for process the arrangement of router those routers are connected with mesh topology, then applies a genetic algorithm to find shortest path analysis if it is shortest path it will check whether it is faulty router or not otherwise it will again resend to genetic process.

If there is no fault path occurs, it will produce results, but if any faulty router is present means remove the router for data transmission. When a router is connected with mesh topology because if any node fails means it does not affect the information it passes through the other connection or it having many other ways to communicate.

In this technique, the input for communication trace graph are system level floor plan and interconnection architecture elements. In the floor plan router is located in physical connection, thereby it reduces the space of this algorithm and its runtime by selecting the router location.

The shortest distance from any node to the router and all inter-router distance also determine from the known possible physical location of the router. By using the clock period of core which is initiating the write operation for that physical length of inter-router and node-router connection can be constrained**.**

Normally, the NOC comprises of router, network interfaces and links allowing communication between the Processing Element. The path to be traversed for a data packet between a source and a destination through the router is defined by the routing algorithm. In the adaptive XY algorithm, if the chosen port is busy, the header flit and all subsequent flits of this packet will be blocked. In this packet, the routing request will remain active until a connection is established in some future execution of the procedure in this router it cannot avoid from deadlock appearance. But in case of genetic algorithm, it provides the better fault coverage than deterministic algorithm and it can also be applied to generate test patterns for complex combinational circuits.

4. RESULTS AND DISCUSSIONS

From the results, router arrangement is done by regular route with the help of selection and read/write component. By routing the router in four directions it chooses the best path through the selected line 1 and selected line 2 is used to transmit the data through selected path.

The results are taken from the Xilinx 14.2 version it also compare with Xilinx ISE. So the Placement and Routing (P&R) runtime, Memory usage, Wire length and congestion is high for ISE and for VIVADO the Placement and Routing (P&R) runtime, Memory usage, Wire length and congestion are reduced.

At the component level, unit tests should be considered as basic test. Black box and white box testing are the software testing terms to test the product. The test entry screen, messages and responses must not be delayed any more with the help of this test product. From Figure-3, the router arrangement finds the parent node data.

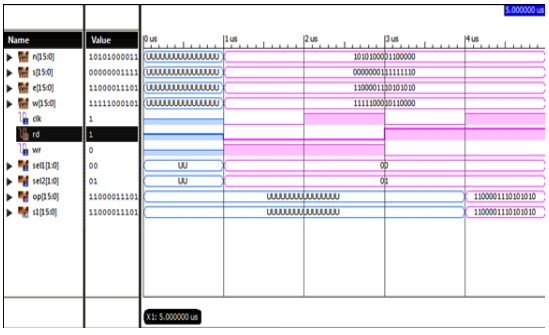

Figure-3. The output waveform of router arrangement.

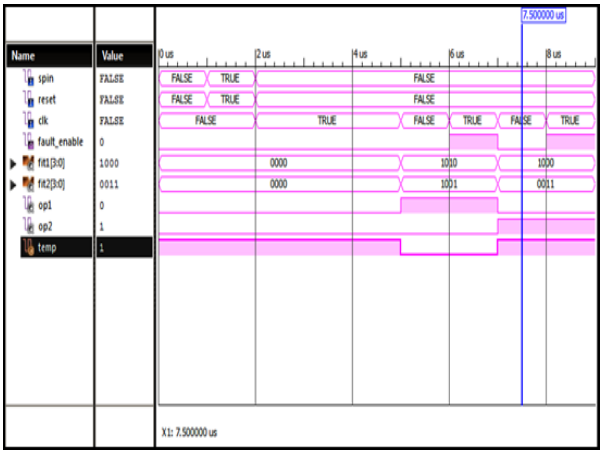

Figure-4. The output waveform for finding the shortest path.

From Figure-3 and 4, it chooses the random number generator term The above program passes the value ‘8’ to main code in a generic manner so that the output generated by the code is 8 bits in size.

The functional and unit test is used to test the product here the functional test are considered the terms are valid and invalid and it also considers the function and output terms to be checked.

Here the identified valid input is accepted and identified invalid input are rejected and then the function as well as output can be identified with the help of this functional test.

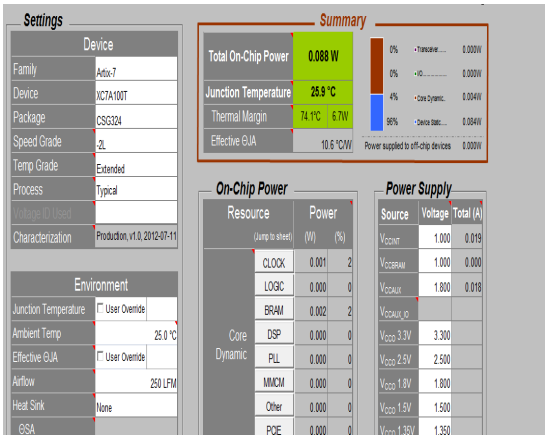

Figure-5. Power analyzer from Xilinx power estimator.

Then the roulette wheel selection process takes place so the input of the roulette wheel are clock, reset, spin and the output are digit0, digit1. Fitness proportionate selection is otherwise known as roulette wheel selection. The solution with a higher fitness will be less likely to be eliminated.

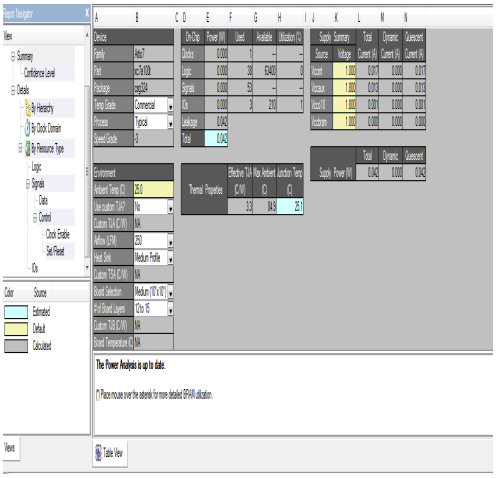

Figure-6. Power results from xilinx power analyzer tools.

To find the shortest path analysis with the help of crossover, mutation, fitness function. So the input of the crossover is parent1, parent2, clk, reset and the output is child1, child2. So here the child node data are getting from the parent node. It has 16 bit data which is the process of making more than one parent node to produce a child node data.

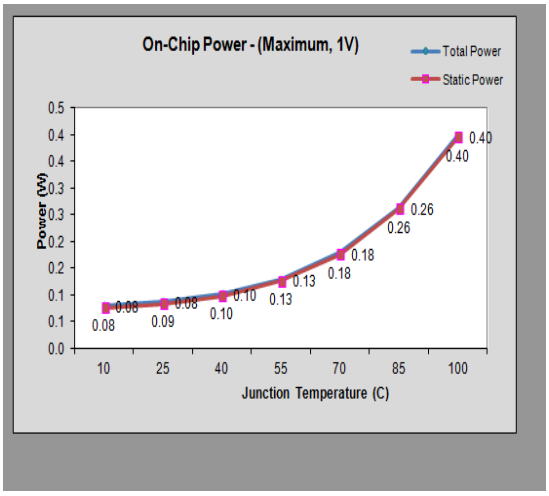

Figure-7. Graph diagram for power Vs Junction temperature.

The mutation is used to find, modify bit position with the help of crossover and encoder. To avoid local minima by preventing of chromosome for that mutation should allow this algorithm. The input of fitness are clock, reset, spin and the output of fitness are fit1, fit2. Here spin look like a clock, which is a bit by bit analysis. It produces 4 bit data value when clock and enable becomes high otherwise it does not produce the output.

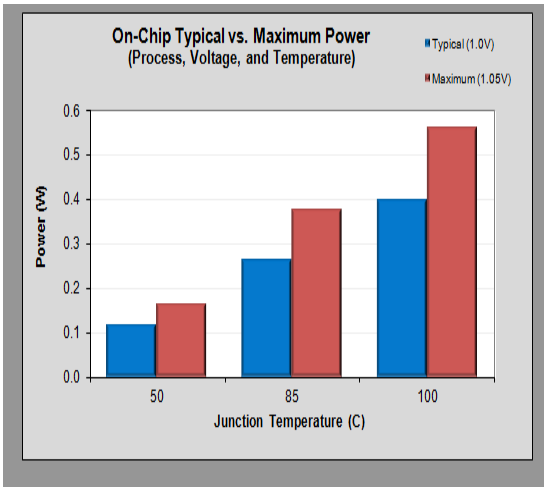

Figure-8. Graph diagram for on-chip typical Vs maximum power.

From the above Figure-8, it shows the power comparison results. These comparisons and simulation for regular route and fitness function to find shortest path analysis output waveform can be simulated with the help of Xilinx.

5. CONCLUSIONS

The new error detection mechanism for dynamic NOCs is Genetic algorithm, which is used to find parent node data for router arrangement and it also analyzes the shortest path in the NOC to transmit the data efficiently with the help of genetic operators (crossover, mutation, fitness function). The power value obtained from results is 0.04mW. So that power consumption gets reduced 20% compared to adaptive router architecture and the results shows the graph for On-chip typical Vs maximum power. It can also allow the accurate localization of permanent faulty routing blocks in the network. In future, the fault analysis process has taken place to identify the damaged routers in the NOC chip architecture to reject the path for required damaged router and then the data can be transmitted through faultless path.

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