VOL. 10, NO. 7, APRIL 2015 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences


www.arpnjournals.com

AN EFFICIENT PARALLEL ARCHITECTURE IN DESIGN AND IMPLEMENTATION OF ADAPTIVE LMS ALGORITHM

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ABSTRACT

The proposed work is to implement the parallel architecture for adaptive LMS filter configuration, a concurrently processed filter is realized which adapts the time controlled block. The filter co-efficient are negotiated, which are uploaded in to the look up table. These data are further configured and retrieved from the stored buffers. Single block is realized here depends upon the timing control these blocks are called a function. This architecture reduces the area utilization and Power consumption. The proposed system is precise and easy to configure and update.

Keywords: adaptive filter, least means square algorithm, parallel architecture Look up table.

1. INTRODUCTION

Adaptive filters extend to wide range of signal processing, image processing and wireless communication. Some of signal processing applications are Plant identification & Channel estimation, Inverse system modeling, Signal prediction in DPCM speech Quantizer, Interference cancellation in the Biomedical sensing system and Active noise control system. The implementation of higher order adaptive filters requires fast convergence property and Adaptability to make time varying impulse response [11-14].

LMS adaptive filter most popular & widely used not only because of its simplicity but gives satisfactory convergence performance [11].

The direct-form LMS adaptive filter has long critical path due to its inner product computation to obtain filter output. Inner product decreases by pipelining. Conventional LMS does not support pipelined implementation, so DLMS is used The DLMS (Delayed LMS) is an advanced architecture where pipeline is implemented with small modifications to suit VLSI technology. [1-2].

The LMS algorithm used with pipelined and parallel FIR (finite impulse response) filter architectures produces delays in the co-efficient or increases the hardware requirement, decreased by adaptation delays, high performance rate without the dependency on FIR filter length. Hybrid architecture is proposed by combining a transpose – form architecture. Compute the correction term and calculates the delays LMS error [3].

The existing system used to modify version of the DLMS algorithm without degrading the convergence characteristics. It results in higher throughput maintenance by using a new look ahead transformation. It results in improving the convergence characteristics though the algorithm suffers large hardware complexity with more delays [4].

Lan *et al.*,[5] proposed an efficient systolic and suitable for a single chip realization, which furnish the lowest critical period in the word – level and better convergence without sacrificing finite – driving, area, cost, regularity & local connection characteristics.

Higher speed FPGA combined with DLMS is implementation to maintain low latency output. In addition DLMS, and "fine grained" pipelining is implemented with direct form and transpose form it results direct form has high speed, low latency design compared to transpose form [6].

Yi *et al.* [7] Proposed fine grained pipelined design of an adaptive filter that supports high sampling frequency but with pipeline depth. The adverse effects of the architecture is that power dissipation increases, adaptation delay increases and convergence performance degrades. Meher *et al.* [8] has been made further effort to reduce the number of adaptation delay.

Sang *et al.* [9] proposed a novel pipelined architecture for low power, high throughput and low area adaptive filter based on distributed arithmetic (DA) which gives enhanced throughput by parallel LUT table & concurrent process of filter operation and weight updating. To decreases area complexity, carry – save accumulation is used. The reduction in power consumption is achieved by using fast - bit clock [9].

Meher *et al.* [10] proposed area – delay – power efficient low adaptation delay architecture for fixed point implementation of LMS adaptive filter. It also uses inner – product computation to decrease adaptation delay to achieve faster convergence performance & decrease critical path. The proposed design is found to be more efficient in terms of power – delay – product (PDP) & energy – delay product (EDP). It gives degradation of steady state error [10].

2. REVIEW OF LMS ALGORITHM

Adaptive filter has a time variant character, coefficients are adjusted to utilize a cost function or to satisfy predetermined function. Adaptive filters have some important characters are it can adjust their character automatically for changing environment and system requirement (Self Optimize),Decision making tasks and specific filtering process can be performed by using

trained adaptive filters with some updating equations.

Adaptive filter obtain using observation random process x(n) to another random process y(n) with digital filters. Each iteration adaptive filter coefficients are updated, until the coefficients converge which is used to minimize the difference between the filter output and the desired signal. It consists two main block are general filter block, coefficient update block.

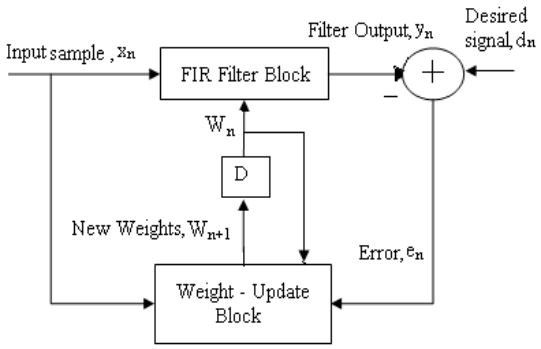

Figure-1. Structure of conventional Least Mean Square adaptive filter.

To implement the LMS algorithm, each sampling period, filter weights can be updated with the estimated error which is equals to the difference between the filter output and the desired response. The n^{th} iteration of the least mean square adaptive filter is updated according to the following equations.

$$W_{n+1} = W_n + \mu e_n x_n \quad (1a)$$

Where,

$$e_n = d_n - y_n \quad y_n = W_n^T - x_n \quad (1b)$$

Input vector X_n and weight vector W_n at the nth iteration given by, respectively

$$X_n = [x_n, x_{n-1}, \ldots, x_{n-N+1}; \quad (1c)$$

$$W_n = [W_n(0), W_n(1), \ldots, W_n(N-1) \quad (1d)$$

Where, e_n is the error computed during the n^{th} iteration, which is used to update the weights, d_n is the desired response, and y_n is the filter output of the n^{th} iteration, μ is the convergence factor or step – size, it should be a positive number, and N is the number of weights in least mean square adaptive filter.

3. PROPOSED SYSTEM

The proposed work is to implement parallel architecture for adaptive LMS filter configuration. Least mean square filter block processed concurrently. Designing the analog filter in digital ways requires a lot of storage and considerations where the filter coefficients are negotiated and uploaded in the look up table. These data is further configured and retrieved from stored buffers. In the proposed architecture achieving low power consumption and high throughput, high speed of the system.

a) LMS Adaptive filter with parallel architecture

In parallel processing, which is duplicated the hardware of the original system and produce the output is multiple and multiple output in a clock period while the effective sampling speed is increased by the level parallelism. While reducing supply voltage in a parallel system, it reduces power consumption of the system.

A direct form LMS adaptive filter have error and weight updating block, which are commonly used area rigorous components like multipliers, weight registers and tapped delay lines. The proposed system error computation and weight updating block not processed concurrently. A single is required for performing both error and weight updating block. While error computation block requires more time than weight updating, the error component block perform in first clock cycle & weight updating block perform in the second clock cycle.

The proposed work is to implement the input data block contains two subs block, configuration input block and input data look up table. Input's (cut – off frequency, weights, and filter coefficients, n^{th} - input) are configured and stored in Look up table.

Least Mean Square filter has (i) F block which is digital filter block, (ii) Weight updating block. The desired signal and estimated error signal is given as input to digital comparator and the output is feedback to the mathematical repeat computation to get the desired round off results. The output is taken from weight updating block and given to repeater with delay and the output is placed in queue data. The next stage is with some small amount of delay.

Figure-2, a concurrently processed filter which adapts the time controlled single blocks is realized here. Designing the analog filter in a digital manner required lots of storage and considerations, where the filter co-efficient are negotiated here which are uploaded in to the look up table. These data are further configured and get back from the stored buffers. Here only the single block is designed hence, depends upon the timing control these blocks are called like a function. This design architecture reduces the area utilized and reduces the Power.

b) Low power architecture technique

The proposed system used to design low power architecture combining the LMS adaptive algorithm and achieving low power and area. The low power coding techniques are (1) clock gating. (2) Power gating. (3) sequenced latching. Clock gating used in synchronous circuits Clock gating used in synchronous circuits for reducing power consumption and also used to saves power by adding more logic to a circuit to prune (to reduce something by removing things that are not necessary) the clock tree. In sequenced latch like a register this case, which is used to store the value, and prevents from the noise signal.

While reducing the power consumption in integrated circuit design power gating technique is used. It is a most widely used technique, which is used to reducing leakage current. It includes to reducing the switches size, portioning the transition delays, and reducing energy dissipation in transition mode.

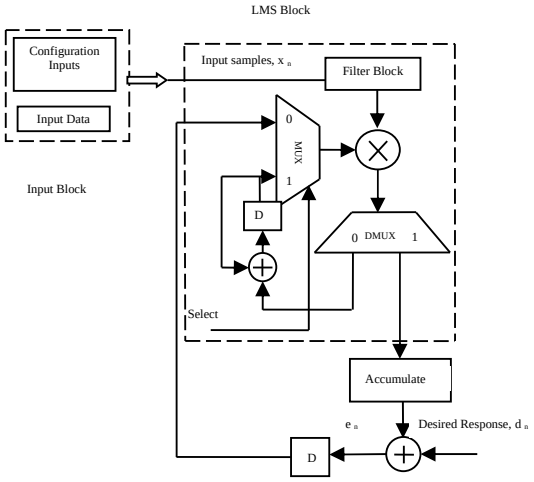

Figure-2. Proposed Single stage LMS Adaptive filter.

In the proposed system, design environment is XILINX ISE and the simulator is MODELSIM simulator. The hardware requirement of the system is XILNX SPARTAN development Board, Complex programmable logic device and the device is XC3S500E.

Thus coded the proposed design in VHSIC hardware description language and synthesized by synopsis.

The proposed system has to design low power architecture combining least mean square adaptive algorithm and achieving low power area.

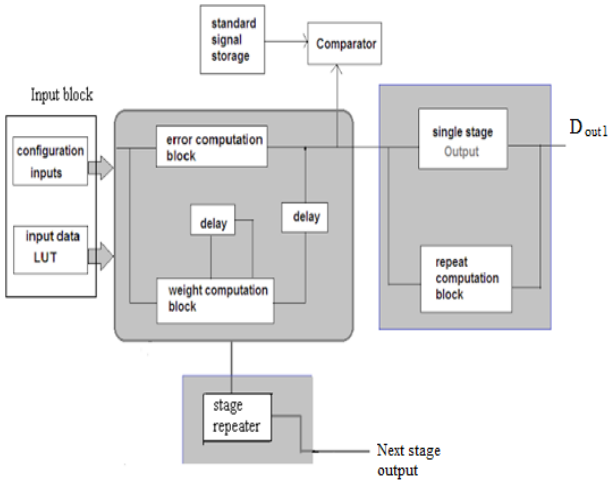

Figure-3. Block diagram of a proposed system.

4. RESULTS AND DISCUSSION

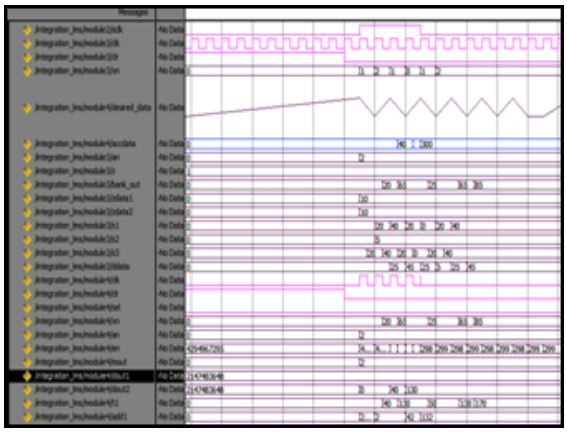

Figure-4. Proposed system simulation output .

Figure-4 shows the output of proposed work [simulation output]

The advantage of the work done is that, data can be included as and when the simulation is taking place. It is observed that there is no loss of data in this work. It is also noted that there is no undetermined state during simulation in this work.

The proposed system when compared to Van and Feng [4] system is efficient as far as power consumption is concerned. While comparing Yi.et al with the work done, as specified in this paper, power consumption is even lower. This is considered as advantage.

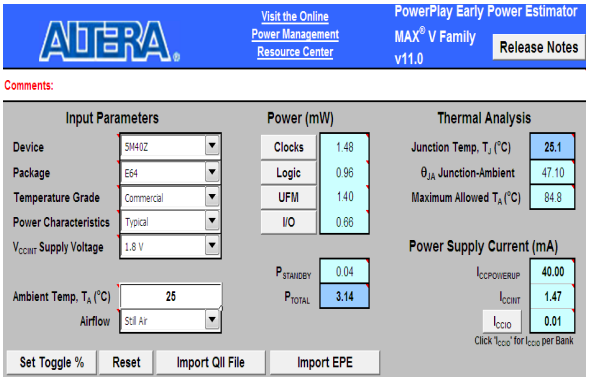

Figure-5. Power and area analysis of proposed system.

Table-1. Comparison with existing.

Design	Performance analysis	
	Filter length	**Power consumption**(mW)
Van and Feng [4]	4	3.24
Yi.et al [7]	4	4.25
Proposed System	4	3.14

5. CONCLUSIONS

Thus, an efficient parallel architecture for direct least mean square algorithm with reduction in power consumption is implemented. The direct form adaptive filter provides less complexity better convergence than transpose form. The proposed system is precise and easy to configure and update which reduces the Power consumption and achieves high throughput due to an efficient parallel architecture.

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