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ANALYSIS OF POWER MANAGEMENT IN PORTABLE EMBEDDED DSP APPLICATIONS

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ABSTRACT

Now a days, embedded systems has greatly improved in terms of performance and features. However the process of managing the power consumption is becoming complicated. Many techniques are proposed to address this issue. In this paper the techniques for reducing the power consumption in discussed. This paper summarises about different ideas regarding the working of different power management techniques so that better techniques can be designed for more efficient and high performance embedded systems. Also this work focuses on most of the portable embedded systems that are used in the real time applications.

Keywords: power management, embedded systems, DSP.

INTRODUCTION

Currently, the applications and usage of embedded systems have shown an enormous growth in day to day life. Embedded systems like single board computers and mobile phones and portable devices are incorporated with the onboard features such as camera, Wi-Fi, net browser etc. It is found that the growth in the embedded systems is increased in proportional to the total population. Many portable systems have strict power consumption of 1W to 2W, [1] While ultra-low power embedded systems have power consumption of mille watts. In case of general graphics processors and system processors the power consumption is in the order of few hundred watts. Therefore in order to maintain the level of reliability, performance and durability of the system power management will be an extremely important factor in case of embedded systems.

This paper focuses on the need of power management in embedded systems and also surveys on various methodologies which are intended to improve the energy efficiency of embedded systems. The classifications of various power management techniques are classified on the basis of their key idea and the application area where the system can be used. It helps the embedded system designers to decide upon many power management techniques while designing the system.

BACKGROUND

An embedded system is a combination of hardware and the software and is tailored for any specific application. It can also be built as the part of the complete system. Thus, for an example a washing machine is an embedded system which is designed for specific tasks. In olden days when the first computer was invented it occupied almost a room which also required more power for operation, later due to the advances in technology the size and the power consumption of the embedded systems are reduced.

Origin of power losses

The power loss in an embedded system takes place in two ways, static and dynamic. First is the dynamic power loss arises from the charging and discharging of load capacitance, and the short circuit currents. The leakage power loss arises due to the leakage currents that flow through the devices when it is kept off. Due to CMOS scaling the leakage power is increased greatly Dynamic voltage frequency scaling (DVFS) based techniques work for reducing the dynamic power loss.

Significance of power supervision

Power supervision in embedded systems is important due to the following reasons

Inadequate size and battery

In all the battery operated and the portable devices the power supply is limitation. Power utilised in the devices leads to heat dissipation. The amount of power lost is beyond the acceptable level. This is a major issue in the portable and wearable embedded systems. Further, due to the small size of these systems the amount of heat dissipation is limited. So, small power consumption will result in the use of small size battery that reduces the heat dissipation, cost and area of embedded system. Thus power management can lead to more efficient and easier system design.

Ensuring endurance

When the temperature raises by 15 degree centigrade the risk of device failures are doubled. Hence the power dissipation has a harmful effect on consistency of embedded systems. This observable fact is crucial for medical and mission-critical systems.

Performance requirements

In recent years embedded processors are used to perform mission critical and real time tasks. In order to meet the performance requirements, multi cores processors and multilevel cache have come in to picture. These advancements have inclined the embedded system design

to provide high performance than concentrating on the power consumption.

Current method of usage

In recent years the mobile computing devices are introduced with new features and applications. Due to this portable devices are used everywhere. Even though these systems consume less power than a main device. The overall power consumption of the embedded devices will be very huge.

Types of management

Based on the energy saving approach the techniques are classified into following categories.

1. DVFS (Dynamic voltage and frequency scaling).
2. Using low power modes, known as power mode management. This is also called as dynamic power management.
3. Micro Architectural techniques for saving energy in specific components.
4. Using unconventional cores such as DSP's or GPU's of FPGA.

Dynamic votage and frequency scaling technique

Power aware scheduling is formulated with the scope to use a dynamic voltage scaling in order to save energy.

DVFS technique is proposed to change the voltage or frequency of a system depends on the performance and power requirement of an application. The dynamic power consumption of the system can be controlled with the help of the DVFS technique. The rigorous analysis of the Complementary metal oxide semiconductor shows that the dyanamic of it entirely depends on the frequency and the square of the voltage, $P\alpha FV^2$. There for it achives a greater energy saving. Now a days many commercial microprocessors support DVFS technology for saving power eg. AMD power save, Intel's Speed step. The disadvantage of this technique is that it doesn't offers better performance in terms of the accuracy of the result obtained and also the system goes slower. DVFS requires programmable clock generators and DC-DC convertors which add extra load to the power supply. Further the voltage transitions requires a few microseconds to stabilize.

Hua *et al.* [44] discusses about the opening available for saving energy in embedded systems using DVFS. Beacause of the overhead associated in providing different voltage levels for a system to perform, the DVFS offers an system incorporated with the advantage providing number of voltage levels with better energy efficiency.

Kianzad *et al.* [54] studied about genetic algorithm to integrate task scheduling and voltage scaling using a single iterative optimization loop. Their technique holds good where the deadline of the task has to be met. The algorithm executes the task as per the schedule in such a way that the energy efficiency is met. Their technique distributes slack proportionally to all the tasks and implements DVFS for saving energy. They propose techniques for saving energy in both single and multicore embedded systems.

Multimedia applications does not require a system to meet the deadline. This is acceptable as it doesnot make much difference in the output. Hua *et al.* [45] utilize this fact, along with the information on statistical task execution time to propose techniques to save energy in embedded systems by dynamic voltage Scaling. They have proposed two algorithms. The first algorithm ensures high completing ratio with possible lowest power consumption. The second algorithm deliberately drops some tasks to create slack for saving additional energy, so that application specific quality of service constraint is fulfilled. Thus these algorithms provide opportunity to scale between high task completion ratio and lowest possible power consumption.

Choi *et al.* [46] propose a DVFS technique which enables achieving a precise energy-performance trade-off. This methodology uses run time information about the CPU usage, Memory usage and selects optimal clock frequency and corresponding minimum voltage level based on ratio of the on- chip computation time to the off-chip access time. Their technique reduces CPU frequency in memory-bound region of a program to avoid the loss in the performance.

Gheorghita *et al.* [47] analyses about the power management technique for both applications scenerios where meeting the deadline is important and where it not mandatory such as hard and soft real time applications. The paper elaborates about the various types of operating modes of the system in order to save energy. As an example, Note pad is used for various purposes such as creating documents, playing videos, playing games etc. Since document creation requires less computational power, battery power can be saved by using smaller voltage level at that particular time. This technique can be used as a guide for real time design choices by providing specific operational modes for specific scenarios. This technique holds good for both hard and soft real time systems.

Saewong *et al.* [58] proposed four DVFS techniques for saving energy in embedded systems. The first technique uses a single operating frequency for the whole execution of the application in such a way that task-deadline is met and energy is minimized. The other technique find suitable frequency same as first technique with the difference that it takes priority in the order off tasks. Hence, if meeting the deadline of a higher priority task requires running other tasks at larger frequency than what is minimally required for meeting their deadlines. Other technique uses nonlinear-optimization to find the optimal frequency, however this process is complex. The fourth technique monitors the actual execution time of the tasks and further optimizes the energy used by the tasks by reducing the time than pre allocated worst case running times.

Quan *et al*. [59] anticipated two algorithms for saving energy in real-time embedded systems. The algorithm depicts a minimum constant speed that can be used throughout the execution process, such that the system is shutdown when idle. The other algorithm supports both constant speed and variable voltage levels for minimizing energy.

Zhu *et a*l. [60] studied about the energy saving technique in multiprocessor systems. It enables the use of processor slack time from the shortest time execution task. By using this extra slack the speed of execution of previous task is reduced which results in saving power. They show that sharing slack enables to meet all the task or process specific deadlines. They show the effectiveness of their technique for both tasks with dependence (i.e. precedence constraints) and without dependence.

Xian *et al.* [61] present a technique for scheduling in multiprocessor systems to save energy. For scheduling periodic real time tasks, their technique uses earliest deadline for scheduling to ensure meeting the deadlines of all the critical tasks and there by minimize the power consumption.

Kan *et al.* [41] propose a DVFS technique for saving energy in soft real-time embedded systems. They find optimal frequency for a task from the available set of frequencies. Afterwards, from the actually available frequencies the closest frequencies which are larger and smaller than the optimal frequency is selected and the fraction of time each off them should be used to meet the deadline is decided. In this method if the first deadline is missed the algorithm can continue with the next deadline such that extra amount of energy is conserved.

Yang *et al.* [71] propose technique for mapping concurrent tasks onto a heterogeneous multiprocessor platform in an energy efficient manner. On different processors, the execution time and the energy consumption of tasks are different. Hence their technique finds a task-ordering and process execution technique in different ways and generates a Pareto-Optimal set such that each point is better than the other one in at least one way. This information is used runtime to save energy using dynamic voltage setting and to find a global energy efficient solution.

Kim *et al.* [30] discuss per-core DVFS technique for saving energy in embedded systems. Scaling CPU frequency will reduce the CPU-bound operations but has a little effect on memory bound operations due to this fact the voltage and frequency are reduced for memory bound operations. Their application finds optimal frequency setting for each operation in offline manner. Use of on-chip regulators enables fine grained voltage transitions using which the memory bound intervals can be more effectively used.

Usage of modes at applications

In embedded systems different hardware provide different operating modes. These operating modes have different amount of power consumption and the time taken for the processor to come back to normal mode. In general, the largest lowest the power consumption the slowest the processor returns to normal mode. For saving the energy while keeping performance loss bounded, these modes should be properly used. Also when a low power mode is used when the system is idle it should return back and process the task when requested.

Li *et al.* [78] propose a method for selecting the power modes for the optimal power management of embedded systems under timing and power constraints. Their system proposes timing based mode transition such that the system can meet power and performance requirements.

Hoeller *et al.* [79] propose an interface for power management of hardware and software components. This method allows applications to express when certain components are not being used, based on this power management can be done by transitioning the individual peripherals or entire system into low-power modes. This frees the programmer task of manually setting and controlling the power modes.

Huang *et al.* [76] propose an energy saving technique which works by adaptively controlling the power mode of the embedded system according to historical arrivals of tasks. Their technique take decision regarding when to transition the system from low power mode to normal mode and vice versa, depending upon the energy efficiency of a particular mode and the consideration of meeting the deadlines.

Bhatti *et al.* [26] present an online framework to integrate DVFS with power-mode management (PMM) scheme to save energy in embedded systems.

Niu *et al.* [6] propose a technique to save both leakage and dynamic energy in embedded systems by integrating DVFS and PPM. In this case when the processor is active, their technique chooses a processor speed such that the dynamic power and leakage power are balanced. In case if the processor is in idle state the system delayes the coming tasks as much as possible such that their deadlines are not missed or scattered. Also short idle intervals are merged in large idle intervals such that the system can stay either in idle mode or in active mode for a long time.

Kim *et al.* [55] study the trade-off between voltage scaling and dynamic power-mode management. Under the assumption that voltage scaling will not reduce the power consumption in peripheral devices. Further voltage scaling will increase the execution time and increases the leakage energy consumption. Also the opportunity to send the device to low power mode is greatly reduced. Towards this, they propose a technique which exploits task-slack by partitioning the task execution into several intervals and shuts down the unneeded peripheral device on a per-interval basis.

Shin *et al.* [32] propose a technique for saving energy by integrating DVFS and PMM. In real time embedded systems idle times arises due to inherent slacks and priorities or early completion of tasks than their worst case time. They use Offline DVFS approach for saving energy.

Cheng *et al.* [80] propose an online technique for performing energy-aware I/O scheduling for hard real-time systems. Their technique uses system slack to perform power mode transitions to save energy. Their system performs inter-task scheduling not intra-task scheduling , since it may lead to missed deadlines which will be critical in the case of hard real time systems.The decision to transition are taken based on break-even time calculation, which shows the minimum time the device needs to be idle for the mode transition to provide positive energy savings.

Awan *et al.* [81] propose an approach for saving energy in embedded systems using multiple low-power modes. Their technique uses offline analysis and computes break-even time for each mode. Since high priority tasks create slack, their technique accumulates this task by allowing the device to stay in idle mode for longer time.

Cutback energy in explicit components

Several researchers propose micro architectural techniques for saving energy in embedded systems.

Yang *et al.* [82] discuss a technique for saving main memory energy in embedded systems. Their technique uses software based RAM compression to increase the effective size of memory. The memory compression is only used for the applications which get benefit in performance or energy. For such applications the compressed RAM area is changed dynamically.

Trajkovic *et al*. [83] propose a buffering based technique for saving energy in low-power embedded systems.

Reddy *et al.* [89] present an approach for saving cache energy in multitasking embedded systems. Their algorithm selects best cache partitioning available for different applications in an offline manner and uses this information to allocate cache at runtime. Their algorithm also reduces inter-tasking interference in a multitasking environment.

Tsai *et al.* [106] propose a technique for saving energy in embedded processors by using a memory structure called “Trace Reuse cache” (TRC). It uses the same memory hierarchy as that of normal instruction cache. TRC reuses the instructions from the pipeline back-end of processor and efficiently delivers the instruction sin form of traces. Thus, TRC enables the processor to achieve high performance and reduce the power consumption.

Hajimiri *et al.* [92] integrate cache reconfigurationand code compression to improve both performance and energy efficiency of embedded systems. Their technique performs exhaustive exploration of cache design space by varying line size, total size and associativity. Different simulations are done and based on the results the configuration with minimum energy can be selected. Since doe compression increases the execution time it partially covers up for the performance losses due to cache reconfiguration.

It is aware that there is a long intra and inter program variation in cache requirement of different programs. Using this cache can be dynamically allocated based on the application requirements and the unused space can be turned off to minimize power consumption. Based on thisidea, Albonesi [103] proposes selective-ways approach where some of the ways of the cache are turned off to save energy, such that performance degradation remains bounded.

Zhang *et al.* [99] propose highly-configurable cache architecture for facilitating dynamic reconfiguration to save energy in embedded systems. Their cache architecture contains four separate banks such that each bank operates as 4 separate ways. By concatenating these ways the associativity of the cache can be changed.

CONCLUSIONS

To meet the challenges in the present day, management of power at different level is most important. The power can be analysed and managed at chip level, architectural level, application level and system level. This paper presents an idea in how the power could be managed for better performance of the embedded systems. Our work can be focused on the architectural level power management in low power and portable embedded systems. Especially it can be useful in the medical applications.

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