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DIFFERENTIAL 10T TCAM WITH PARALLEL PAI-SIGMA MATCHLINE

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ABSTRACT

A low power differential 10T TCAM with parallel Pai-Sigma matchlines is presented which consumes less compare power during search operation, compared to 6T-TCAM. It performs parallel comparison with stored data which reduces power consumption of matchlines of TCAM and also search time is reduced .The NAND and NOR type matchlines are combined to form the Pai-Sigma matchlines. If NAND (NOR) type TCAM cell is used then NAND (NOR) type matchline is used. NOR type TCAM has feature of high speed and high compare power. NAND type TCAM has low speed and low compare power. In Pai segment the NAND type cells are connected in parallel to form the NAND type matchline. In Sigma segment NOR type cells are connected in series to form the NOR type matchline. The matchline incurs the problem of short circuit current due to mismatch and match result of NAND and NOR matchlines. NAND type matchline exist the problem of charge sharing when the search result of the NAND line is mismatches. This proposed TCAM has less compare (search) power compared to the NAND/NOR type TCAM cell.

Keywords: match line (ML), search-line (SL), match line search amplifier (MLSA), parallel pai-sigma match-line (P^2SML), ternary content addressable memory (TCAM).

INTRODUCTION

Content Addressable Memory (CAM) is application oriented memory that executes search operation in a single clock cycle. It can be used in mobile devices to check viruses. CAM can be divided into two types 1. TCAM 2. BCAM. TCAM can store ('0', '1','X') bits, where 'X' bit can be used as wild card entry and called as don't care or mask bit. CAM can be used in commercial application like packet forwarding and packet classification in Internet Protocol. A large email in the internet is subdivided into small packets. Then each packet address is compared with the look-up table and finally routed to destination address through network router.

CAM cell performs two types of function one is bit storage and another is bit comparison. Bit storage can be done by cross coupling two inverters. NAND and NOR type cell implements the bit comparison and it is types of CAM cell. Both CAM cells perform XNOR function. For look-up operation in network routers CAM [3] is a good choice due to its fast search capability.

Basic TCAM cell is shown in Figure-1. In_address is the input address of the data. Decoder selects the input address and applied to all data words. Search data register is used to store the input search word. When stored data word and search data word will matches the hit signal is generated at the hit signal generator. Priority address encoder [6] gives the highest priority address among the bundle of matches. Data word will be stored in NOR / NAND type TCAM cell. When designing a CAM circuitry power consumption is main concern, because each search operation begins with the parallel comparison with the stored data. NAND type CAM is slowest but consumes less power. NOR type CAM is fastest and consumes too much power. Based on type of CAM cell matchline type is selected.

CAM architecture [11] is shown in Figure-2. It consists of 3 data words and 4 bit (4 cells). ML_0, ML_1, ML_2 are matchlines connected matchline sense amplifier (MLSA) for each CAM word.

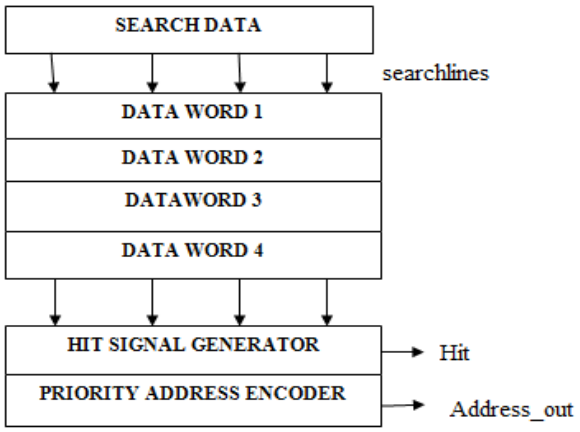

Figure-1. TCAM cell.

Search operation begins with loading the search data into search data register [1]. Each search line and its complement connected to each CAM cell. Matchlines are precharged to high i.e. default state is match state. Each bit in the search data is broadcasted into corresponding search lines that compares search data against the stored data. If comparison result is matched, the corresponding matchline is in precharged state. Otherwise matchline is discharged to ground. NOR and NAND type TCAM cell has SRAM cell, where cross coupled inverters can serves as bit storage nodes.

This paper presents a differential 10T TCAM with Pai- Sigma matchline to reduce the power consumption of matchline.

The proposed matchline does not have the problem of charge sharing and short circuit current. The switching activity of the search line is low.

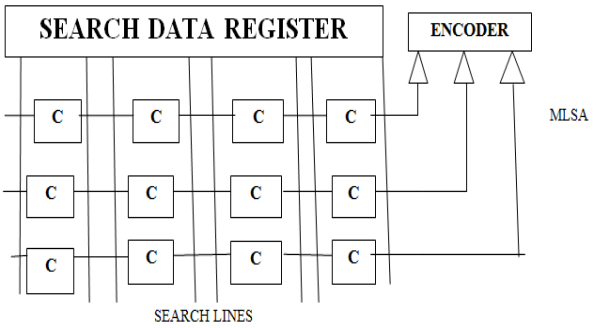

Figure-2. CAM architecture.

PARALLEL PAI-SIGMA MATCHLINE

NOR type TCAM cell is shown in Figure-3. It has BCAM bit, mask bit and also two NMOS transistors are connected in series. NOR type matchline is used for the NOR type TCAM cell. When TCAM executes a compare operation, the matchlines are precharged to V_{dd} during the precharge phase. Based on the comparison result either matchline remains precharged state (match) or discharges to ground (mismatch). The status of transistors determines the output. If all transistors are off, no discharge path through the transistors. It indicates the matched output. If the transistors are ON, precharged matchlines are connected to ground via discharge path. For speed and power consumption concern both NOR and NAND type TCAM cells are used.

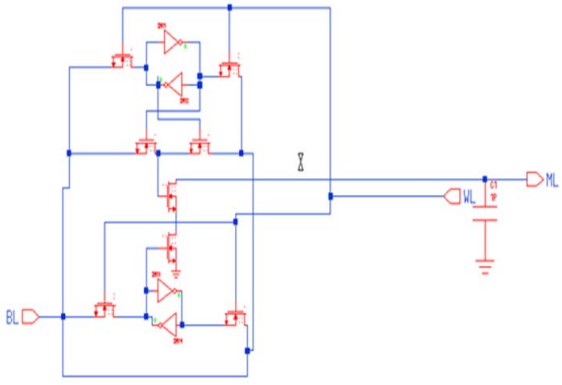

Figure-3. NOR type TCAM cell.

NAND type TCAM cell two NMOS transistors connected in parallel which is shown in cross coupled inverters forms the bit storage. When both the search data and stored data will match, the output of matchline will be high.

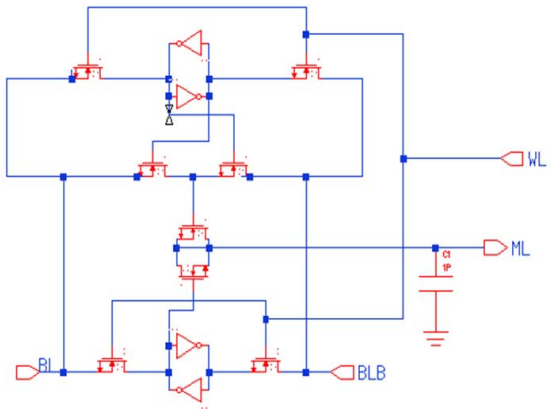

Figure-4. NAND type TCAM cell.

To reduce the power consumption of the TCAM cell many techniques were demonstrated. Matchline partitioning method is one favorable power reducing method. In this method matchline is partitioned into NAND type matchline [6] and NOR type matchline. Both types of matchlines are combined to improve the performance of TCAM.

In Pai matchline structure, NAND type TCAM cells are connected together. Each match result is propagated from one cell to another consecutive cell. Similarly all the bits are parallely compared. If single bit mismatch occur the matchline is grounded, so the path is disconnected. The Pai segment realizes the NAND function. In Sigma matchline structure, NOR is type TCAM cells connected in parallel. Sigma segment realizes the NOR function.

Pai segment and Sigma segment [7] are merged together to reduce the compare power. During search operation NAND type matchlines are activated to achieve high speed. Based on the result NOR matchlines are activated to reduce the power consumption. Delay of the NAND-NOR matchline is less than the NAND match-line.

Single Pai-Sigma matchline method incurs the problem of short circuit current and charge sharing. Short circuit current problem can be alleviated by using replica of matchline. But this method has area overhead and leads to process variation. By precharging the matchlines to high state, charge sharing is eliminated. Search lines are precharged to V_{dd}-V_t. All intermediate nodes are precharged to V_{dd}. NAND matchline still has the problem of charge sharing.

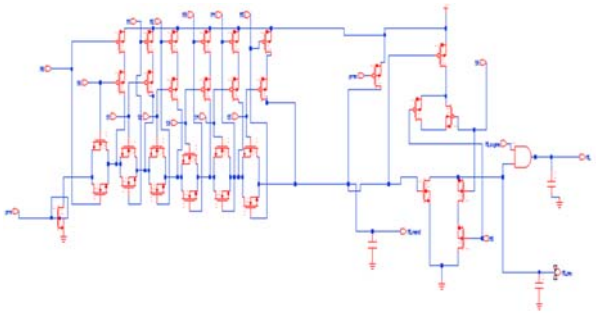

Figure-5. Single Pai-Sigma match-line.

Table-1. Match result.

ML_{Pai}	ML_{Sigma}	ML_{NAND}	ML
0	0	1	0 (match)
0	1	0	0 (mismatch)
1	1	1	1 (match)
0	0	0	0 (match)
1	0	1	0 (mismatch)

The function of single Pai-Sigma matchline is shown in Table-1. ML_{Pai} and ML_{Sigma} performs the AND function. During the precharge phase Pre = 0. Pai segment internal nodes are precharged to V_{dd}. When both the data are same the output will be match.

Based on the number of bits in the Pai segment, power consumption and speed is determined. By reducing the product of speed and power the energy required for search operation is minimized. The product of power and delay is minimum [12] when the number of bits is in range 8 or 10. The TCAM is simulated for 8 bits. To reduce power and delay the Pai segment and Sigma segment is partitioned into 2, 4 or 8 sub segments. Among the all segmentation 2 sub segments are selected. Two sub segments are evaluated using interface logic.

Figure-6 shows parallel Pai-Sigma matchline. PaiA and PaiB are two segments of Pai segment. SigmaC and SigmaD are two segments of Sigma segment. Pai segment is precharged to V_{dd}. The precharging operation of Sigma segment is controlled by ML_{Pai}. If search result of Pai segment is match then ML_{Pai}=0. Then the Sigma segments are precharged to V_{dd}. AND operation of ML_{PaiA} and ML_{PaiB} is ML_{Pai}.

Table-2. Pai segment function.

ML_{paiB}	ML_{paiB}	ML
0	0	0
0	V_{dd}	0
V_{dd}	0	0
V_{dd}	V_{dd}	V_{dd}

During compare operation the precharge signal is set to '0', so ML_{PaiA} will be zero. Then the matchlines of SigmaC and SigmaD are precharged to V_{dd} in the precharge phase. ML_{PaiA} and ML_{PaiB} are logic 1 when the result is match in the evaluation phase.

The NMOS transistors in the Sigma segment is turned on and two segments of Sigma segment [12] are in evaluation phase [12]. ML is at logic 1, when the comparison result of SigmaC and SigmaD are at logic 1 (match). Charge in the Sigma segment is not discharged to ground when the output is mismatch in the Pai segment.

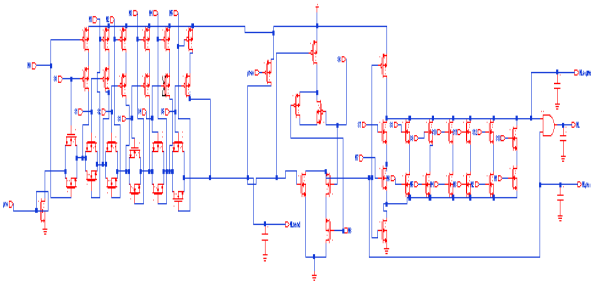

Figure-6. Parallel Pai-Sigma match-line.

PROPOSED DIFFERENTIAL 10T TCAM WITH P²SML

The differential 10T TCAM lower power consumption and delay associated with the matchline is low. Figure-7 shows the differential 10T TCAM. It has four NMOS transistors connected like mirror image.

B and BLB are input bits to compare with the stored data. During the compare operation WL (word line) is at logic '1'. If stored data does not matched with the search data matchline (ML) is connected to ground via the two NMOS transistors.

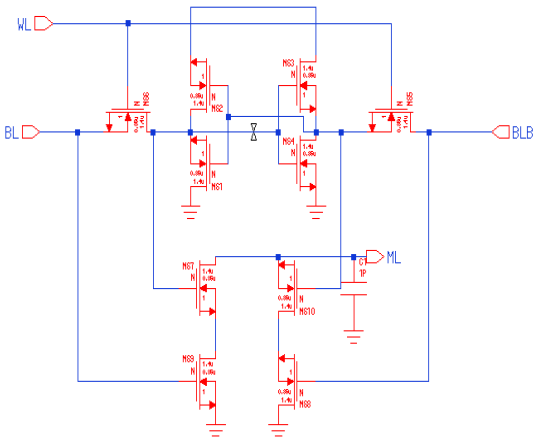

Figure-7. Differential 10T TCAM.

Figure-8 shows the NOR type TCAM using the differential 10T TCAM. It executes the XNOR [8] operation that is when both data are same output will be logic 1. If both the data are not matched the output will be

at logic 0. Figure-9 shows the differential NAND type TCAM in which two NMOS transistors are connected in parallel.

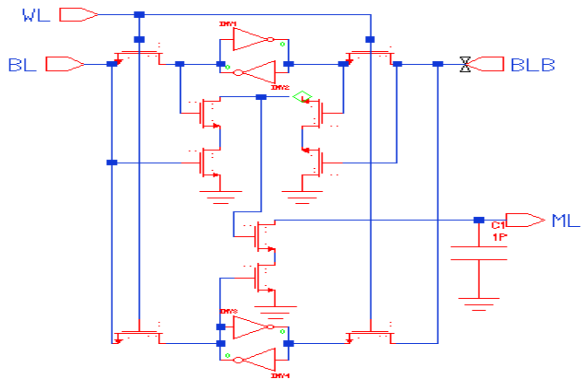

Figure-8. Differential NOR type TCAM.

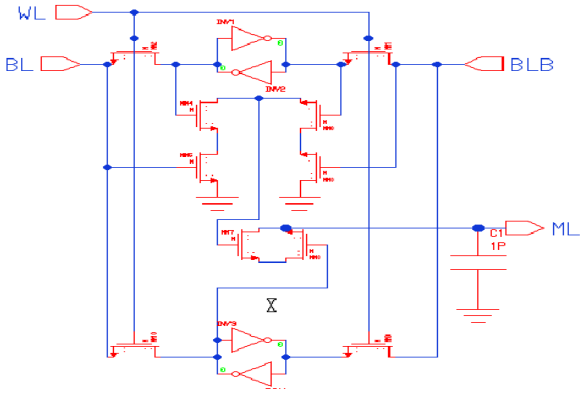

Figure-9. Differential NAND type TCAM.

Differential 10T TCAM for 8 bit is shown in Figure-10. In precharge phase all the matchlines are charged to V_{dd}. For searching stored 'X' bit in the TCAM cell search bits are set to '00'. Don't care bit can be stored by setting cross coupled inverter nodes D = 1 and D' = 1 i.e. disables the both pull down paths regardless of the inputs. Storage and search bit conditions are shown in Table-3.

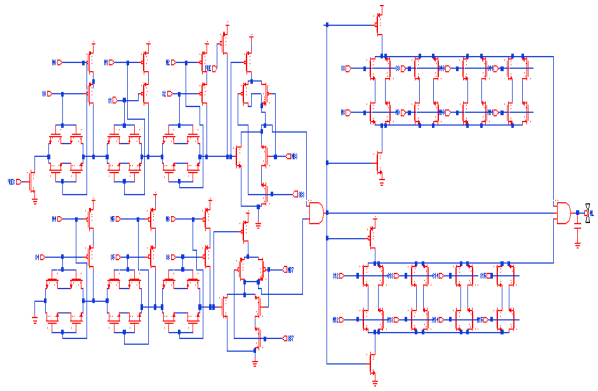

Figure-10. Differential 10T TCAM with P^{2}SML.

Table-3. Search conditions.

Stored Value	Storage D	Nodes D'	Search BL	Bits BLB
0	1	1	0	0
1	1	0	1	0
X	0	1	0	1

Table-4 shows the power consumption and operating frequency of the proposed TCAM.

Table-4. Comparison of TCAM.

Technology	P^{2}SML	Differential 10T TCAM
Operating frequency	60MHz	60MHz
Operating voltage	1.8V	1.8V
Power consumption	0.286mW	0.256mW
Energy	2.287 (fJ/bit)	2.102 (fJ/bit)

RESULT DISCUSSIONS

Differential 10T TCAM result is shown in Figure-11. Initially the coupled inverters store the bit. When the stored bit and search bit are same, the matchline is in precharged state.

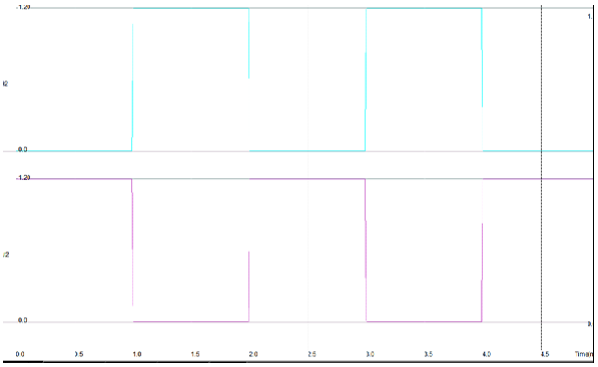

Figure-11. Differential 10T TCAM.

Simulation result for NAND type differential TCAM is shown in Figure-12. By setting word line to logic '0', the storage of data bit in the inverters starts. The stored bit is logic '0'. The search bit in bit line BL will be pattern of ones and zeros (address INPUT). When the BL bit and stored bit will be logic 1, ML output will remains in the V_{dd} condition. when BL and search bit will be mismatches i.e. '10','01' the ML output will discharges to ground.

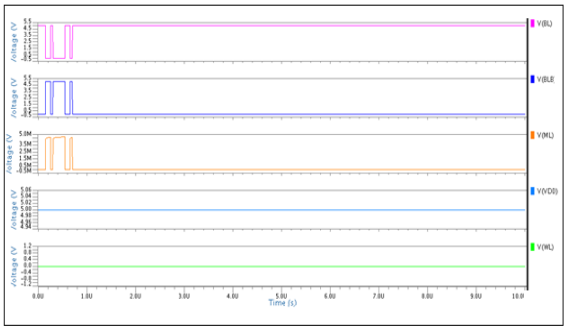

Figure-12. Result of NAND type differential TCAM.

Both NAND /NOR type differential TCAM executes the XNOR function. NOR type differential TCAM is shown in Figure-13.

Figure-13. Result of NOR tye differential TCAM.

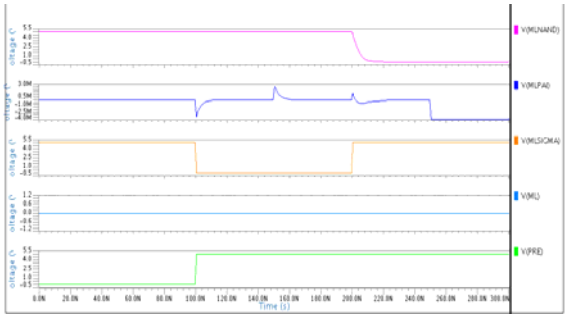

Figure-14. Result of proposed TCAM with P^{2}SML.

Figure-14. Shows simultion result of the proposed TCAM with Parallel Pai-Sigma matchlines. Based on the result of Pai sigments , Sigma sigments are activated. This method reduces the power consumption of the Sigma segments, when Pai segment result is mismatch.

Table-5. Circuit performance.

TCAM TYPES	SWITCHING ACTIVITY	DC SHORT CIRCUIT PATH	CHARGE SHARING
AND TCAM	0.25	YES	NO
NOR TCAM	0.5	NO	NO
P^{2}SML	0.25	NO	NO
Differential TCAM	0.22	NO	NO

Table-5 shows the circuit performance of the various type of TCAM. Switching activity of the searchlines is low. Energy required for search operation also reduced. Operating frequency of the circuit is 60MHz.

CONCLUSIONS

In this paper the proposed TCAM does not have short circuit current and charge sharing problem. Based on Moore's law transistor count is increased but area reduction is achieved. Switching activity of the proposed TCAM is low. This paper reviews the NAND and NOR type matchlines with differential 10T TCAM. The proposed TCAM layout will be designed using EDA tool. The segmented matchline overcomes the static power dissipation. For the future work differential TCAM architecture would be applicable to low power and high performance memory related devices.

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