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INVESTIGATIONS ON LIFTING SCHEME BASED DWT OFDM AND ITS FPGA IMPLEMENTATION

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ABSTRACT

One of the most promising modulation techniques is Orthogonal Frequency Division Multiplexing. In most of the wireless and wired standards, it has been widely adopted. The main idea of OFDM is to utilize the numerous number of closely spaced orthogonal subcarriers into a parallel stream of channels to transmit data. Here in this paper, implementation of DWT based OFDM in FPGA is done using lifting scheme architecture. The lifting scheme of DWT architecture is made by using both System generator XILINX and Simulink MATLAB and the results are analyzed. Also the linking of lifting scheme with OFDM is done. The FPGA implementation of DWT based OFDM using lifting scheme is done using Spartan 3E FPGA.

Keywords: DWT, OFDM, FPGA.

1. INTRODUCTION

Orthogonal frequency division multiplexing (OFDM) is a technique that transmits a single stream of data over a multiple number of carriers. It is a modulation and multiplexing schemes which is robust against frequency selective fading. The arrangement of the N number of sub is in such a way that all are orthogonal to each other. So that the total space occupied will be less and also without inter carrier interference (ICI) .So by this way the available spectrum has been used in efficiently [1]. This can be practically achieved by using IFFT block in the transmitter end with N number of inputs. So after performing the N point IFFT the modulated and multiplexed signal with all the error correction coding reaches the channel and it is given by the expression [2],

$$X_k = \frac{1}{N}\sum_{m=0}^{N-1} Xm\, e^{j2\pi kn/N}$$

So at the receiving end, once the signal is received the reverse process of above sequence happens and by performing FFT the number of modulated sub carriers can be extracted and it is given by the expression [3],

$$X_m = \sum_{k=0}^{N-1} X_k\, e^{j2\pi km/N}$$

The above said process is common in most of the wireless systems which uses OFDM. This OFDM is said to be conventional OFDM. Even though due care is taken in designing the conventional OFDM, the orthogonality is affected which leads to ICI .To avoid this and to guard this against ICI inclusion of cyclic prefix has made into practice [4].

Cyclic prefix is nothing but the extension of the available signal that is a small portion of the redundant information. By using this cyclic prefix at the rear end by deploying a single tap of filter we can demodulate the signal which will be in linear convolution form is correspondingly converted into cyclic convolution form[5].This cyclic prefix, which is a must in conventional OFDM occupies some definite space and restricts the efficiency by 20 to 25% [6].

So at the receiver side it is possible to calculate the correlation values with respect to the center frequency of sub channels, obviously without any crosstalk. Band pass filtering and similarly base band processing can be achieved by the usage of multicarrier technique based on DFT.

The hardware performing Fast Fourier Transforms (FFT) can be built to eliminate those sub channel oscillator and the coherent demodulators. These high speed hardware can be built out by using Very Large Scale Integration Techniques (VLSI) .Using these efficient FFT techniques the transceivers are implemented which reduces the number of operations in DFT from N2 to N log N [12], [13], [1].

Maintaining orthogonality within the carriers is the key of OFDM. While doing the integration over a time period T, if we get the value as zero if and only if the the signals are orthogonal to each other. This is the criteria for the signals to be orthogonal. Therefore, mathematically orthogonality can be represented as: [4], [14], [15].

$$\int_0^T COS(2\pi n f_o t)\cos(2\pi m f_o t)\,dt$$

Where, n, m: unequal integers; f_o: fundamental frequency; T: time period.

For present day data rate the conventional OFDM may be enough but in near future the wireless system will be of so much of data hunger and there by the restriction over efficiency may not be a tolerable one. So we need a system which is free from cyclic prefix and also free from ICI. In order to avoid ICI without cyclic prefix, we need to transform the overlapping nature. This leads to the replacement of IFFT/FFT to IDWT/DWT [7], Where IDWT is inverse discrete wavelet transform and DWT is discrete wavelet transform [8], [7].

In DWT based OFDM, the system which uses IDWT block in place of IFFT block and DWT in place of FFT block. So far this DWT based OFDM is in the laboratory level and some of the papers [8], [9] researches the theoretical possibilities of the same. In this paper the possibility of DWT based OFDM using lifting scheme is investigated and also the implementation of the same is carried over FPGA. For this the further paper is formed as, the second section describes the system model of both conventional OFDM and DWT based OFDM. And the third section details about the DWT based OFDM based on lifting scheme. The next section describes its FPGA implementation process and the succeeding section depicts and discuss about results.

2. OFDM SYSTEM MODELS

The OFDM system model comprises both conventional OFDM and DWT based OFDM models. Here in this section the description of both conventional OFDM and DWT based OFDM is given.

a) Conventional OFDM

Conventional OFDM in the sense IFFT block is used in the transmitter and FFT block is used in the receiver. This idea have been proposed in the mid of 1960s. In the IFFT block N point operation takes place. After the necessary modulation and multiplexing techniques the signal is transmitted through the channel. In case of error suitable error corrections are made and the same inverse operations take place correspondingly in the receiver [2] [3]. The main drawback of this system is that we have to deploy cyclic prefix and similarly the bandwidth which is available for the transmission of the signal is reduced. The Figure-2 shows the necessary blocks for the transmission of the signal, if we are using IFFT/FFT instead of those IDWT/DWT blocks given in the figure, we have to include addition of cyclic prefix and correspondingly the removal of same.

b) DWT based OFDM

In DWT based OFDM, the IFFT is replaced by IDWT and FFT is replaced by DWT. The transceiver model in Figure-1 gives the idea about the DWT based OFDM system, the input sine wave is given to the modulator, and thereby converting data into modulated signals. These modulated signals are given to the IDWT block where the parallel transmission of data through the channel takes place [10], [11].

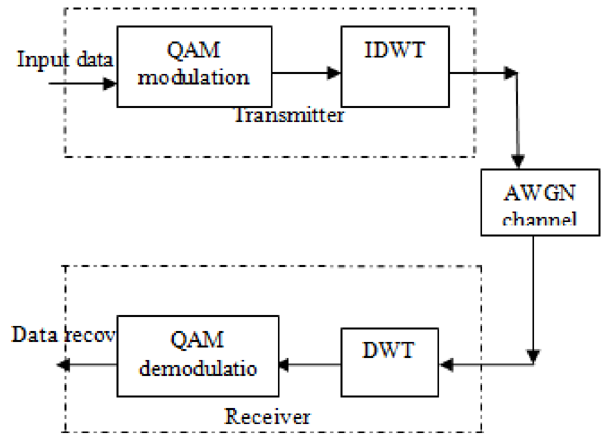

Figure-1. An OFDM transceiver model representation.

The signal which is received through the channel is retrieved at the DWT block. Then the signal is demodulated and the signal is recovered.

3. DWT BASED OFDM BASED ON LIFTING SCHEME

The introduction of lifting scheme in the DWT based OFDM system results in minimum number of calculations and also the computational complexity of the system is reduced. Figure-2 represents the lifting scheme representation for N=3. It consists of mainly 3 steps splitting, lifting, and scaling. Here we are dealing with three stages. The output of the 1st stage is given as input to the 2nd stage and similarly the input to the 3rd stage is 2nd stage output.

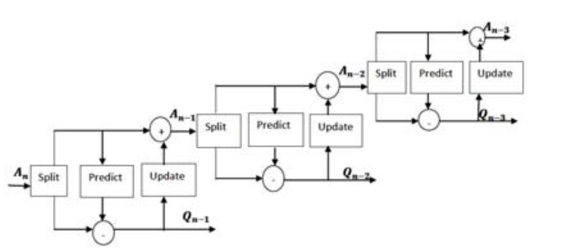

Figure-2. Lifting scheme for N=3stages.

The lifting scheme steps are:

Split steps

In split step the input data which is given is splitted into even and odd samples; even samples are represented by Xen and Xod for odd samples.

Lifting steps

In this step, predict and update filters are included. The even sample is given to the predict filter and the odd samples are predicted from the even samples and the predict filter is followed by the update filter. From the update filter smooth output is obtained.

In this the number of stages for predict and update filter will be three. That is the output of the first

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stage is given to the second and similarly the output of the second is given as the input to the third stage.

Therefore the equation obtained for the third stage will

Predict 3: YHp(i) =J(i) + t[v(i)+v(i+1)]

Update 3: YLp(i) = v(i)+ u +]

Where t= -1.586134342, u= -0.0529801185 and v=1.39604398.

YHp gives high pass filter coefficients and YLp gives the low pass filter coefficients.v is the scaling factor used and J (i) is the output of the 2nd stage which is given as the input to the 3rd stage.

Scaling steps

In this stage the scaling of the functions obtained from the predict and update filter has been done. And the scaling factor is denoted as and is given as v=1.39604398.

4. FPGA IMPLEMENTATION

The implementation of the DWT based OFDM using lifting scheme has been done effectively in Spartan 3E kit. Before the direct implementation to the FPGA effective linking of DWT based OFDM using Lifting scheme has been done. For that two different softwares has been used and they are linked together to obtain the output. Simulink from MATLAB has been used for modeling of DWT based OFDM and System generator from XILINX has been used for lifting scheme. And they are linked together. Table1 represents the hardware utilization report obtained after implementing the linked model of OFDM with lifting scheme in Spartan 3E FPGA.

The modeling of DWT based OFDM using Lifting scheme is done in Simulink and the corresponding Vhdl Code is generated and its simulation is done. The below shown synthesis report gives the idea about the resources allocated for this particular OFDM implementation.173 slices, 4 flip-flops and 4 LUTs are required.

Table-1. Hardware utilization report.

Logic utilization	Used	Available	Utilization
Number of slices	173	407600	4%
Number of slice flip-flops	4	203800	2%
Number of 4 input LUTs	4	173	2%
Number of bonded IOBs	152	400	38%
Number of BRAMs	1	200	.5%

5. RESULTS AND ANALYSIS

(a) Simulation using wavescope

Here the simulation is done using Wavescope and the results are analyzed. Lifting scheme based DWT architecture is proposed using (9/7) Db filter. The transformation of design from higher abstraction to lower abstraction is synthesis. The DWT design using Lifting scheme is carried out on Spartan 3E development kit. Figure-3 represents the representation of DWT architecture of Lifting scheme when N=3.The lifting scheme architecture is made by using both System generator from Xilinx and the Simulink MATLAB. The simulation result is shown in Figure-4 using Wavescope.

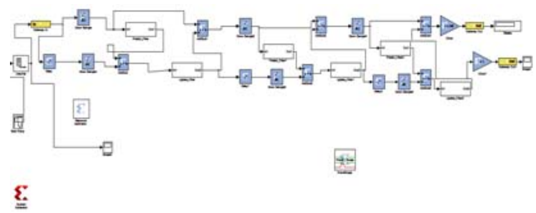

Figure-3. Simulink representation when N=3.

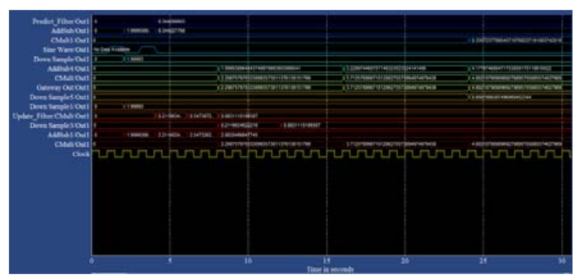

Figure-4. Simulation result using Wavescope.

(b) Simulation resut of linking of lifting scheme with DWT based OFDM

The Lifting scheme which is made using Simulink MATLAB and System generator XILINX is linked effectively With the DWT based OFDM. DWT based OFDM is made using SIMULINK MATLAB. The simulated waveform is obtained using Wavescope and is verified. Figure-5 represents the linking of DWT based OFDM with Lifting scheme. And the Figure-6 represents the output obtained for the linking of lifting scheme with OFDM.

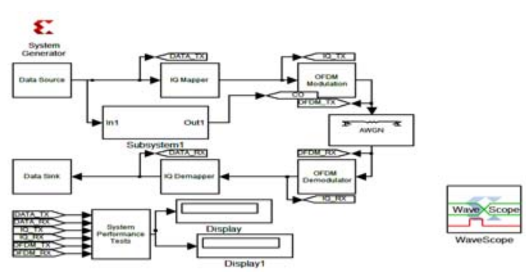

Figure-5. Simulink representation of linking of DWT based OFDM and Lifting scheme.

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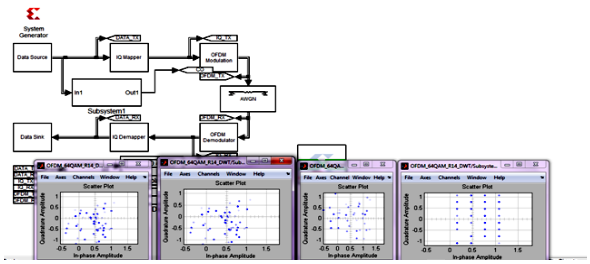

Figure-6. Output obtained for Linking of lifting scheme.

Here the Figure-7 represents the simulation waveform of linking of DWT based OFDM using Lifting scheme. The waveform representation shows the transmitted signal is effectively obtained at the receiver side.

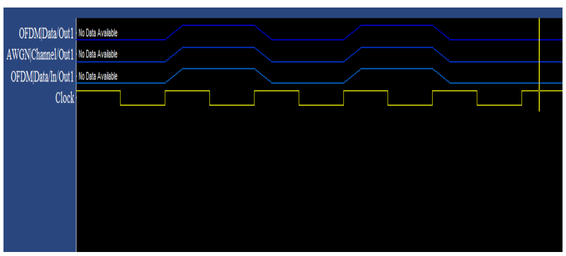

Figure-7. Simulation result of Linking of DWT based OFDM and Lifting scheme using Wavescope.

The RTL schematic of the designed lifting based DWT OFDM architecture is obtained by the Schematic view tool in Xilnix ISE, which is shown in Figure-8. After the synthesis process netlist will be generated. This netlist is saved in Vhdl.

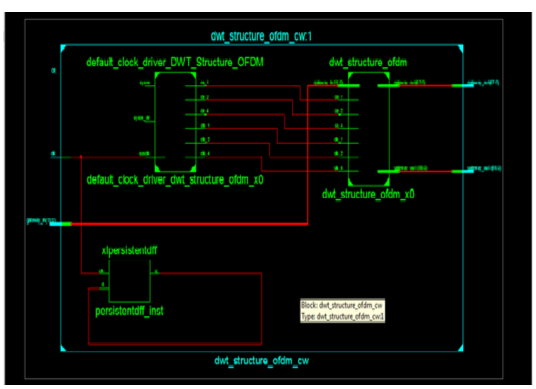

Figure-8. RTL schematic diagram of DWT based OFDM with Linking.

6. CONCLUSIONS

In this paper the simulation result approaches for the linking of lifting scheme with DWT based OFDM are presented. The software reference model is made in Simulink MATLAB and System generator using XILINX. The linking is done effectively and the corresponding RTL schematic diagram is obtained. From the synthesis report, out of 9312flipflops, 174 are used. Then the obtained design is implemented on Spartan 3E FPGA and are analyzed.

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