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DESIGN OF LOW POWER HIGH SPEED DRAM ARCHITECTURE USING DUAL EDGE TRIGGERED FLIP FLOP

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ABSTRACT

Memory power consumption plays a major role in the multi-core computer platforms. Now a day, the bandwidth and the capacity of the memory data rate is increased. Due to that, the power consumption becomes higher and higher in the memory which covers a maximum power consumption in the system .Generally, conventional memory system do not provide an efficient mechanism for managing its power and performance tradeoff. Mini-rank architecture is designed for the DDRx memories by breaking each DRAM rank into multiple narrow mini-ranks and activates only fewer devices for each request which reduces the memory power consumption. This technique will cover large area due to different mini-rank configurations in the memory and the data transfer in the signal is slightly slow due to single edge triggered flip-flop. Thus, the structure of the mini-rank architecture is designed efficiently by combining different configuration in the common memory by introducing memory select line for selecting the x32, x16, and x8 bit configurations and also dual edge triggered flip flop is implemented in the memory to reduce the count of the clock cycle.

Keywords: DRAM architecture, low power, DIMM, DETFF, mini-rank design technique.

1. INTRODUCTION

DRAM memory is used in the wide range of electronic applications. The only purpose of the memory is to store the data for the future references. Generally, conventional memory system is a simple and rigid organization which does not provide an efficient mechanism for the power and performance trade off. In a DDR2/DDR3 DRAM memory system, multiple DRAM devices combine to form a group called Rank that should be match with 64-bit data path and serve as a single memory request. Due to that the memory bandwidth is increased but slow improvement on DRAM row and column access which leads to reduction in the bus transfer time and counts only for a small portion in memory access latency in today's memory system. In order to overcome this problem, mini-rank memory system design technique is developed in the DRAM architecture that achieves the significant memory power reduction with slight increase in data transfer time. In this technique, a bridge chip called mini-rank buffer(MRB) is obtained on each DIMM and placed between DDRx buses and devices to break the conventional x64rank into x32, x16 or even smaller to save the memory power. Now, each request is served only by the chips within the mini-rank. Therefore, the DRAM operation power is reduced proportionally. Depending on the bandwidth requirement and memory access behavior for each workload, the power consumption and performance is not achieved properly. So that, heterogeneous mini rank design technique is developed. To improve the overall performance of the system, a newly designed mini rank memory is replaced to the existing memory and the DETFF is introduced in the DRAM architecture.

2. RELATED WORKS

Kun fang *et al*. [1] proposed a new technique called mini-rank design technique which is used to reduce the power consumption by breaking the DRAM ranks into narrow mini-ranks and developed a heterogeneous mini-rank design to balance the power and performance of the memory in the DRAM architecture.

J.H. Ahn *et al*. [2] designed a new method called rank sub setting. The rank sub setting saves the dynamic main memory energy by dividing a memory rank into sub set and also reduces the memory over fetch. The main advantage of the rank sub setting is high-reliability and develops higher system-level energy efficiency and performance at the cost of additional DRAM devices.

Ibrahim Hur *et al*. [3] describe a new approach for memory controller to improve the DRAM energy efficiency and DRAM power. In order to improve the efficiency, we describes a simple power down model for exploiting low power modes of modern DRAMs and explain how the idea of adaptive history-based memory schedulers can be naturally extended to manage power and energy. DRAM power is reduced by using throttling approach which is used to reduce the DRAM activity by delaying the issuance of memory commands.

Brinda Ganesh *et al* [4] developed a alternative architecture called Fully Buffered Dual Inline Memory Module (FBDIMM) which replaces the conventional memory bus width narrow, high speed interface between memory controller and DIMM. The split bus architecture is used in FBDIMM provide system performance sensitive to the read and write traffic on the workload. The FBDIMM and DDRx system is similar and provide better performance characteristics at higher utilization making it a relatively inexpensive mechanism for scaling capacity at higher bandwidth requirements.

Bruno Diniz *et al* [5] present dynamic approaches for limiting the power consumption of the memories. The four techniques were proposed to limit the power consumption by adjusting the power states of the memory devices.

V. Delaluz *et al*. [6] reports that overall power consumption of the system is obtained by DRAM memory. So that, DRAM technology provides a low energy operating mode to achieve a potential benefits of mode control techniques. The researchers conduct an in-depth investigation of software and hardware techniques to avail of the DRAM mode control capabilities at a module granularity for energy savings.

Vinodh Cuppu *et al*. [7] present a simulation based performance study of representative group and it is evaluated in a small system organization. It covers Fast Page Mode, Extended Data Out, Synchronous, Enhanced Synchronous, Synchronous Link, Rambus, and Direct Rambus designs. The simulation based performance reveals many things that the DRAM technologies are attacking the memory bandwidth problem and the bus transmission speed will become a primary limiting factor.
Doug Burger *et al* [8] say that increased tolerance level of memory latency results in insufficient memory bandwidth. Due to that, calculate the pin bandwidth effectively, and then estimate the optimal effective pin bandwidth and measure these quantities by determining the amount by which both caches and minimal- traffic caches filter accesses to the lower levels of the memory Hierarchy.

3. PROPOSED SYSTEM

A. DRAM architecture

The DRAM architecture is designed efficiently by using different design techniques. In the existing process, the DRAM Architecture is designed using Mini-rank technique. In the mini-rank technique, the x64 rank is breaking into mini rank such as x32, x16, or even smaller mini ranks to perform the operation efficiently and to reduce the power consumption. The memory is placed in Dual Inline Memory Module (DIMM). Dual Inline memory Module consists of two mini-ranks. Each mini-rank consists of 32 bits in the memory. The memory in the DIMM consists of x64 bit is divided into two x32 bit, four x16 bit, even eight x8 bit configuration. According to the workload given to the processor, the memory controller will select which type of mini-rank configuration will be efficient. The main purpose of the memory controller is to monitor the bandwidth usage of each application and records the information in the hardware count register.

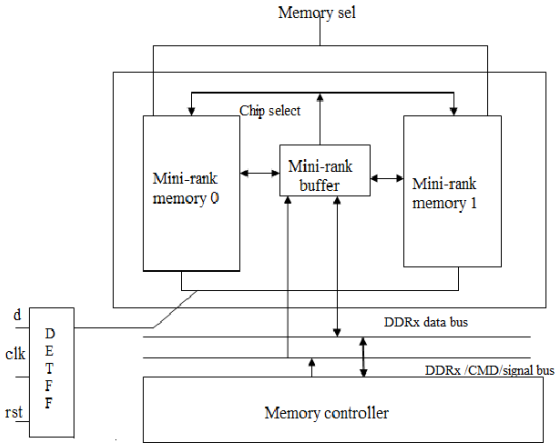

Figure-1. Dual inline memory module.

By using the application of memory controller, which type of configuration can be used is predicted. In the DIMM, mini-rank buffer (MRB) is used to transfer the data between the devices and buses. Then, the MRB used to transfer the command from memory controller to the devices. The mini-rank design technique is efficient but it occupies large number of area in the memory. Because the x32, x16 and x8 bit configuration are designed individually and consumes more space. In order to overcome that, these different configurations are implemented in the common mini-rank memory. The Figure-1 shows the dual inline memory module which consists of two common memory along with mini-rank buffer to transfer data and commands to the devices. The memory select line is introduced in the mini-rank memory. Depends upon the select line the x32, x16 or x8 bit configuration is selected in the common memory. This DRAM architecture will reduce the size of the memory and covers only small area.

B. Dual edge triggered flip-flop

Generally, the operation of the processor will start by giving the input to the clock signal. The clock signal will be in active state only at the positive or negative edge of the signal. If the positive edge is triggered, then the data will be processed only in the positive edge. If the negative edge is triggered, then the data will be processed only in the negative edge of the clock signal. The Single Edge Triggered Flip Flop (SETFF) is efficient in low power applications .But in the processor or controller, large number of operations were performed whereas single edge triggered flip flop is not efficient and the performance will be low, Because it consumes large number of clock signals, automatically frequency range will be increased. In order to overcome that, Dual Edge Triggered Flip Flop is implemented in the memory to improve the speed of the processor as well as to reduce the power consumption of the memory. The Figure-2 shows the Dual Edge Triggered Flip Flop which is designed using D-flip flop and gates. In the DETFF both positive and negative edge will be in active state. So that

the data will be transferred both in the positive and negative edge if the reset signal will be in inactive state. When the reset signal is active, no data will be processed.

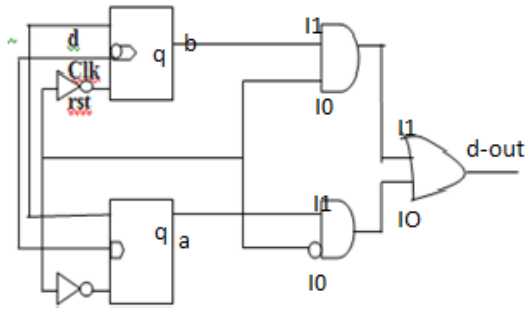

Figure-2. Dual edge triggered flip flop.

Therefore the clock cycles in the process will be reduced to half of the clock signal. For example, if the 32 bit data is transferred, it requires only 16 clock cycles instead of 32 clock cycles. It leads to reduction of clock cycles in the DRAM architecture.

4. EXPERIMENTAL RESULTS

A. Simulation output for x8 mini-rank configuration

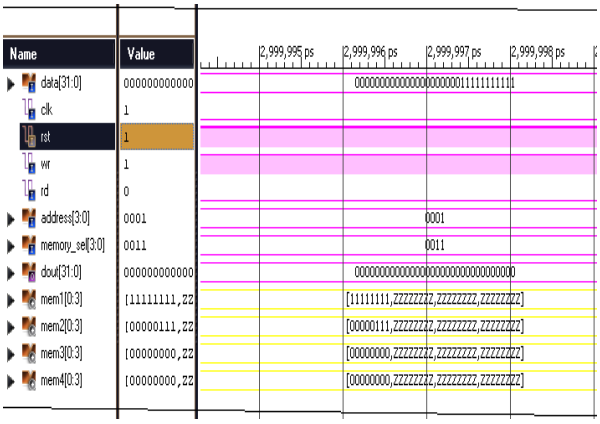

Figure-3. Write operation.

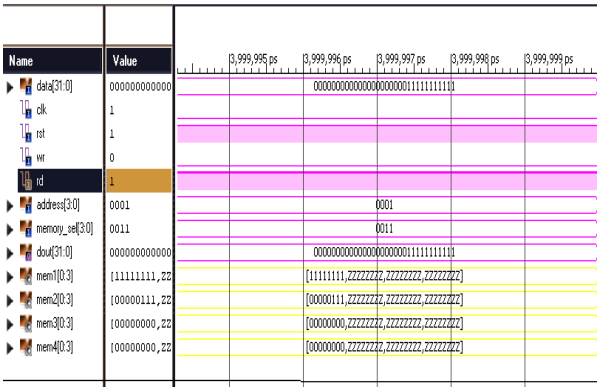

Figure-4. Read operation.

B. Simulation output for x16 bit mini-rank configuration

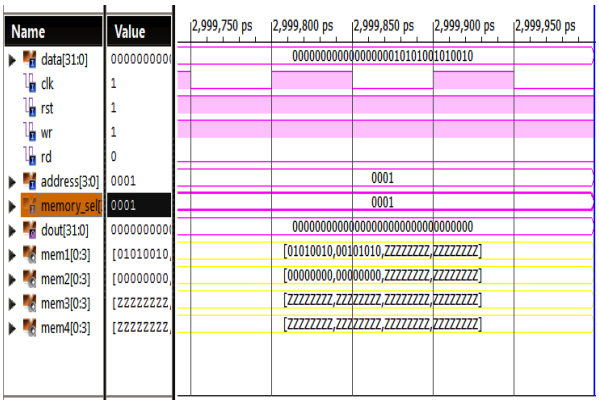

Figure-5. Write operation.

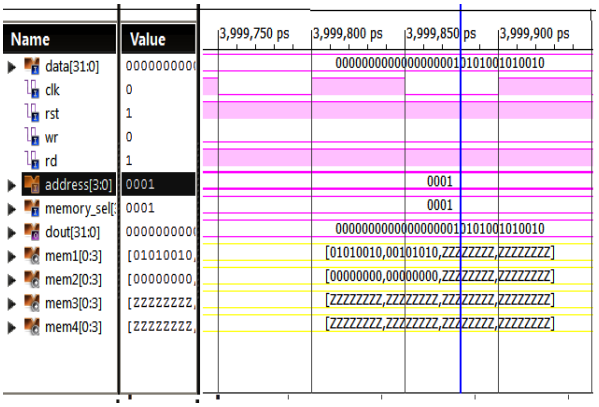

Figure-6. Read operation.

C. Simulation output for x32 bit mini-rank configuration

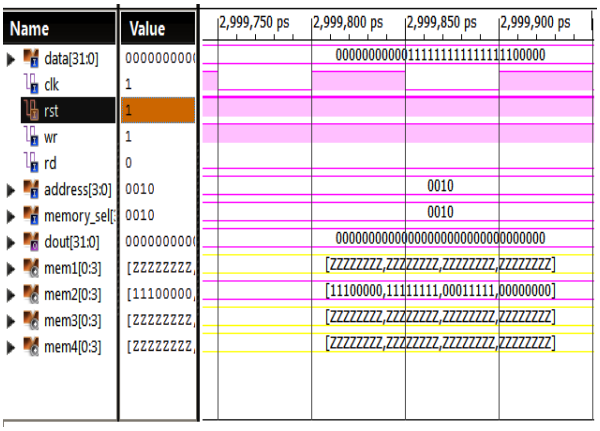

Figure-7. Write operation.

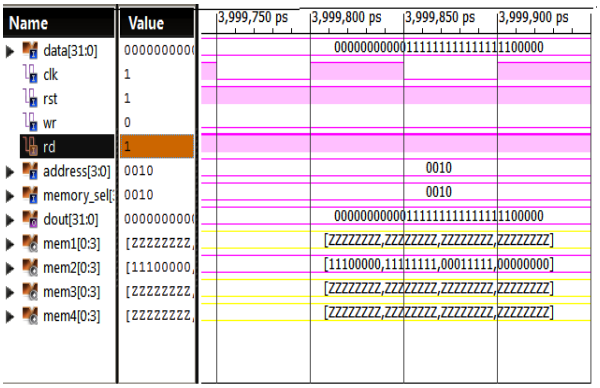

Figure-8. Read operation.

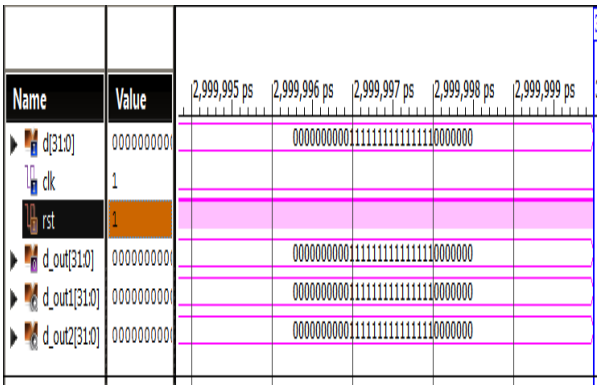

Figure-9. Dual edge triggered flip flop.

5. CONCLUSION AND FUTURE WORK

The structure of the DRAM architecture is designed using mini-rank design technique. The mini-rank design technique reduces the power consumption but it covers large area due to breaking ranks into mini-ranks such as x64 rank into x32, x16, or even x8 mini rank configuration. In order to reduce the area, all this different configurations are mixed together and designed in a common mini-rank memory and these different configurations were selected by the memory select line depends upon the workload recorded by the memory controller to predict which type of configuration is suitable for the current process by using previous results.

Thus the process will be enhanced by implementing DETFF in this DRAM architecture. The DETFF consists of D-flip flops and gates. It reduces the count of the clock cycles by activating both positive and negative edges of the signal and the frequency will be automatically reduced. Simultaneously, the power consumption of the memory will be reduced. Therefore the performance of the DRAM architecture will be increased using this DETFF and the newly designed mini-rank structure.

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