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VARIATION-TOLERANT SUB-THRESHOLD SRAM CELL DESIGN TECHNIQUE

Soumitra Pal, Malreddy Shekar Reddy and Aminul Islam
Birla Institute of Technology, Mesra Ranchi, Jharkhand, India
E-Mail: soumitra10028.13@bitmesra.ac.in

ABSTRACT

At present SRAM cell is under renovation stage. Researchers are trying to propose an SRAM cell that withstands the ever-increasing PVT (process, voltage and temperature) variations and supports low-voltage operation even under subthreshold regime. In this article, a 10T SRAM cell based on DSBB and DTMOS techniques is proposed. This cell is identical to conventional 10T (CON10T) SRAM cell except the body bias connections of the FETs used in the design. This cell is operated in subthreshold region varying from 400 mV to 200 mV. The proposed cell offers 2.64× higher read current and 1.36× tighter spread in read current. It takes 38.04% shorter time to sense a particular data available at the storage nodes with 50.58% improvement in its distribution. The proposed cell benefits 19.48% of write delay and 3.33× tighter spread in write delay compared with its conventional counterpart. It also offers 2× improvement in its write-ability and 2.67× increment in read current to leakage current ratio (I_{READ}/I_{LEAK}) with same RSNM (105 mV) and hold power (1.17 nW) @ 400 mV.

Keywords: SRAM, DSBB and DTMOS techniques, read current, read delay, read static noise margin (RSNM), write delay, write static noise margin (WSNM), hold power.

1. INTRODUCTION

The gradual increase in the usage of portable devices like wireless sensor node processor, implantable medical devices, mobile phones have made optimization of power consumption one of the major factors to be kept under consideration while conceptualizing the design element.

As estimated by ITRS (International technology road map for semiconductors) in its 2011 edition [1], SRAM cell occupies 90% of the total area of the chip. Therefore, to optimize the power consumption of the chip, decrement of the power consumption of an SRAM cell becomes inevitable. Operation of SRAM cell in sub-threshold region ($V_{DD}<V_t$) is one of the promising techniques to decrease the power consumption [2], [3]. This is because of the fact that power consumption (P) is proportional to square of the supply voltage (V_{DD}), mathematically $P \alpha V_{DD}^2$.

Operating a 6T SRAM cell in subthreshold region is more challenging because of its yield degradation. RSNM (read static noise margin) is major concern in subthreshold region. In conventional 6T SRAM cell both read stability and write ability cannot be improved simultaneously [4]. This is due to the fact that, to attain appropriate read stability, it requires smaller width of access transistor to keep the cell ratio (β_{ratio}) higher [5], whereas for appropriate write ability the width of access transistor should be larger, in order to keep the pull-up ratio (γ_{ratio}) lower [6]. To overcome this problem many different configurations of SRAM cells have been developed like single ended 8T and 10T [7]-[10], which improves read stability by providing the alternative read path which is different from the conventional 6T. However, these cells face the problem of decreased sense margin, as they are single ended [12]. This problem of sensing is eliminated by using differential SRAM cells. A further improvement in leakage current is observed in differential 8T (D8T) [11] and 10T (D10T) SRAM cells [12].

In this paper a fully differential 10T SRAM (UNCON10T) cell is proposed based on DTMOS (Dynamic Threshold MOS) and DSBB (Dynamically Swapped Body Bias) techniques. In the proposed cell the body bias connections of PFETs and NFETs of the cross-coupled inverters are connected to gnd (ground) and V_{DD} (supply voltage) respectively and body of other MOSFETs are connected to their respective gate. The performance of the proposed circuit is observed at different subthreshold voltages ranging from 400 mV to 200 mV and compared with the conventional 10T (CON10T) [12].

a) The proposed circuit (UNCON10T) displays considerable improvement in read delay, write delay and in their variabilities.
b) The read current is much larger compared with conventional 10T SRAM cell (CON10T).
c) The proposed UNCON10T shows drastic improvement in WSNM compared with its counterpart (CON10T).

All the observations, which are presented below, are obtained using HSPICE 16-nm PTM [13] with 5000 Monte Carlo simulations.

Rest of the paper is organized as follows. Section II presents brief discussion on DTMOS and DSBB techniques. A brief explanation of the proposed SRAM cell is presented in Section III. Section IV presents the results obtained in simulations. Finally, Section V concludes the paper.

2. DTMOS AND DSBB TECHNIQUES

In DTMOS technique the substrate and gate of a MOSFET are connected together. If the gate voltage is non-zero, the substrate-source and substrate-drain junctions of an NMOS are forward biased. This reduces

the threshold voltage, which in turn increases the drain current of the MOSFET. The equation provided below explains the reason behind the variations in the threshold voltage and thereby drain current.

$$V_t = V_{t0} + \gamma\left(\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}\right)$$

where V_{t0} is the threshold voltage at zero substrate bias; V_{SB} is the source to body bias; $2\phi_F$ is the surface potential; $\gamma = \left(\frac{t_{ox}}{\varepsilon_{ox}}\right)\sqrt{2q\varepsilon_{si}N_A}$, where t_{ox} is oxide thickness; ε_{ox} is permittivity of oxide, ε_{si} is the permittivity of silicon, N_A is the doping concentration; q is the charge of an electron.

DTMOS is robust against V_t fluctuation and temperature variation [14]. Moreover, when the front gate and the back gate are directly connected, the overall intrinsic capacitance reduces as the oxide capacitance of front gate and that of back gate appear in series combination [15].

The DSBB technique is unique and different from conventional SBB (swapped body bias) technique due to the fact that in the proposed DSBB technique, the body of NFET (PFET) is connected to V_{DD} (GND) only during accessing of the cell contrary to permanent connection in SBB. Due to dynamic connections in case of DSBB, the leakage current is improved as compared to that of in SBB model.

3. PROPOSED SRAM CELL

The proposed design is similar to the conventional 10T (CON10T) (Figure-1), except the body bias connections of drivers of cross-coupled inverters which are connected to write word line (WWL). The substrates of respective pull-up devices are connected to complementary write word line (WWLB). The substrates of the remaining transistors are connected to their respective gate, making them DTMOS. Because of this body biasing, the improvements in read delay, write delay and their variabilities are obtained (as discussed in the next section) at the cost of very minimum area overhead of the SRAM cell, which is due to the use of WWLB (Figures 2 and 3).

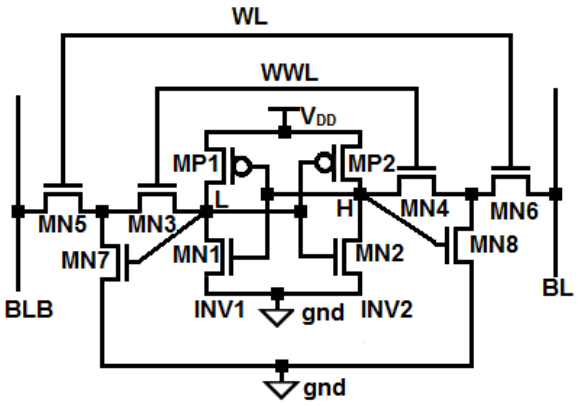

Figure-1. Conventional 10T (CON10T).

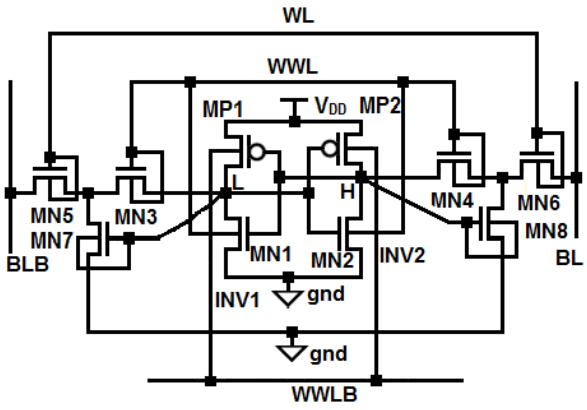

Figure-2. Proposed unconventional 10T (UNCON10T).

The important factor in the design of an SRAM memory cell is the sizing of FETs. These sizes of FETs are selected to obtain desired cell ratio [5] and pull-up ratio [6] for maintaining moderate RSNM and WSNM in conventional 6T SRAM cell. However, this is not the case for the proposed UNCON10T SRAM cell, as there is an alternative read path.

A fair comparison of the proposed design with its conventional counterpart is made by maintaining the same sizes of the respective FETs in both the designs. The width of the FETs used in the design (for 16-nm technology) are 16 nm for MP1/2, 24 nm for MN3/4/5/6 and 32 nm for MN1/2/7/8 and the length of all the FETs is 16 nm, the minimum value allowed in the 16-nm technology node.

4. SIMULATION RESULTS AND COMPARISON

The simulation results of conventional 10T (CON10T) and proposed unconventional 10T (UNCON10T) presented in this section are obtained using HSPICE 16-nm PTM [13] with 5000 Monte Carlo simulations.

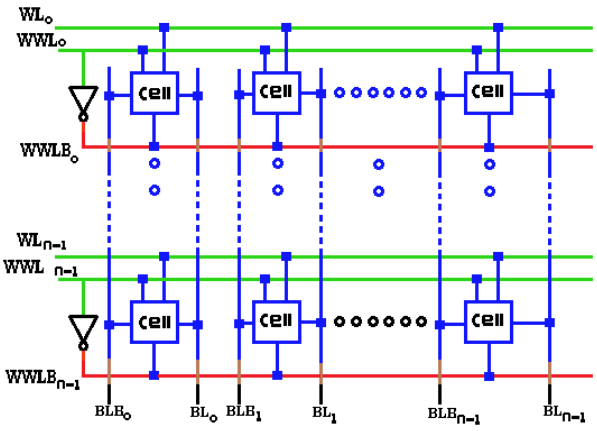

Figure-3. Architecture of the proposed design.

The Gaussian distribution with 3σ variation of 10% [1] is used in the parameters of channel length (L), channel doping concentration (NDEP), threshold voltages (V_{tp}, V_{tn}) and oxide thickness (t_{ox}).

A. Read current estimation

Read current (I_{READ}) is the current flowing through the read access transistor of SRAM cell during read operation. The current flow during read operation and its variability (ratio of standard deviation (σ) to its mean (μ)) are calculated and tabulated in Table-1. A significant improvement of I_{READ} is observed in UNCON10T compared to CON10T as evident from the Table-1 and the Figure-4. This is due to body biasing of the read buffer transistors (MN5/7 and MN6/8) in the proposed UNCON10T SRAM cell, which reduces the threshold voltage of the respective MOSFETs. This leads to higher I_{READ} during read operation. I_{READ} of CON10T and UNCON10T at a supply voltage of 400 mV are 769 nA and 2030 nA respectively. Therefore, an increment of 2.63× is observed in I_{READ}. The proposed cell also offers 1.36× narrower spread in I_{READ} compared to CON10T at the same voltage. The narrower spread in the variability of read current results in narrower spread of read delay (T_{RA}) in the proposed design.

Table-1. Read current and its variability.

Cell	V_{DD} (V)	σ of I_{READ} (nA)	μ of I_{READ} (nA)	Variability (σ/μ)
CON10T	0.40	306.0	0769.0	0.398
	0.35	128.0	0280.0	0.457
	0.30	044.0	0088.7	0.496
	0.25	012.8	0024.8	0.516
	0.20	003.2	0006.1	0.525
UNCON10T	0.40	595.0	2030.0	0.293
	0.35	293.0	0809.0	0.362
	0.30	108.0	0262.0	0.412
	0.25	031.6	0070.0	0.451
	0.20	007.3	0015.5	0.470

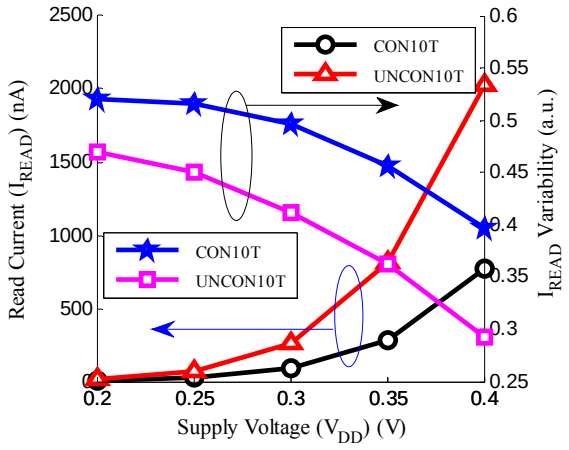

Figure-4. Read current and its variability Vs Supply Voltage (V_{DD}).

B. Read delay and its variability

During read operation of CON10T and UNCON10T, WL (word line) is kept high and WWL (write word line) is maintained at low. Therefore, transistors MN5 and MN6 conduct and MN3 and MN4 do not conduct. The bitlines BL and BLB are precharged to the supply voltage. One of the read driver transistors (MN7/8) conducts depending on the data (logic '1') stored at L/H (see Figures 1 and 2) which leads to discharge of either one of the bitlines (BL/BLB) through MN6/8 or MN5/7. The time taken (by BL/BLB) to drop by 50 mV from its precharged value after WL is triggered, is known as read access time (T_{RA}) or read delay of the SRAM cell [16].

Variability (ratio of standard deviation (σ) to the mean (μ)) along with the read access time of the proposed UNCON10T is estimated and compared with CON10T. The comparisons of read access time and its variability, between the CON10T and the proposed UNCON10T are provided in Figure-5 for subthreshold voltages varying from 400 mV to 200 mV.

The proposed circuit outperforms the CON10T as evident from the Figure-5. The reason behind this improvement is the decrement of threshold voltage of the concerned MOSFETs due to DTMOS technique resulting in higher read current and shorter read delay.

Figure-6 shows the distribution plots of UNCON10T and CON10T @ 400 mV. From this plot, it can be deduced that both the minimum value and the maximum value of proposed UNCON10T are shorter than that of CON10T, which signify that shorter time is needed to read the stored cell content. Both the distribution curves intersect at 1.35 ns. Based on the estimated data UNCON10T has 92.06% of its statistical samples shorter than 1.35 ns implying that shorter time is needed for read operation compared to CON10T, which has 87.5% of its statistical samples longer than 1.35 ns.

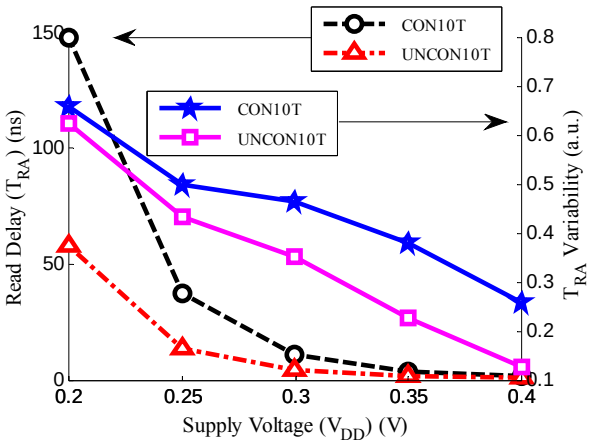

Figure-5. Read delay and its variability vs supply voltage (V_{DD}).

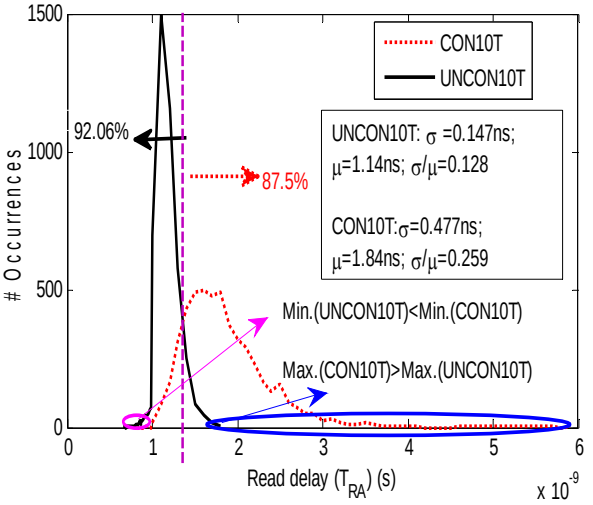

Figure-6. Read delay distribution of UNCON10T and CON10T.

C. Write delay and its variability

During write operation of CON10T and UNCON10T, both WWL and WL are enabled. Therefore, the access transistors MN3/4/5/6 conduct. Depending on data ("1" or "0") to be stored at storage nodes L/H, bitlines, BL/BLB are loaded with "1" or "0".

Write delay or write access time (T_{WA}) is the time taken by the node L/H (initially storing logic '0') to reach 90% of its supply voltage after WWL is triggered [16].

The comparison of write delay (T_{WA}) and variability (ratio of standard deviation (σ) to the mean value (μ) of T_{WA}) are presented in the Figure-7 with the voltages ranging from 400 mV to 200 mV in the subthreshold region.

Write access time and its variability is improved in the proposed cell (UNCON10T) compared to its counterpart CON10T as observed in Figure-7. The improvements in write delay and its narrow spread is obtained due to DTMOS and DSBB techniques at the cost of very less area overhead of WWLB.

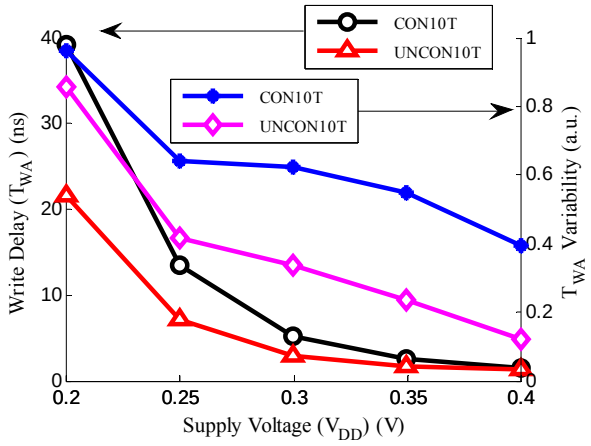

Figure-7. Write delay and its variability vs supply voltage (V_{DD}).

D. RSNM analysis

RSNM is the measure of stability of the SRAM cell during read operation. RSNM (Read static noise margin) is the minimum amount of noise voltage required at the node L/H to flip the cell content [17]. As SRAM cells are sensitive to noise during read operation, RSNM is an important design metric. Smaller the cell ratio (β_{ratio}) lesser the noise voltage required to flip the state of the SRAM cell in conventional 6T. However, this is not the case in the proposed UNCON10T and CON10T, as these cells are read decoupled.

The conceptual setup for measuring the RSNM of the proposed cell is sown in Figure-8 (a similar setup is used for conventional 10T). RSNM is estimated from the "butterfly curve" as shown in Figure-9. This "butterfly curve" is obtained from the read VTCs (voltage transfer characteristics). The VTCs of INV1 and INV2 are obtained by varying the voltages of N1 and N2 from 0 V to V_{DD}. A square with largest diagonal is inscribed in the smaller lobe of the "butterfly curve". The length of this square is the measure of RSNM of the SRAM cell. The "butterfly curve" has three distinct roots, which signifies the functionality of the SRAM cell as a bistable circuit [18].

From the Figure-9, it can be concluded that the RSNM of CON10T and proposed UNCON10T are equal because both the cells are read decoupled.

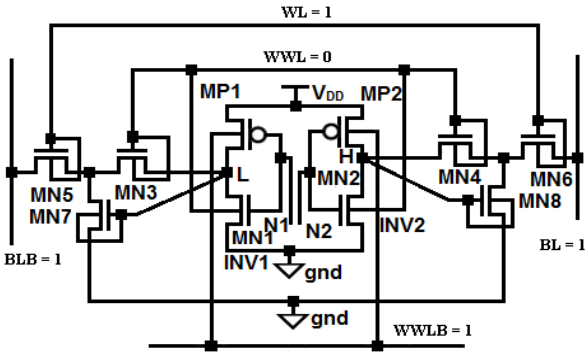

Figure-8. UNCON10T SRAM cell used in RSNM calculations.

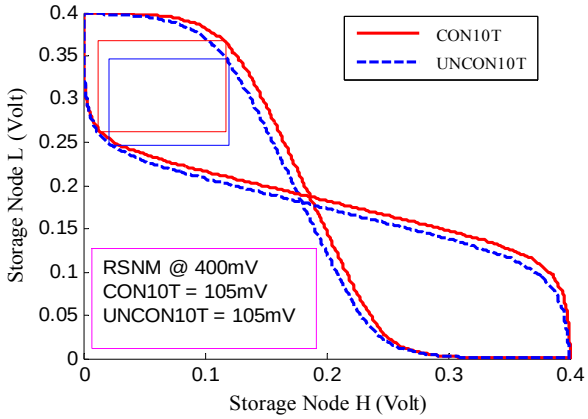

Figure-9. Static VTCs during read operation.

E. WSNM analysis

The ability of an SRAM cell to pull down the node storing "1" below the switching threshold voltage of the other inverter storing "0", owing to which the cell content of the inverter storing '0' gets flipped as desired, is analyzed through WSNM.

WSNM is calculated using the curve obtained from the combination of read VTC and Write VTC. A smallest square is embedded in the lower half of this curve. The side length of this square is the WSNM of the SRAM cell (see Figure-10) [18]-[19]. As observed in the plot (Figure-10) WSNM of UNCON10T (30 mV) is 2× larger than that of CON10T (15 mV) @ 400mV. This is because the body of the access transistors in the proposed circuit is connected to their gates of the respective FETs, thus decreasing the threshold voltage of the access transistors and hence increasing the write current flow through MN3/4/5/6. Therefore, write ability of the proposed UNCON10T is improved. Moreover, the read VTC and write VTC meet in a single point (Figure-10). This signifies that the SRAM cell can be operated in monostable mode [20].

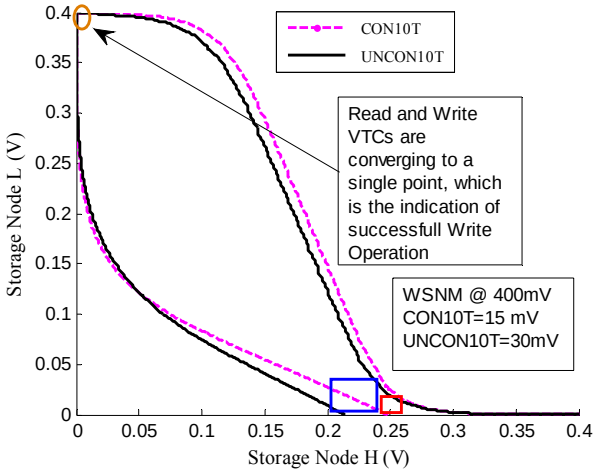

Figure-10. Static VTCs during read and write operation.

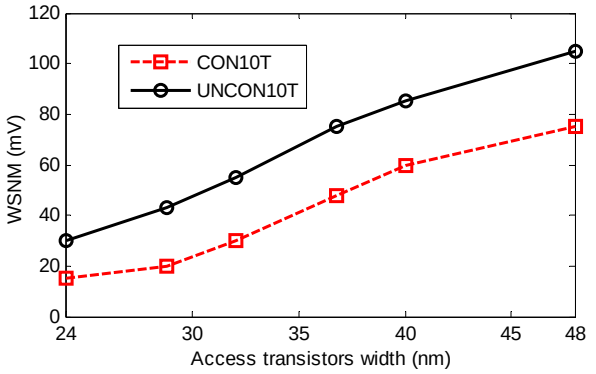

Figure-11. WSNM Vs Access transistors width.

To improve write-ability (WSNM), the widths of the access transistors (MN3/4/5/6) are upsized. Comparative results of WSNM versus width of access transistors are plotted in Figure-11. As evident from the plot, the WSNM of UNCON10T is higher than CON10T at all respective widths.

F. Hold power

Hold power is the important design metric, as the cells remain mostly in the hold mode (expect when the cell is accessed). During hold mode, WL and WWL are turned low. Therefore, WWLB is high, thus substrates of PFETs of the cross-coupled inverters are connected to V_{DD} and the substrates of NFETs are connected to GND. Hence, the proposed cell is identical to CON10T in hold mode. Thus, power dissipated in the hold mode of the proposed circuit is same as the CON10T.

Figure-12 shows the power dissipation plot (H_{POWER}) of UNCON10T and CON10T, the power dissipation is the same in both the cells as evident from the theoretical discussion and the plot.

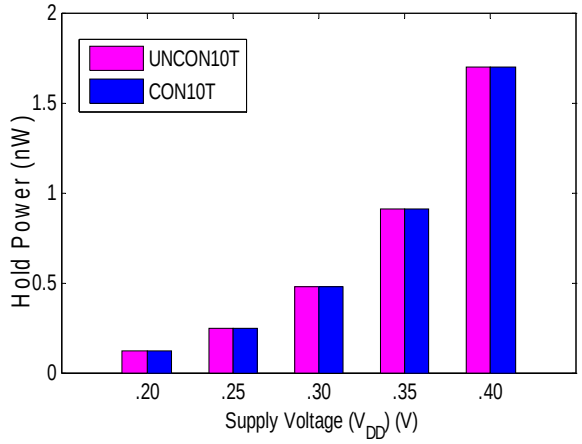

Figure-12. Hold power vs supply voltage (V_{DD}).

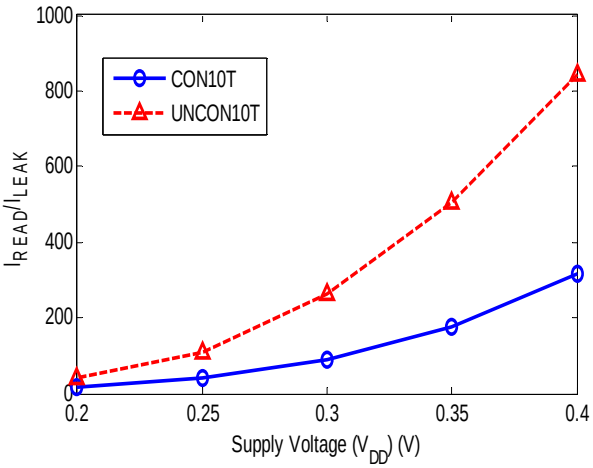

Figure-13. I_{READ}/I_{LEAK} vs supply voltage (V_{DD}).

G. Read current to leakage current ratio

Leakage current (I_{LEAK}) is the current flowing through the SRAM cell during hold mode. Therefore, leakage current is same in both CON10T and UNCON10T SRAM cells. As the I_{READ} of UNCON10T is higher than that of CON10T (see Table-1 and Figure-4), the I_{READ} to I_{LEAK} ratio is larger in the proposed cell compared to its counterpart. The ratio of I_{READ} to the I_{LEAK} of proposed SRAM cell and its conventional counterpart is shown in Figure-13. This improvement signifies that increased quantity of SRAM cells can be used in a column of the SRAM memory array without the problem of misread by the sense amplifier.

5. CONCLUSIONS

A 10T SRAM cell based on DSBB and DTMOS techniques is proposed in the subthreshold region. An improvement in read current, read delay, write delay are observed. It also shows narrower spread in read current, read delay and write delay. It also achieves higher WSNM and I_{READ} to I_{LEAK} ratio. The proposed SRAM cell therefore, is an attractive option for subthreshold operation.

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