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LOW POWER TERNARY SHIFT REGISTER USING CNTFETS

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ABSTRACT

In the last few decades, interest in multivalued logic has grown rapidly due to its potential advantages over binary logic for designing energy efficient digital systems. In this paper, a ternary D flip flop with preset and clear inputs is designed using Carbon Nanotube Field Effect Transistor based ternary logic gates. The chiralities of the carbon nanotubes (CNT) used for constructing CNTFET based ternary logic circuits are (19, 0), (13, 0) and (10, 0) of diameters 1.487nm, 0.783nm and 1.018nm with threshold voltages of 0.293V, 0.428V and 0.557V respectively. The designed ternary D flip flop is used as basic building gate for constructing serial in and serial out (SISO) shift registers with improved design and energy efficiency. Finally simulation results using Hspice simulator are reported to show that the proposed CNTFET ternary logic circuits consume significantly less power with considerable reductions in power delay product as compared to conventional binary logic circuits.

Keywords: chiralities, CNT, CNTFET, D flip flop, hspice, multivalued logic, power delay product, SISO shift register, ternary, threshold voltage.

INTRODUCTION

Multi-valued logic replaces the classical Boolean characterization of variables with either finitely or infinitely many values such as ternary logic or fuzzy logic [1-2], since it reduces the complexity of interconnects and chip area [3]. By employing ternary logic, serial and serial-parallel arithmetic operations can be carried out faster. In many cases, MVL logic has been combined with binary logic to enhance the performance of CMOS technologies [4]. Three kinds of MVL circuits are current-mode MVL, voltage-mode MVL and mixed-mode or hybrid mode MVL. Several current-mode MVL circuits have been fabricated which shows better performances compared to binary circuits [5]-[8]. But the power consumption of current mode MVL circuits is high due to their inherent nature of constant current flow during the operation. Voltage mode circuits consume a large current only during the logic level switching, thus offers less power consumption.

CNTFET replaces conventional devices for low power and high performance design, due to ballistic transport and low off current properties, [9 - 11]. As the threshold voltage of the CNTFET is determined by the diameter of the CNT, a multi-threshold design can be achieved by employing CNTs with different diameters. Recently, efforts have been done for designing combinational circuits using multi-threshold CNTFETs [14]. In this paper, the ternary logic design based on multi-threshold CNTFETs is assessed by designing ternary SISO shift register and compared with binary logic design.

This paper is organized as follows: section 2 Introduces ternary logic operation. Section 3 deals with the fundamental ideas of CNTFET. Circuit level implementation of combinational ternary logic circuits such as ternary D flip flop, ternary SISO shift register etc have been discussed in section 4, simulation results in section 5 and comparison with conventional circuits in section 6. Finally in section 7, the research paper has been concluded with the work undertaken in this research work and the scope for improvement of the circuit level transistor models.

Ternary logic operation

In order to maintain the Moore's exponential growth, the IC industry must solve many problems, importantly interconnection problem, both on-chip and between chips. The reason being, the silicon area used for interconnections may be greater than that used for the active logic elements [13-15]. One of the best solutions for these interconnection problems is the use of circuits with more than two levels. This paper brings the very best answer for the significant question that,' whether it is possible to design multi valued ICs with performance better than or equivalent to the performance of the corresponding two-valued ICs?'

If a third value is introduced to the binary logic function, the resultant is the ternary logic function. Let 0, 1 and 2 be the ternary values to represent false, undefined and true conditions respectively. Any ternary function f(x) of n variable (X_1, X_2,…X_n) is defined as a logic function that maps $\{0,1,2\}^n$ to $\{0,1,2\}$. The fundamental operations of ternary logic can be defined as,

$$\begin{aligned} X_i + X_j &= \max\{X_i, X_j\} \\ X_i \bullet X_j &= \min\{X_i, X_j\} \\ \overline{X_i} &= 2 - X_i \end{aligned} \quad (1)$$

The basic ternary logic gates are designed according to the convention defined by equation (1).

Carbon Nanotube field effect transistor

Carbon nanotube field effect transistors consist of semiconducting Carbon nanotubes, which is acting as conducting, channel, that bridges the source and drain contacts. Based on the operation of the device, CNTFET can be classified as Schottky barrier (SB) CNTFET or MOSFET like CNTFET. In the case of SB CNTFET the

majority carriers tunnelling through the Schottky barriers at the end contacts decide the conductivity of the device. As a result, the on current and device performance of SB CNTFET is determined by the contact resistance of source and drain contacts, instead of the channel conductance. Schottky barrier CNTFET exhibits ambipolar transport behaviour and by choosing the appropriate work function of source/drain contacts the polarity and the bias point of the device can be adjusted. Unlike SB-CNTFET, MOSFET like CNTFET exhibits unipolar behaviour and the conductivity of the device is modulated by the gate-source bias. Though the SB CNTFET produces good dc current with the self aligned structure, its ac performance is very poor due to the arrangement of gate electrode closer to the source/drain metal. Also the ambipolar behaviour of SB CNTFET not best suits the complimentary logic design. By considering both the fabrication feasibility and excellent device performance, MOSFET like CNTFET has been used for constructing ternary CNTFET logic family. The diameter of the CNT can be calculated as, $D_{CNT} = \frac{\sqrt{3}a_o}{\pi}\sqrt{n_1^2 + n_1 n_2 + n_2^2}$ where a_o = 0.144 nm is the inter-atomic distance and the threshold voltage of the intrinsic CNT is given by, $V_{th} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}}$ where a=2.49Å is the carbon to carbon atomic distance, V_π = 3.033eV is the carbon π-π bond energy in the tight binding model and e is the unit electron charge. Thus, the threshold voltage of the CNT is inversely proportional to the diameter of the CNT in turn the chiral vector. In this paper, the chiralities of the CNTs used for modeling of CNTFETs are (19, 0), (13, 0) and (10,0) with diameters 1.487 nm, 0.783 nm and 1.018 nm respectively.

Circuit level implementation of ternary logic

A compact SPICE model including non-idealities is used for simulations which has been designed for unipolar, MOSFET-like CNTFET based circuits, also considers Schottky Barrier Effects, including CNT, CNT Charge Screening Effects, Source/Drain, and Gate resistances and capacitances. HSPICE simulator has been used to simulate the proposed ternary-logic based sequential circuits. The threshold voltages of CNTFETs used in the circuits are shown in Table-1.

Table-1. Threshold voltages of CNT with different chiralities.

Chirality (n_1, n_2)	Diameter (nm)	Threshold voltage (V)
(19,0)	1.487	0.293
(10,0)	0.783	0.557
(13,0)	1.018	0.428

Ternary NAND

A complementary CNTFET network can be used for ternary logic circuits design for achieving good performance and lower power consumption, and also to avoid the use of large resistors in the circuits which may lead to high power dissipation. Ultimately, size and area can be reduced by avoiding the large resistors. The most fundamental building block for the designing of sequential circuit is TNAND. The basic function of TNAND gate is defined as

$$Y_{NAND} = \overline{Min\{X_1, X_2\}}$$

The circuit realization of TNAND and TNOR gates requires 5 n-CNTFETs and 5 p-CNTFETs as shown in Figure 6.4(a) and Figure-6.4(b). The chirality of the CNT used for transistors T_1, T_2, T_5, T_6 is (19, 0), for T3, T_4 is (13, 0) and for T_7, T_8, T_9, T_{10} is (10, 0). The diameter of CNT used for T_1, T_2, T_5, T_6 is 1.487, for T_3, T_4 is 1.018 and for T_7, T_8, T_9, T_{10} is 0.783. The threshold voltage for T_1, T_2, T_5, T_6 is 0.293V, for T_3, T_4 is 0.428V and for T_7, T_8, T_9, T_{10} is 0.557V. Input A is given to the gate terminal of CNTFETs T_2, T_6, T_7 and T_8 and input B is given to the gate terminal of CNTFETs T_1, T_5, T_9 and T_{10}. The truth table for TNAND gate is given in Table-2.

Table-2. Truth table for TNAND gate.

A	B	Y_{NAND}
0	0	2
0	1	2
0	2	2
1	0	2
1	1	1
1	2	1
2	0	2
2	1	1
2	2	0

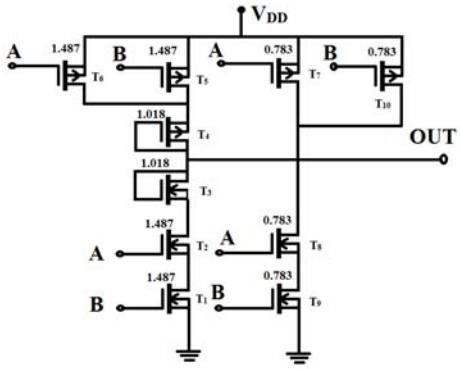

Figure-1. Structure of Ternary NAND gate.

Ternary D flip flop with binary clock

A similar structure of flip flops used in binary is applied for constructing ternary D flip flop by replacing all the binary logic gates with ternary logic gates constructed using CNTFETs.

The structure of ternary D flip flop is shown in Figure-2 and truth table in Table-3. The designed D flip flops can be used in many applications such as shift registers, frequency dividers, counters etc. In this paper, it is used to design shift registers. The data supplied to the D flip flop is ternary input data whereas the clock input is binary. When the clock input is high, the D flip flop reads the input value and transmits the input value to the output. The designed ternary flip flop is able to transmit all three logic levels i.e. 0, 1 and 2. When the clock input is low, the D flip flop retains its previous state. The performance of the flip-flop is verified using Hspice simulator. The designed D flip flops can be used in many applications such as Shift registers, frequency dividers, counters etc. In this paper, it is used to design shift registers.

Table-3. Truth table of ternary D flip flop with binary clock.

CLK	Data	Q	Q_{prev}
2	0	0	X
2	1	1	X
2	2	2	X
0	X	Q_{prev}	-

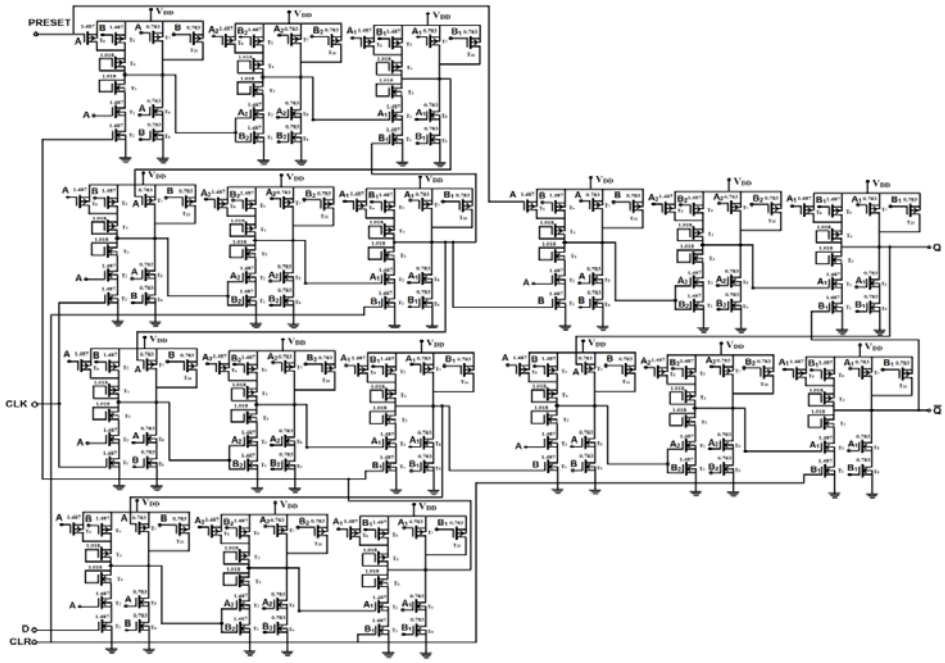

Figure-2. Structure of ternary D flip flop.

Ternary D flip flop with ternary clock

The structure of ternary D flip flop with ternary clock is similar to Figure-2. For the clock input of logic 0 and logic 2, the output behavior of the ternary D flip flop with ternary clock input is same as the behavior of binary clock input. For the intermediate value (logic 1), the value of Q output depends on data input as shown in Table-4.

Table-4. Truth table of ternary D flip flop with ternary clock.

CLK	Data	Q	Q_{prev}
2	0	0	X
2	1	1	X
2	2	2	X
1	0	0	0
		1	1,2
1	1	1	X
1	2	1	0,1
		2	2
0	X	Q_{prev}	-

Binary serial in serial out (SISO) shift register

A shift register is a cascade of flip flops that share the same clock signals. The data is stored as a one dimensional bit array and the shifting of a bit is enabled by the transition of the clock pulse. The output of the register will be the output of any one of the flip flop and the output of the last flip flop is connected to the data input of the next one in the sequence. This results in a circuit that shifts in the data present in its input and shifts out the last bit in the array by one position.

Figure-3 shows the basic four bit CNTFET serial-in serial-out shift register implemented using four CNTFET D flip flops. The circuit of D flip flop functions as follows. A reset applied to the 'CLR' input of all the flip flops resets their Q outputs to 0s. The flip flops shown respond to the transition of the clock pulses from low to high.

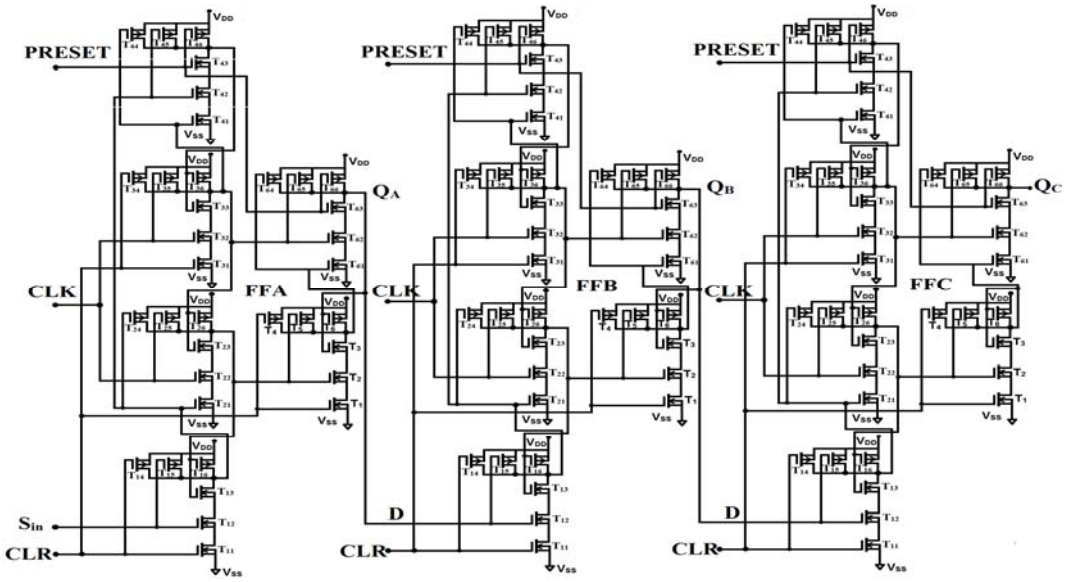

Figure-3. Structure of SISO shift register.

In general, in a three bit shift register of the type shown in Figure-3, a data bit present at the data input terminal at the time of the n^{th} clock transition reaches the Q_C output at the end of the $(n+3)^{th}$ clock transition. During the fourth and subsequent clock transitions, data bits continue to shift to the right and at the end of the sixth clock transition the shift register is again reset to all 0s. Thus, in a three bit serial-in serial-out shift register, it takes three clock cycles to load the data bits and another three cycles to read the data bits out of the register.

Ternary SISO shift register

In digital electronic circuits, a shift register is a cascade of flip flops, sharing the same clock, which has the output of anyone but the last flip flop connected to the "data" input of the next one in the chain, resulting in a circuit that shifts by one position the one dimensional "bit array" stored in it, shifting in the data present at its input and shifting out the last bit in the array, when enabled to do so by a transition of the clock input.

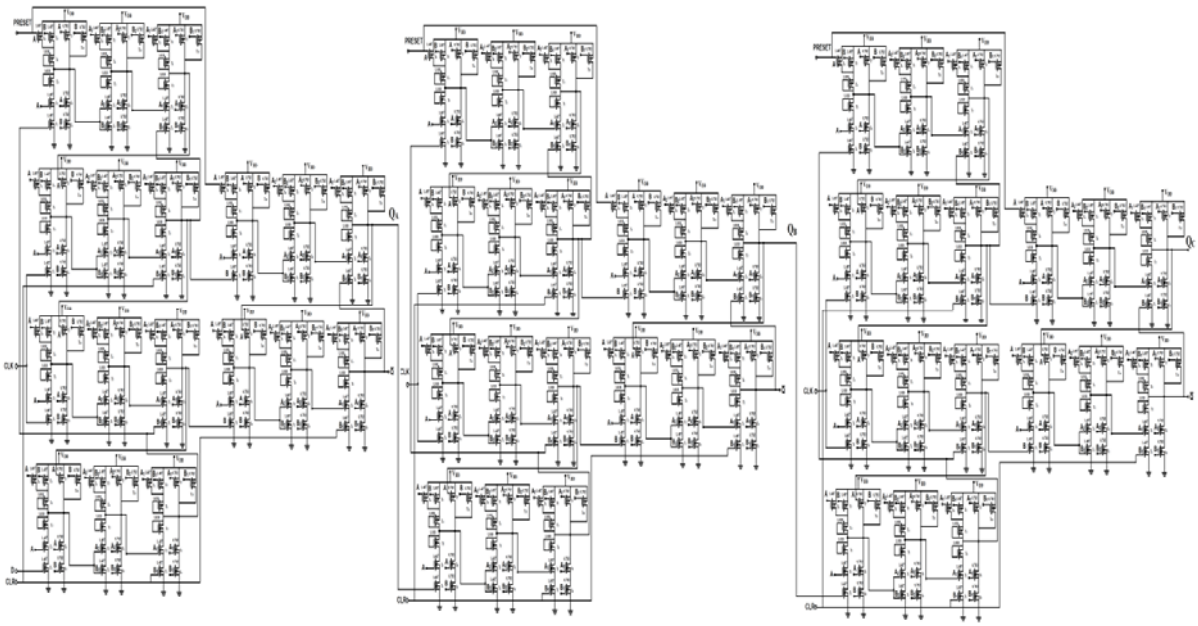

Figure-4. Structure of ternary SISO shift register.

Figure-4 shows the basic three bit ternary serial-in serial-out shift register implemented using ternary D flip flops. The circuit functions as follows. A reset applied to the 'clr' input of all the flip flops resets their Q outputs to 0s.

During the first clock transition, the Q_A output goes from logic '0' to logic '1'. The outputs of the other two flip flops remain in the logic '0' state as their D inputs was in the logic '0' state at the time of clock transition. During the second clock transition, the Q_A output goes from logic '1' to logic '2' and the Q_B output goes from logic '0' to logic '1', again in accordance with the logic status of the D inputs at the time of relevant clock transition. During the third clock transition, the Q_A output goes from logic '2' to logic'0 ', the Q_B output goes from logic '1' to logic '2' and the Q_C output goes from logic '0' to logic '1'. Thus, we have seen that a logic '2' that was present at the data input prior to the occurrence of the second clock transition has reached the Q_B output at the end of fourth clock transitions. This bit will reach the Q_C output at the end of sixth clock transitions. In general, in a three bit ternary shift register of the type shown in Figure 4, a data bit present at the data input terminal at the time of the nth clock transition reaches the Q_C output at the end of the $(n+6)^{th}$ clock transition.

SIMULATION RESULTS AND DISCUSSION

The behavior of the circuits are analysed by implementing the designed circuits in Hspice.

Figure-5 shows the behaviour of 2-input ternary TNAND gate from which the proper functioning of the circuits for various input variables can be observed. The average delay and average power consumed by the ternary TNAND are $7.47*10^{-12}$s and $1.95*10^{-7}$W respectively. Thus the power delay product is $1.46*10^{-18}$J. The proposed design achieves more than 300 times improvement over the design proposed by Subhajit Das (2011) (PDP = $4.74*10^{-16}$ J).

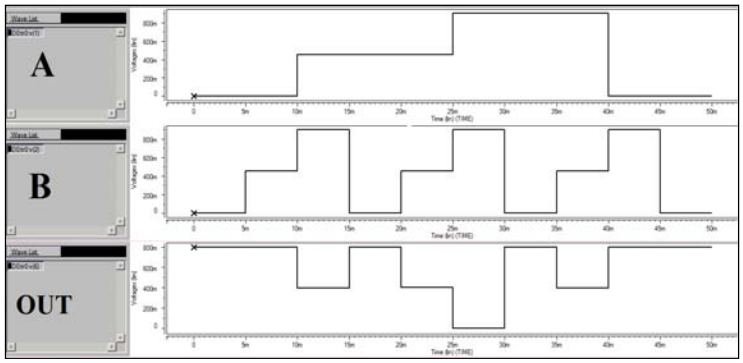

Figure-5. Transient response of Ternary NAND gate.

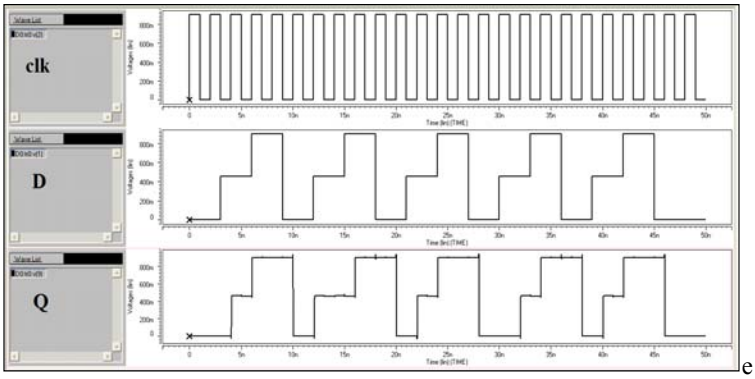

Figure-6. Behavior of ternary D flip flop with binary clock.

Figure-6 shows the behavior of D flip flop with binary clock and Figure-7 shows the behavior of D flip flop with ternary clock. The power delay product of the proposed design is improved by 3 times than binary design.

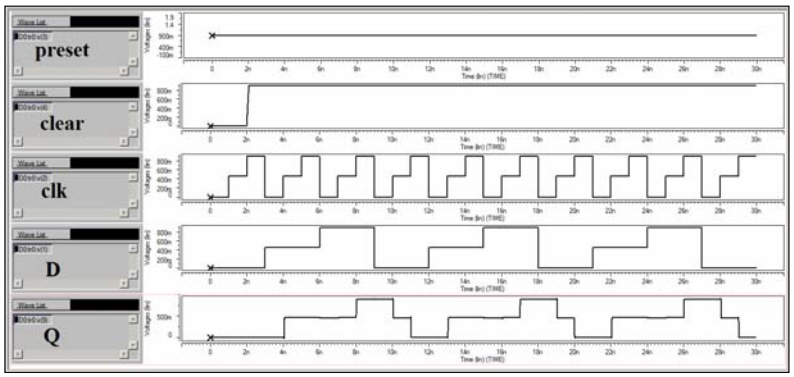

Figure-7. Behavior of ternary D flip flop with ternary clock.

The waveforms shown in Figure-8 include the clock pulse train (clk), the data (S_{in}) to be loaded onto the shift register and the Q (Q_A, Q_B, and Q_C) outputs of different flip flops (FFA, FFB, and FFC). During the first clock transition, the Q_A output goes from logic '0' to logic '1'. The outputs of the other two flip flops remain in logic '0' states as their D inputs were in the logic '0' state at the time of clock transition. During the second clock transition, the Q_A output remains at logic '1' since its D input is again at logic '1' and the Q_B output goes from logic '0' to logic '1', again in accordance with the logic status of the D inputs at the time of relevant clock transition. Thus, we have seen that a logic '1' that was present at the data input prior to the occurrence of the first clock transition has reached the Q_B output at the end of two clock transitions. This bit will reach the Q_C output at the end of third clock transitions.

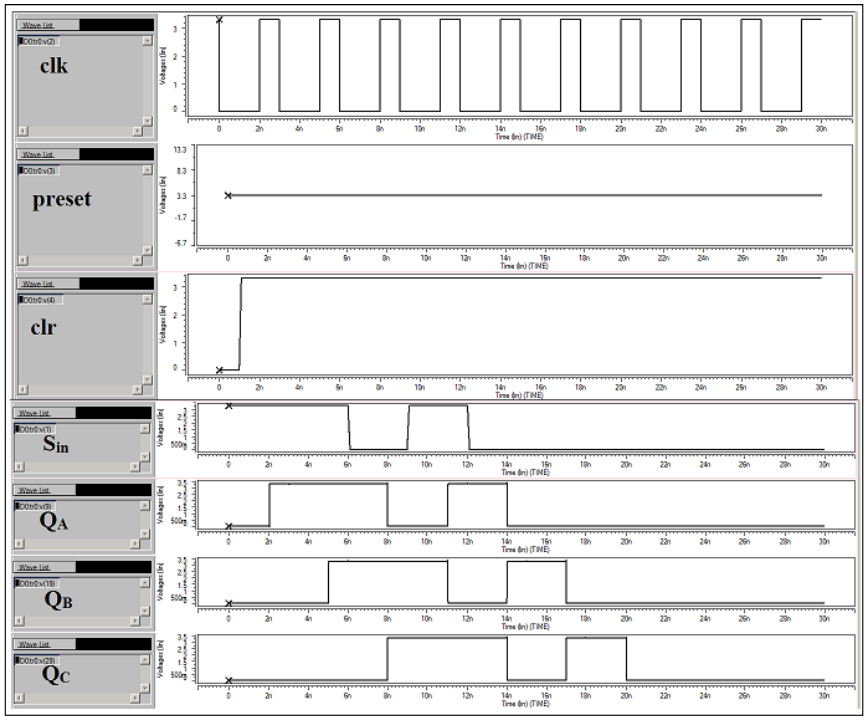

Figure-8. Behavior of SISO shift register.

The waveforms shown in Figure-9 include the clock pulse train, the waveform representing the data to be loaded onto the shift register and the Q outputs of different flip flops. The flip flops shown respond to the LOW to HIGH transition of the clock pulses.

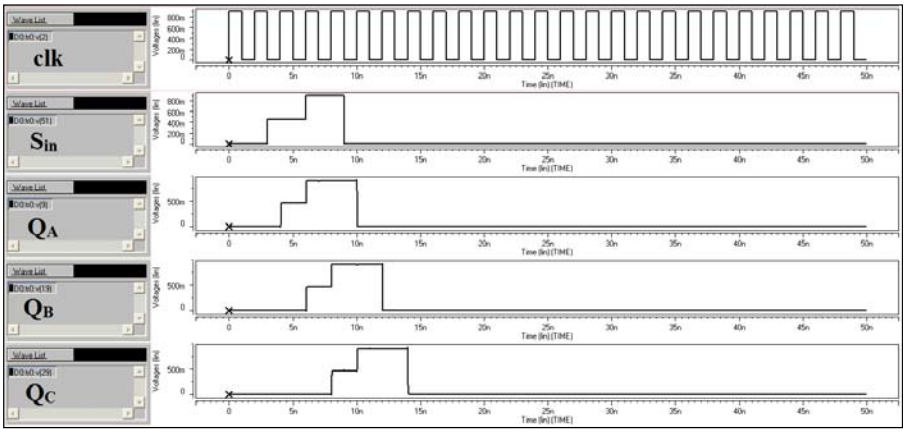

Figure-9. Behavior of SISO shift register.

Comparison of Binary-logic and Ternary-logic

Table-5 shows the comparison results of binary and ternary logic circuits. The average delay of the binary D flip flop is 4.9854 $*10^{-11}$ S and average power consumed is 6.172$*10^{-6}$ W. Therefore the power delay product is 3.0769$*10^{-16}$ J. The average delay of the binary SISO shift register is 5.134 $*10^{-11}$ S and average power consumed is 7.045 $*10^{-6}$ W. Therefore the power delay product is 3.6169$*10^{-16}$ J. The average delay of the ternary D flip flop is 3.0378$*10^{-11}$ S and average power consumed is 4.8492 $*10^{-6}$ W. Therefore the power delay product is 1.473 $*10^{-16}$ J. The average delay of the ternary SISO shift register is 3.9773 $*10^{-11}$ S and average power consumed is 5.2869 $*10^{-6}$ W. Therefore the power delay product is 2.1027$*10^{-16}$ J. Figure-10 and Figure-11 shows that the proposed ternary logic design is faster and consumes less power compared to binary logic family.

Table-5. Comparison of binary and ternary logic circuits.

Combinational circuit	Binary logic			Ternary logic		
	Delay (s)	**Average power** (W)	**PDP** (J)	**Delay** (s)	**Average power** (W)	**PDP** (J)
D Flip Flop	$4.9854 *10^{-11}$	$6.172 *10^{-6}$	$3.0769*10^{-16}$	$3.0378 *10^{-11}$	$4.8492 *10^{-6}$	$1.473*10^{-16}$
SISO shift register	$5.134*10^{-11}$	$7.045 *10^{-6}$	$3.6169*10^{-16}$	$3.9773 *10^{-11}$	$5.2869 *10^{-6}$	$2.1027*10^{-16}$

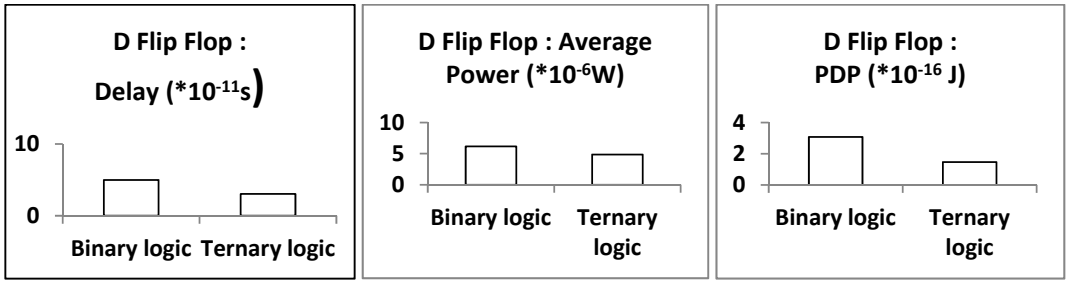

Figure-10. Comparison of binary and ternary D flip flop.

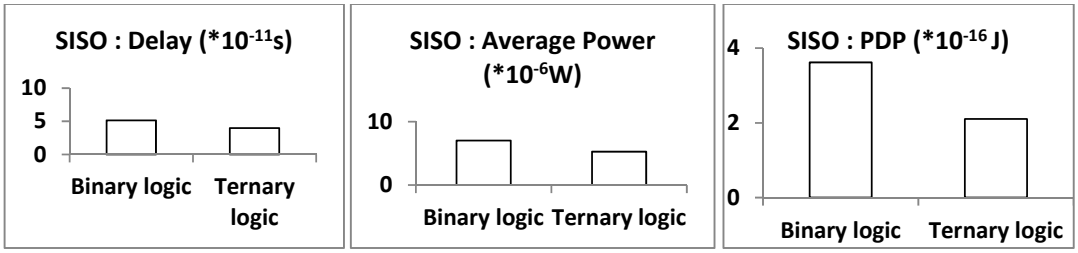

Figure-11. Comparison of binary and ternary shift register.

CONCLUSIONS

The prospects of applying ternary logic in computation have been discussed in this paper. Multi-threshold CNTFETs have been used for realizing ternary circuits such as clocked D flip flop, Shift registers etc. All simulations have been performed in HSPICE and the simulated results validated the correct operation of the realized circuits. Comparison made between binary and ternary logic showed that the circuits designed using ternary logic is predicted to be faster than classical binary circuits and works at even lower power.

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