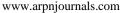
**ARPN** Journal of Engineering and Applied Sciences

© 2006-2015 Asian Research Publishing Network (ARPN). All rights reserved



# SIMULATION AND FAULT DIAGNOSIS OF POSITIVE OUTPUT ELEMENTARY SUPER LIFT LUO CONVERTER

B. Balaji and J. Barnabas Paul Glady

Department of Electrical and Electronics Engineering, Sathyabama University, Chennai, India E-Mail: balaji.bc91@gmail.com

### ABSTRACT

Fault Diagnosis in a DC-DC converter is very important to prevent the converter from the damage. The aim of the paper is to diagnosis the fault and to prevent the converter from the damage. This Paper deals with design, modeling and simulation of open and short circuit switch fault analysis using MAT Lab Simulink. The converter used here is a Positive Output elementary Super Lift LUO Converter (POESLLC). Open Circuit and Short Circuit Switch faults are created, and cleared using a closed loop control and corresponding waveforms are studied. The Simulation results are compared with theoretical results. A simulink model is developed and it is successfully used for fault diagnosis.

Keywords: positive output elementary super lift LUO converter (POESLLC), short circuit fault, open circuit fault, ciruit breaker.

# 1. INTRODUCTION

Nowadays DC-DC converters are more widely used in all types of applications such as drives, electric vehicles, renewable energy power systems etc. Therefore it is necessary to have reliable DC-DC converter. The two most important elements in DC-DC converters are semiconductors and aluminum electrolytic capacitor. In the literature it is said that more than 50% of maloperations occur in converter is due to electrolytic capacitor and 35% of mal-operations in converters are due to semiconductor switches. Therefore the DC-DC converter should be build with a fault tolerant capability, So that the operation of the system is not affected.

The fault tolerant system has to perform three operations. They are fault detection, fault identification and remedial actions. In this paper fault identification which is otherwise called fault diagnosis is performed in basic LUO [4] converter configuration.

In literature several papers have reported the fault detection for power electronic converter. The faster diagnosis of switch fault in the converter is studied from [1]. The faults in the converter due to aluminium electrolytic capacitor and semiconductor devices are reported in [2, 16]. The control of positive output elementary super lift LUO converter by PI is reported in [3]. Fault detection in multilevel converter is reported in [5].

In matrix converter the open circuit fault detection is reported in [6, 7, 13]. The open circuit fault in the converter in Induction motor drives is reported in [8][14]. The diagnosis of fault by using FPGA is reported [9][15]. In [11] kalman filter is employed in ordinary DC-DC boost converter. In [10] fault detection was done in grid connected photovoltaic system. The open circuit fault diagnosis in a converter is reported in [12][17].

In this paper the switch fault in the DC-DC POESLLC converter is diagnosed during the operation and faulty section is isolated in POESLLC. The circuit operation and its analysis were done in section II. The simulation was presented in section III. The conclusion is presented in section IV.

#### 2. CIRCUIT OPERATION

LUO Converter circuit is shown in Figure-1 which performs boost operation. The LUO Converters is preferred due to its high voltage gain, less ripple content, high power density.

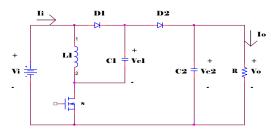


Figure-1. Circuit diagram of POESLL.

The POESLC Circuit Consists of Supply Voltage , two free wheeling diodes D1, D2 Inductance L, Switch S, the switch used is MOSFET and the Load (resistive).

# Mode 1

The equivalent circuit of POESLLC in Mode 1 is shown in Figure-2. In this mode the switch conducts (i.e) closed. The diode D1 is forward biased and the diode D2 is reverse biased. In this mode input is connected to the capacitor C and inductor L the capacitor, inductor and source voltage are parallel to each other. The capacitor gets charged to the input voltage and the current in the inductor is increases in this mode.

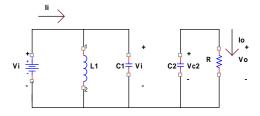


Figure-2. Equivalent Circuit of POESLLC in Mode 1.

©2006-2015 Asian Research Publishing Network (ARPN). All rights reserved.

### www.arpnjournals.com

A

Applying Kirchoff's current law in a circuit

$$V_{i} = V_{L1} = V_{C1}$$

$$I_{i} = I_{L1} + I_{C1}$$

$$I_{C2} = I_{o}$$
(1)

The inductor voltage is given by,

$$V_{L1} = L_1 \frac{di_{L1}}{dt} \tag{2}$$

But  $V_L = V_i$ 

$$V_{i} = L_{1} \frac{I_{2} - I_{1}}{t_{1}}$$
(3)

The time taken for mode 1 is given by,

$$t_1 = L \frac{\Delta I}{V_i} \tag{4}$$

The inductor ripple content in mode 1 is given by,

$$\Delta I = \frac{t_1 V_i}{L} \tag{5}$$

The output voltage at the end of mode 1 Is,

$$V_{C2} = V_O = I_O R_O \tag{6}$$

Mode 2

The equivalent circuit of POESLLC in Mode 2 is shown in Figure-3. In this mode the switch S is in OFF Condition (i.e) opened and here the diode D1 is reverse biased and diode D2 is forward biased. In this mode the source voltage, inductor and capacitor C1 are in series with capacitor C2 as shown in Figure-3.

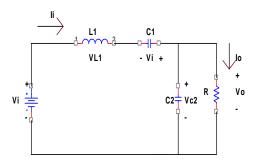


Figure-3. Equivalent circuit of POESLLC in Mode 2.

Applying Kirchoff's current law in a circuit,

$$I_{i} = I_{L1} = I_{C1}$$

$$I_{C1} = I_{C2} + I_{O}$$

$$V_{i} + V_{L1} + V_{C1} = V_{C2}$$
(7)

Assuming 
$$V_{C1} = V_i$$

$$2V_i + V_{L1} = V_{C2}$$
(8)

The inductor voltage is given by,

$$V_{L1} = L_1 \frac{di_{L1}}{dt} \tag{9}$$

Since in mode 2, the inductor releases the stored energy,

$$V_{L1} = -L_1 \frac{\Delta I}{t_2} \tag{10}$$

The time taken for mode 2,

$$t_2 = \frac{L_1 \Delta I}{2V_i - V_{C2}} \tag{11}$$

The inductor ripple content during mode 2

$$\Delta I = \frac{t_2 (2V_i - V_{C2})}{L_1}$$
(12)

The capacitor voltage of LUO converter is,

$$V_{C2} = 2V_i + \frac{D}{1 - D}V_i$$
(13)

$$V_{C2} = V_O \tag{14}$$

The output voltage of converter is,

$$V_o = 2V_i + \frac{D}{1 - D}V_i \tag{15}$$

The time period is given by,

$$T = L_1 \Delta I \left[ \frac{3V_i - V_{C2}}{2V_i^2 - V_{C2}V_i} \right]$$
(16)

Total inductor ripple is given by,

$$\Delta I = \frac{T}{L_1} \left[ \frac{2V_i^2 - V_{C2}V_i}{3V_i - V_{C2}} \right]$$
(17)

The Capacitor ripple is given by,

$$\Delta V_C = \frac{I_O}{CF} \left[ \frac{V_O - 2V_i}{V_O - V_i} \right]$$
(18)

#### 3. SIMULATION

The LUO Converter is simulated using mat lab simulink. The simulation parameter is shown in Table-1.

(8)

© 2006-2015 Asian Research Publishing Network (ARPN). All rights reserved.

#### www.arpnjournals.com

Name	Symbol	Value
Input Voltage	Vi	14 V
Output Voltage	Vo	42 V
Inductors	L	11 mH
Capacitors	C1,C2	1000 mF,3500 mF
Duty Cycle	D	0.6
Load Resistance	R	5 Ohms
Output Current	Io	8.3 amps

 Table-1. Simulation parameters.

The simulated Circuit diagram for POESLLC is shown in Figure-4.

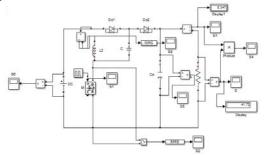


Figure-4. Simulation circuit of POESLLC.

The DC input voltage to the POESLLC is 14V and it is shown in Figure-5. The inductor current of POESLLC is shown in Figure-6. From the Figure-6 it is understood that it is 30.63 amps. The output voltage of POESLLC is 41.73V and it is shown in Figure-7. The Output Current of POESLLC is 8.3 amps and it is shown in Figure-8.

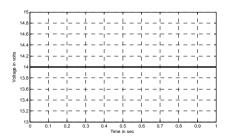


Figure-5. Input voltage to the POESLLC.

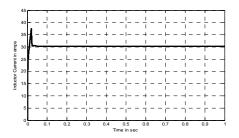


Figure-6. Inductor current of POESLLC.

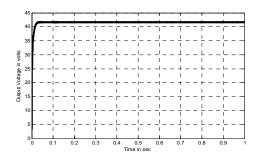


Figure-7. Output voltage of POESLLC.

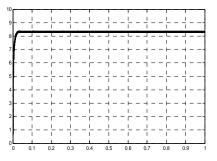


Figure-8. Output current of POESLLC.

LUO Converter with Short Circuit fault is simulated using the blocks of simulink. The circuit diagram with short circuit switch fault is shown in Figure-9.

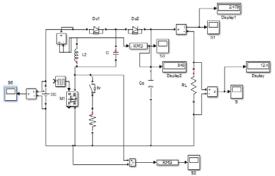


Figure-9. Simulation circuit of POESLLC with short circuit fault.

Short Circuit Fault on the device is created by connecting the low resistance in parallel with switch through circuit breaker. The value of resistance is low so that the current starts to pass through the resistance when the circuit breaker is closed. So there occurs a shorting of switch. The DC input Voltage is 14V and it is shown in Figure-5. The inductor current is 840Amps because a short circuit fault is created and it is shown in Figure-10. The output voltage of POESLLC decreases to 12.4V and it is shown in Figure-11. The output current decreases to 2.4 amps from 8.4 amps and it is shown in Figure-12.

# ARPN Journal of Engineering and Applied Sciences

©2006-2015 Asian Research Publishing Network (ARPN). All rights reserved.

¢,

### www.arpnjournals.com

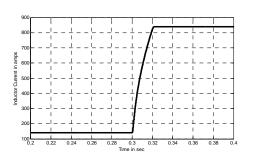


Figure-10. Inductor current during short circuit fault in POESLLC.

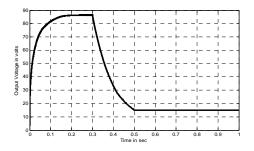


Figure-11. Output voltage during short circuit fault in POESLLC.

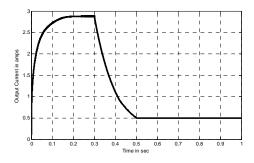


Figure-12. Output current during short circuit fault in POESLLC.

The circuit for clearance of short circuit fault is shown in Figure-13 which contains a additional circuit breaker. Whenever a short circuit in the switch occurs the breaker disconnects source from the converter. and thus the converter is protected from getting damaged. The input voltage is 14V which is shown in Figure-5. The inductor current decreases becomes of short circuit to 0 amps which is shown in Figure-14. The output voltage also decreases because of short circuit fault to 0.23V which is shown in Figure-15. The output current is 0.007 amps which is shown in Figure-16. The switching signal to the circuit breaker is shown in Figure-17. The breaker signal will be "1" if there is no fault in the converter. But if there is fault the signal to the breaker is "0".

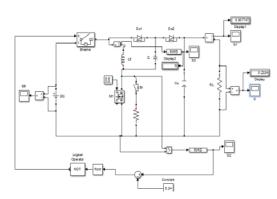


Figure-13. Simulation of short circuit fault clearance circuit.

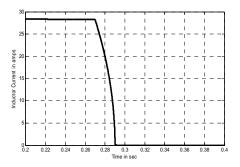


Figure-14. Inductor current in short circuit fault clearance circuit.

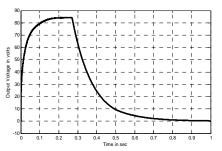


Figure-15. Output voltage current in short circuit fault clearance circuit.

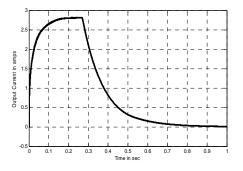


Figure-16. Output current in short circuit fault clearance circuit.

ARPN Journal of Engineering and Applied Sciences

©2006-2015 Asian Research Publishing Network (ARPN). All rights reserved.

#### www.arpnjournals.com

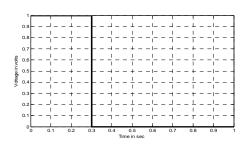


Figure-17. Switching signals to circuit breaker current in short circuit fault clearance circuit.

The POESLLC with open Circuit fault is simulated using the blocks of simulink. The circuit diagram with open circuit switch fault is shown in Figure-18.

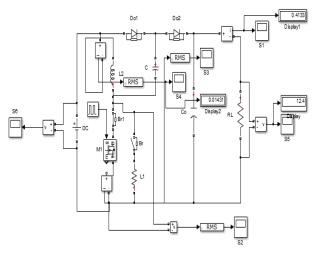


Figure-18. Simulation circuit of POESLLC with open circuit fault.

The Open Circuit Fault in the POESLLC circuit is created by connecting the high resistance in parallel with switch through circuit breaker. The value of resistance is high so that the current is made to flow in resistor by disconnecting the switch using a breaker so that the open circuit fault occur in the converter circuit. The DC input Voltage is 14V which is shown in Figure-5. The inductor current decreases to 0.01 amps as shown in Figure-19. The output voltage is 12.4 V which is shown in Figure-20. The output current is 0.41 amps which is shown in Figure-21.

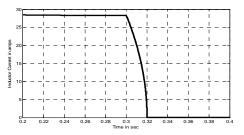


Figure-19. Inductor current during open circuit fault.

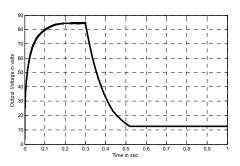


Figure-20. Output voltage during open circuit fault.

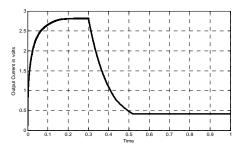


Figure-21. Output current during open circuit fault.

The circuit for clearance of open circuit fault is shown in Figure-22. The input voltage is 14 V shown in Figure-5. The inductor current gets reduced 0 amps and it is shown in Figure-23. The output voltage is 9.8 V and it is shown in Figure-24. The output current is 0.41 amps shown in Figure-25. The input signal to the breaker is show in Figure-26. The breaker signal will be "1" if there is no fault in the converter. But if there is fault the signal to the breaker is "0".

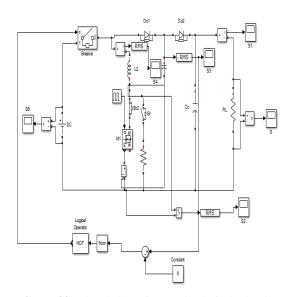


Figure-22. Simulation of open circuit fault clearing circuit.

ARPN Journal of Engineering and Applied Sciences

©2006-2015 Asian Research Publishing Network (ARPN). All rights reserved



www.arpnjournals.com

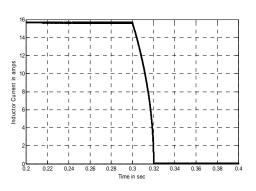


Figure-23. Inductor current in open circuit fault clearing circuit.

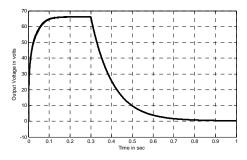


Figure-24. Output voltage in open circuit fault clearing circuit.

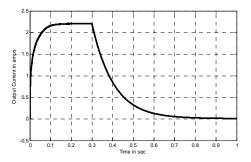


Figure-25. Output current in open circuit fault clearing circuit.

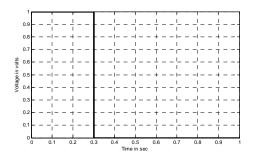


Figure-26. Switching signals to circuit breaker in open circuit fault clearing circuit.

### 4. CONCLUSION

Open Circuit and Short circuit Switch faults are created, analysed and simulated successfully. The results of simulation for open circuit and short circuit switch faults are presented. The indication of increasing current in the inductor represents the short circuit fault. The indication of zero current in the inductor represents open circuit fault of the switch. The present work deals with crisp logic controlled simulation study. Simulink models for open circuit in closed loop circuit and short circuit faults in closed loop are developed and they are used for simulation. The simulation results closely agree with theoretical results.

# REFERENCES

- Mahmoud Shahbazi, Ehsan Jamshidpour, Phillippe Poure, Shahrokh Saadate and Mohammad Reza Zolghadri. 2013. "Open Circuit and Short circuit switch fault diagnosis for non isolated DC-DC converter using FPGA", IEEE tran of Indus elect. Vol 60, No. 9, ppl. 4136-4146, September.
- [2] A.Amaral and A.Cardoso. 2012. "on line fault detection of aluminium electrolytic capacitor, in step don DC-DC converter using input current and output voltage ripple", IET power electron., Vol 5, No. 3, pp 315-322, March.
- [3] K.Ramash Kumar and S.Jeevananthan. 2010. "PI Control For Positive Output Elementary Super Lift LUO Converter", world academy of science, engg. and tech. Vol 4, March.
- [4] Luo.F.L. 1998. "LUO converters voltage lift technique" proceedings of IEEE pow. elect., special conference IEEE-PESC'98 Fukuoka, japan 17-22, pp.1783-1789, May.
- [5] P.Lezana, R.Aguilera and J.Rodriguez. 2009. "Fault detection in multicell converter based on output voltage frequency analysis ", IEEE tran, Indus elect., Vol. 56, No. 6, pp.2275-2285, June.
- [6] S.Cruz, M.Ferreira, A.Mendes, and A.J.M.Cardoso. 2012. "Analysis and diagnois of open circuit faults in matrix converter", IEEE Trans. Indus.Elect., Vol. 58, No. 5, pp 1648-1661, May 2011, January.
- [7] S.Khwan-on, L.De Lillo, L.Empringham and P.Wheeler. 2012. "Fault tolerant matrix converter motor drives with fault detection of open switch faults" IEEE Tran. Indus.Elect., Vol. 59, No. 1, pp 257-268, January.
- [8] D.U.Campos-Delgado and D.R.Espinoza-Trejo. 2011. "An observer based diagnosis scehe for single and simultaneous open switch faults in inductyion motor

©2006-2015 Asian Research Publishing Network (ARPN). All rights reserved.



### www.arpnjournals.com

drives", IEEE tran. Ind.Elect. Vol. 58, No. 2, pp 671-679, February.

- [9] M.Shahbazi, P.Poure, S.Saadate and M.R.Zolghadri. 2013. "Fault tolerant five leg converter topology with fpga based reconfigurable control", IEEE Tran. Indus Elect., Vol. 60, No. 6, pp. 2284-2294. June.
- [10] M.Gonzalez, B.Raison, S.Bacha and L.Bun. 2011. "Fault diagnosis in a grid connected phto voltaic system by applying a signl approach", in proc, 37<sup>th</sup> IECON, pp.1354-1359.
- [11] A.Izadian and P.Khayyer. 2011. "Application of Kalman filter is model based fault diagnosis of a DC-DC boost converter", in pro. IEEE VPPC, Chicago, IL, pp.1-6.
- [12] X.Pei, S.Nei Y.Chen and Y.Kang. 2012."open circuit fault diagnosis and fault tolerant stratergies for full bridge DC-DC converters", IEEE Tran. Pow elect., Vol. 27, No 5, pp 2550-2565, May.
- [13] Sivachidambaranathan.V and Dash S.S. 2012. "A Novel Soft Switching High Frequency AC to DC Series resonant Converter", National Journal electronics sciences and systems. Vol. 3, No. 1, pp 1-12.
- [14] G.T.Sundar Rajan and C.Chistober Asir Rajan. 2011. "Input Stage improved power fator of three phase diode rectifier using hybrid unidirectional rectifier", in proc.IEEE conf. On Nano Sience, Engineering and Technology –ICONSET-, Sathyabama University, pp 697-682, nov 28-30, Chennai, India.
- [15] Sasi Kumar.M and Pandian.S.C. 2011. "Modelling and analysis of cascaded H bridge inverter for wind driven isolated seld exited induction generators", journal of electrical engineering and informatics, Vol.3, No. 2, pp.132-145.
- [16] Jayaprakash.S and V.Ramakrishnan. 2014. "A new single-stage solar based controlled full-bridge DC-DC converter." Indian Journal of science and technology Vol. 7 No. 9, pp. 1386-1390.
- [17] A.Ramesh Babu, and T.A.Ragavendiran. 2014. "Performance enhancement of high voltage gain two phase interleaved boost converter using mppt algorithm", journal of theoretical and applied information technology, Vol. 68, No. 2 pp. 360-368, October.