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SLEW RATE ENHANCING TECHNIQUE IN DARLINGTON PAIR BASED CMOS OP-AMP

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ABSTRACT

In this paper the Darlington pair and internal circuit biasing technique is used for the enhancing the slew rate as well as gain and unity gain bandwidth. The proposed CMOS Op-Amp has been verified through Cadence Analog Design Environment with spectre simulator in the standard 45nm CMOS process. In this proposed circuit the gain stage is divided in two parts, first is modified gain stage and second one is Darlington pair stage. The effects of both the modified gain stage and Darlington stage currents are considered in this circuit and a simple analytical expression is given in terms of the load and compensation capacitors. The new scheme allows the slew rate to be increased with only a small increase in static power consumption. At the dc power dissipation of 0.76 mW, the proposed circuit achieves a slew rate of 2791V/µs, gain of 70 dB and unity gain bandwidth of 1.74 GHz.

Keyword: slew rate, darlington pair, op amp, UGB, load capacitor, compensation capacitor.

1. INTRODUCTION

Op-amp is versatile and widely used in all modern instrumentation, communication, and sensor systems, etc. For sensor system where the output switches from one level to another quickly is required. In these applications the rate at which the op amp can change between the two levels is important that is input and output level. Therefore, high slew rate based op-amp architecture should be required. This motivates developing special architecture, which improve op-amp slew rates.

The maximum rate of output excursion defines the slew rate of an amplifier's. The maximum change in the output voltage with respect to per unit time is defined as slew rate. The limitation of slew rate is that it can increase the effect of nonlinearity in op-amp. The output of the op-amp can not able to rise instantaneously to the input voltage at ideal value. The output will be a linear ramp of slope equal to SR. Then its output is slew rate limited and it said to be slewing.

If signals will become distorted, i. e. op amp is operated above its slew rate limit. Slew rate also influences achievable performance in sensor system, filters, D/A output stages, video amplification and data acquisition.

$$SR = \left.\frac{dv_o}{dt}\right|_{\max} \quad (1)$$

Due to the different internal circuitry of op amp arises the slew rate. There are two main reasons, which is responsible for the limitations of op amp chips [1]:

Frequency compensation: The coupling capacitors and load capacitor used within the chip to affect the high frequency response, results change in the slew rate. Compensating the value of capacitor is also limiting the rate of change that can occur at the output, and therefore it affects the slew rate of the op amp.

Output driver limitations: It is found that rise and fall slew rates may be different, results that the chip increases and decreases the output voltage.

In the past many have been designed and reported slew rate-enhanced circuits in different CMOS technologies. A simple and efficient CMOS buffer amplifiers with slew rate enhancement was simulated in 1.5 um CMOS technology, which could achieve 1V/us with capacitive loads 10000 pF and power consumption of less than 1.5mW [2]. A rail to rail CMOS op-amp, implemented in 0.35 um CMOS technology to operate with power consumption 30 mW, capacitive load of 10 pF, gain 54 dB and 6.1 MHz bandwidth has been reported [3]. In [4] A Low- power high-slew-rate buffer amplifier with slew rate 10 V/us for a load capacitance 1 nF was implemented in 0.35 um CMOS process. A High Slew-Rate CMOS Amplifier with both Power supply rejection ratio and slew rate was fabricated in 2 µm CMOS technology [5]. It could achieve 80 V/µs slew rate, positive-supply rejection ratio of 73 dB and negative-supply rejection ratio of 57 dB at 50 KHz with power dissipation of 1 mW. In [6] design circuit was fabricated in a 0.5-µm digital CMOS process which achieves slewing current variation versus common-mode i/p less than ±2% with power consumption 2.3 mW. A Class-AB CMOS Buffer with Slew-Rate 81 V/µs and 1.090 % THD at 10 KHz sin input was reported in 0.35 µm CMOS technology [7]. A op-amp was simulated in 0.35 µm CMOS technology with slew rate 857V/ µs at 0.5 pF load Capacitor [8]. It also achieves a good gain and UGB, 67 dB and 1.25 GHz respectively.

The rest of this paper has been organized as follows. The basic principle of Slew rate of op-amp is given in Section II. Section III describes the methodology and architecture of the proposed circuit. The simulation result and discussion has been summarized in Section IV. Finally, the conclusion of the overall paper is illustrated in Section V.

2. BASIC PRINCIPLE

The bias current source is directly proportional to the slew rate of op-amp in the first stage, which will increase the power dissipation of the circuit. The objective of the presented in this paper is to achieve a high slew rate, with a low power overhead while maintaining other performance of op-amp unchanged [9]. The internal architecture of the op amp is responsible for the slew rate. Due to limited bandwidth of the op-amp, there are linear phenomenon occurred I. e. It does not lead nonlinear distortion. An op-amp connected in unity gain configuration as shown in Fig 1. The output would be expected from the follower if the only limitation on its dynamic performance is the finite op-amp bandwidth. The transfer function of unity gain op-amp [10-11].

$$\frac{V_o}{V_i} = \frac{1}{1 + s/\omega_t} \tag{2}$$

Which is low pass STC response with a time constant $1/\omega_t$. Therefore the step response should be

$$v_o(t) = V\left(1 - e^{-\omega_t t}\right) \tag{3}$$

Due to different circuit configuration of op amps, it may have different slew rates for positive and negative transitions. The different configuration of op-amp is responsible for the different slew rate. They have a complementary output to pull the signal up and down and i.e. the circuit cannot be exactly the same at two sides. [1].

3. PROPOSED DARLINGTON PAIR BASED OP-AMP

The proposed circuit of enhancing the slew rate is shown in Figure-1. The proposed circuit mainly categorized into two stages. The first part is the simple differential stage and the second part is a common source.

The first stage of operational amplifier circuit is known as differential stage (Figure-1). The transistors M3 and M4 construct the input stage of the differential stage (V→I) and the transistors M1 and M2 composes the current mirror of the differential stage (I→V), which provides the gain and slew rate of circuit in the first stage. The purpose of the M5 is to supply biasing current to the differential stage. It consists of cascaded voltage-to-current (transconductance stages) and current-to-voltage stages (load stages). The step input is appears as a differential signal between two input terminals, such a large signal will exceed the voltage required to turn off one side of the input differential pair. The sink current pulled by coupling capacitor C_C Then the output voltage will be ramp with slope I/ C_C. That is

$$v_o(t) = \frac{I}{C_C} t \tag{4}$$

Thus the slew rate

$$SR = \frac{I}{C_C} \tag{5}$$

The proposed circuit is divided in two parts in gain stage, which are used for improvement in slew rate. First one is modified gain stage and the second one is Darlington stage. The principle of operation is detecting the onset of slewing operation of the circuit and activating the additional current sources in the appropriate directions. The additional current sources are activated only during the slewing operation of the op-amp circuit, and hence power dissipation and other performance measures of the basic op-amp circuit mostly remains unchanged. The transistor M8, M9 and M10 are modified gain stage. The M11 is biasing transistor, which provide the transconductance for Darlington pair transistor. The second stage of gain stage is a Darlington pair stage. The effect of transistor D1 is to increase the current gain through the stage and to increase the input resistance. For the purpose of the low-frequency, small-signal analysis of circuits, the two transistors D1 and D2 can be thought of as a single composite Transistor. The UGB of Darlington stage is

$$UGB = f_t = \frac{g_{D1}}{C_{gsMb1,Mb2}} \tag{6}$$

g_m = Transconductance.

C_{gs} = Gate to source capacitance.

A simple relationship between UGB and slew rate is

$$UGB = \frac{g_m}{2\pi C_C} \tag{7}$$

And

$$g_m = \frac{I}{V_{ov}} \tag{8}$$

$$SR = 2\pi f_t V_{ov} \tag{9}$$

Thus the slew rate is determined by overdrive voltage of transistor D1 and D2. A high slew rate is obtained by D1 and D2 at larger V_{OV}.

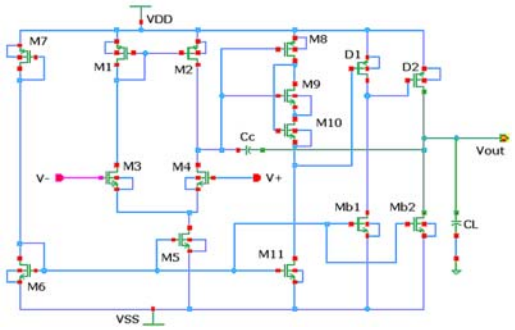

Figure-1. Proposed op amp circuit.

4. SIMULATION RESULTS

The proposed in this paper has been simulated in Analog Design Environment of Cadence using 45nm library. The proposed circuit operates at ±1V supply. Almost the important parameters of op-amp have been extracted from the circuit, however the Slew rate characteristics shows superior results however all results are unchanged. The proposed circuit has been designed. The slew rate at different load capacitor and fixed compensation capacitor is shown in Figure-2.

The rise slew rate of circuit given as the minimum deviation from actual value at any given capacitor in between the specified range of the circuit. For the specified range of the given proposed circuit the rise slew rate shows an 2791V/µs, at .5 pF load capacitor while shows a of 1418 V/µs at 1pF load capacitor. The graph for slew rate at different load capacitor are given in Figure-3.

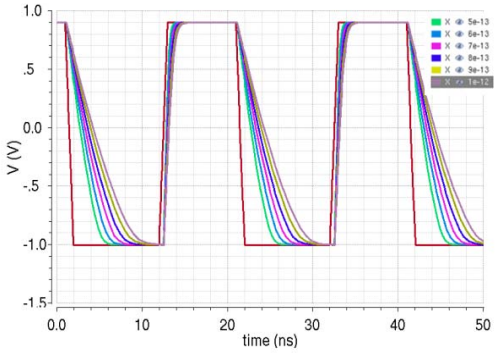

Figure-2. Slew rate at different load capacitor.

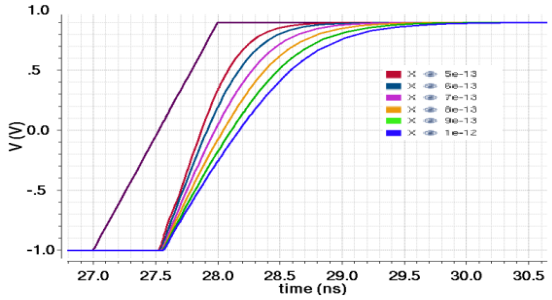

Figure-3. Rise slew rate.

The circuit has been simulated fall slew rate at different capacitor value to get the better operating conditions. The circuit has been simulated in five different capacitor values. The simulation result is shown in Figure-4. From the result, it can be observed that at .5 pF load capacitor 505 V/µs shows the better result for the designed circuit. The rise and fall slew rate is summarized in Table-1.

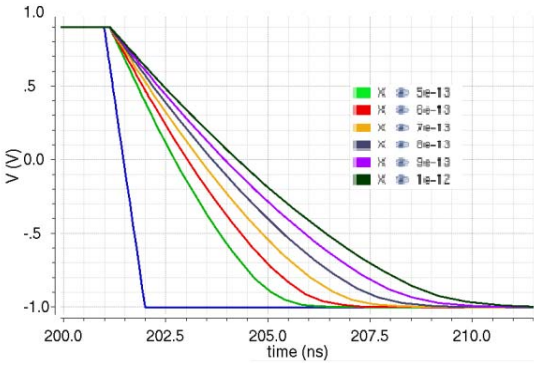

Figure-4. Fall slew rate .

Table-1. Slew Rate at different load capacitor.

Load capacitor (pF)	**Rise slew rate** (V/µs)	**Fall slew rate** (V/µs)
1	1418	257
0.9	1663	290
0.8	1845	336
0.7	2000	365.2
0.6	2576	435
0.5	2791	505

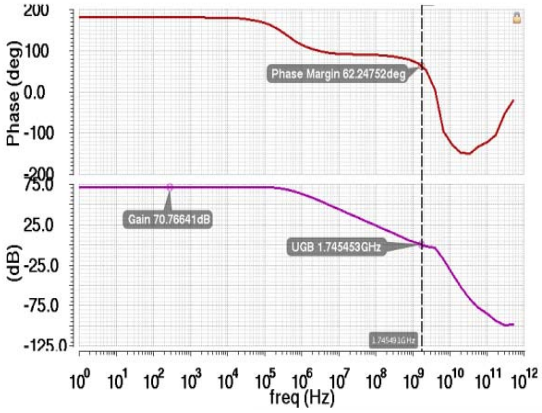

Figure-5. AC response of propoesed circuit.

Table-2. Performance comparison of proposed circuit with previously designed circuit for slew rate improvement.

Parameter	[12]	[7]	[8]	Proposed Circuit
Technology	5 µm	350 nm	350 nm	45 nm
Power supply	±5 V	3 V	3.3 V	±1 V
Slew rate	128 V/µs	81 V/µs	857 V/µs	2791 V/µs
Gain	54 dB	-	67 dB	70 dB
Phase	-	-	65 ^{o}	62 ^{o}
UGB	15 MHz	-	1.25 GHz	1.74 GHz
Power consumption	7.5 mW	243 µW	9.5 mW	0.76 mW

The AC response of the proposed Op amp, are shown in Figure-5. For 0.5 pF load capacitor, the proposed Op amp achieves a DC gain 70 dB and UGB 1.74 GHz. The overall resultant power dissipation of the proposed circuit with improved slew rate. In Table-2 the proposed op-amp has been compared with previously designed circuits. From the table it can be observed that the proposed circuit shows a high slew rate. Generally for CMOS op-amp the slew rate is directly proportional to the bias current of MOSFET, and hence increasing the power consumption. But, the proposed design keeps the power consumption in check, well within 0.76 mW.

5. CONCLUSIONS

The proposed circuit presented in this paper utilizes the variation in load capacitor. The rise voltage produces better results in terms of slew rate for the designed circuit. The rise slew rate of the designed circuit is also quite high. Moreover the slew rate of circuit for 2791 V/µs. The gain and phase of the circuit is also quite good with respect to the frequency. The power dissipation of the circuit is also on the lower side, which is well under 1mW. Since the proposed circuit for a widespread range of slew rate with satisfactory can find its application in military and aerospace sensor applications.

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