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INPUT VECTOR MONITORING CONCURRENT BIST ARCHITECTURE USING MODIFIED SRAM CELLS

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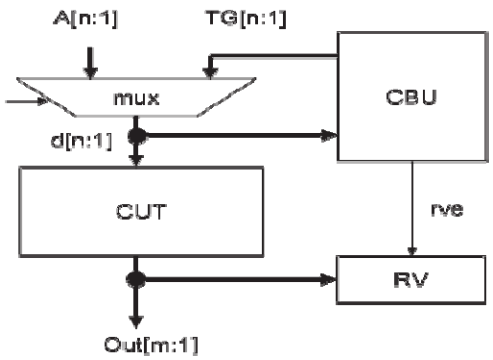
ABSTRACT

Input vector monitoring concurrent BIST performs two modes of operation, normal mode and test mode during test mode the test generator value is compared with higher order bits and the output is given to comparator circuit. During normal mode the inputs to the CUT are driven from the normal inputs. The modified SRAM is used to reduce the switching activity hence the dynamic power dissipation can be reduced. The output is verified by response verifier (RV) and the fault is identified using testing. The operating speed is faster since the operation is carried out as parallel process and it is suitable for all the type of IC's.

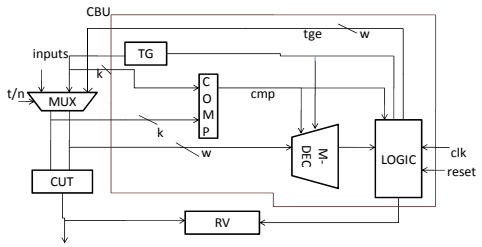
Keywords: comparator, test generator enable, concurrent BIST unit, modified SRAM, logic module, concurrent test, response verifier.

1. INTRODUCTION:

Built-in-self test (BIST) techniques constitute a class of schemes that provide the capability of performing testing with high fault coverage. Hence, they constitute an attractive solution to the problem of testing VLSI devices. BIST techniques are typically classified into offline and online. Offline architectures operate in either normal mode (during which the BIST circuitry is idle) or test mode. During test mode, the inputs generated by a test generator module are applied to the inputs of the circuit under test (CUT) and the responses are captured into a response verifier (RV).The bits are classified into higher and lower order bits. During the normal mode the vector that drives the inputs of the CUT is driven from the normal input vector. It operates in two modes. When T/N=0 it operates in normal mode, if T/N=1 the operation is said to be in test mode. The modified decoder and the modified SRAM are used. The decoder operation is carried along with TGE and CMP values based on which the decoding operation occurs. Modified SRAM is used not only for storing purpose but also for reducing the switching activity. This leads to reduction in dynamic power dissipation. The output from both the logic circuit and the CUT are captured and it is verified using response verifier (RV). The process is carried out parallel hence speed of operation is more.



2. BLOCK DIAGRAM DESCRIPTION



a) Hardware test pattern generator

This module generates the test patterns required to sensitize the faults and propagate the effect to the outputs. As the test pattern generator is a circuit (not equipment) its area is limited. So storing and then generating test patterns obtained by ATPG algorithms on the CUT Using the hardware test pattern generator is not feasible. Instead, the test pattern generator is basically a type of register which generates random patterns which act as test patterns. The main emphasis of the register design is to have low area yet generate as many different patterns (from 0 to 2^{n-1}, if there are *n* flip-flops in the register) as possible.

b) Decoder

A decoder is a device which does the reverse operation of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. In digital electronics, a decoder can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input

and output codes are different. e.g. n-to-2^n, binary-coded decimal decoders. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word. Decoding is necessary in applications such as data multiplexing, 7 segment display. The example decoder circuit would be an AND gate because the output of an AND gate is "High" (1) only when all its inputs are "High." Such output is called as "active High output". If instead of AND gate, the NAND gate is connected the output will be "Low" (0) only when all its inputs are "High". Such output is called as "active low output". A slightly more complex decoder would be the n-to-2^n type binary decoders. These type of decoders are combinational circuits that convert binary information from 'n' coded inputs to a maximum of 2^n unique outputs, the decoder may have less than 2^n outputs. There is 2-to-4 decoder, 3-to-8 decoder or 4-to-16 decoder.

c) Comparator

Comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes. The circuit, for comparing two n-Bit numbers, has 2^n inputs. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. Circuit size depends on the number of transistors and their sizes and the wiring complexity. The wiring complexity is determined by the number of connections and their lengths. All these characteristics may vary from one logic style to another and thus proper choice of logic style is important. The test generator value from the logic block and the higher order bits from the mux unit are compared and the output is given to the logic module block from which the output is obtained based on testing. The testing process is carried out in parallel manner. Based on which the response verifier is activated.

d) SRAM

SRAM is a type of semiconductor memory that uses bitable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data eminence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered.

The power consumption of SRAM varies widely depending on how frequently it is accessed; it can be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used with applications such as moderately clocked microprocessors, draws very little power and can have a nearly negligible power consumption in the region of a few micro-watts.

e) CUT

During normal mode, the inputs to the CUT are driven from the normal inputs. The *n* inputs are also driven to the CBU as follows: the *w* low-order inputs are driven to the inputs of the decoder; the K high-order inputs are driven to the inputs of the comparator. When a vector belonging to the current window reaches the inputs of the CUT, the comparator is enabled and one of the outputs of the decoder is enabled. During the first half of the clock cycle (clk and cmp are enabled) the addressed cell is read; because the read value is zero,the *w*-stage counter is triggered through the NOT gate with output the response verifier enable (rve) signal. During the second half of the clock cycle, the left flip-flop enables the AND gate (other input is clk and cmp), and enables the buffers to write the value one to the addressed cell.

f) Mux

Mux serve as the examples for circuit analysis and modular design. A 2^n-to-1 multiplexer sends one of

2^n input lines to a single output line.

A multiplexer has two sets of inputs: 2^n data input lines .n select lines, to pick on the 2^n data inputs The mux output is a single bit which is one of the 2n data inputs.

g) Proposed scheme

In proposed scheme modified SRAM cell is used which reduces the switching activity and reduces dynamic power dissipation hence the circuit performance is improved and the fault is identified using testing. The speed of operation is improved using parallel processing and suitable for even scan based BIST architectures. The fault coverage is said to be accurate since it identifies the location of fault.

DECODER OUTPUT

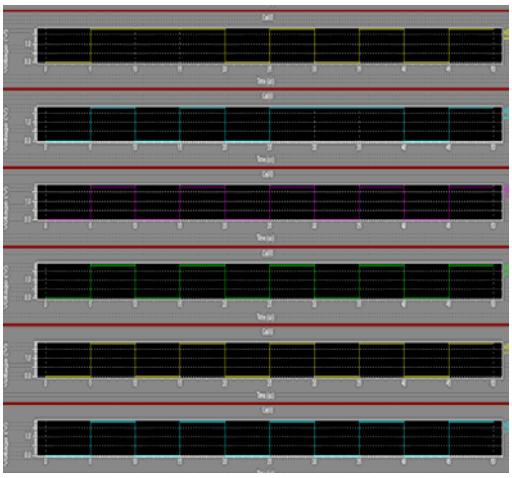


Figure-1. Decoder output.

COMPARATOR OUTPUT

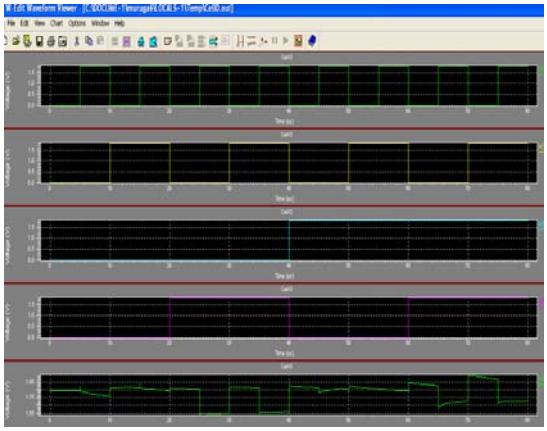


Figure-2. comparator output.

BCUT OUTPUT

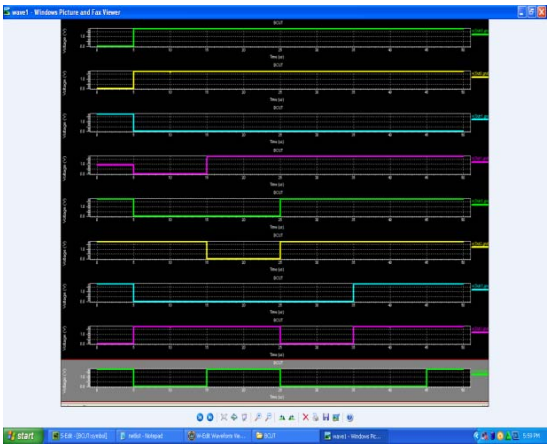


Figure-3. Bcut output.

F. 10T SRAM

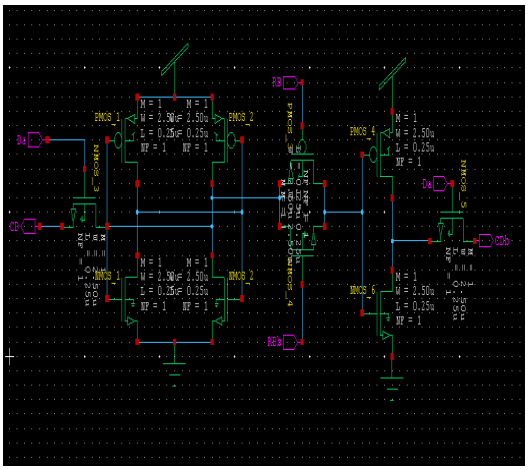


Figure-4. 10T SRAM schematic diagram.

A 10T SRAM cell, as the name suggests, consists of 10 transistors. Out of these transistors, four are pull-up transistors (PUL1, PUL2, PUR1 and PUR2), four are pull down transistors (PDL1, PDL2, PDR1 and PDR2) and two are access transistors (PGL and PGR)[3]. The two pull-down transistors i.e. PDL1 and PDR1 are connected to VGND. This VGND signal is connected to ground during the read operation and VDD, otherwise. In 10T SRAM cell, the access transistors are connected to pseudo nodes (PQ and pQb i.e. nodes between two pull-up transistors) rather than the storage nodes (i.e. Q and Qb). Due to this, the storage nodes are isolated from the BLs and therefore during the read operation, the read current does not flow through the storage nodes and hence maintain the read stability.

In case of the write operation, the VGND is connected to VDD and one of the bit-lines e.g. BL is grounded. Suppose the node Q is storing '1' and node Qb is storing '0'. When a high supply voltage is provided, the node Q is pulled down to '0' due to discharging through the access and the pull-up transistor i.e. PGL and PUL2. Standard Vth pull-up transistors, low Vth access transistors and high Vth pull-down transistors. Due to the low Vth transistors, the gate voltage (Vg) required for activation of the access transistors is low and thus, the access speed for the data stored increases considerably. Also the high Vth Pull-down transistors decrease the leakage in the circuit. In our work, we have used dual Vth scheme in 10T SRAM cell. The working of this cell is the same as the standard Vth 10T SRAM cell except for the access transistors (PGL and PGR), which are used here, have low Vth and the pull-down transistors (PDL2 and PDR2) have high Vth . As explained earlier, due to the low Vth of the access transistors, the access speed of the transistors increases considerably.

This helps in faster access of the data stored in the SRAM cell. Also due to the high Vth pull-down transistors, the leakage of the circuit through theses transistors decreases. Hence, the performance of the cell increases as compared to the dual Vth 6T SRAM cell on an area-power trade-off.

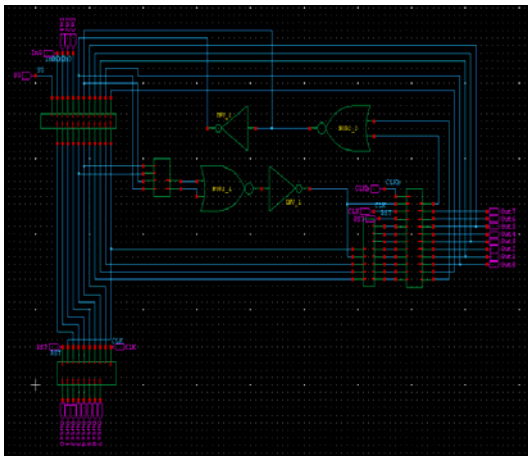


Figure-5. MCUT schematic diagram.

Here the inputs are given internally and externally. During normal mode the inputs to the CUT are driven from the normal inputs. During the test mode the tge (TEST GENERATER VALUE) is compared with higher order bits and the output is given to compartor circuit. The logic block is designed using 10T SRAM inordre to reduce the number of switching activites by means of increasing the transistors hence the chip size can be reduce and the dynamic power dissipation can be reduced. By means of MCUT the speed of operation of the circuit can be improved with reduced power consumption and fast access of data with less memory space.

Tanner Tool 13.0

Low total cost of ownership: Tanner has created a software platform that is cost-effective and easy to use, while still being powerful enough to handle complex designs. Through the years Tanner EDA has remained true to its mission by delivering tools on the Windows infrastructure that can easily augment a company's existing design tool flow.

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Flexible PC-based solutions: Tanner EDA tools are fully optimized for the Windows PC platform, enabling users to leverage their existing infrastructure and work at the office or at home. The flexibility of this platform, along with its familiar, intuitive interface gives designers customizable solutions that are fully portable. This is a good choice for designers who need high-performance EDA tools at a reasonable price.

Production proven tools: During its 20-year history, Tanner EDA has established a reputation as a leading technology innovator and supplier of cost-effective, flexible, and reliable production tools. Today the company boasts 4,000 customers and over 25,000 active licenses in 64 countries worldwide.

Power comparison

	Logic module 10T	**Logic module 6T**
Average Power	1.773648*10^-3watts	2.162147*10^-3watts
Maximum Power	5.828863*10^-3watts@5.00059*10^-6	1.741064*10^-2watts@5.00059*10^-6

	MCUT	**BCUT**
Average Power	2.004839*10^-3watts	1.253295*10^-2watts
Maximum Power	1.390751*10^-2watts@4.50008*10^-5	2.500751*10^-2watts@4.50007*10^-5

CONCLUSIONS

BIST schemes constitute an attractive solution to the problem of testing VLSI devices. Input vector monitoring concurrent BIST schemes perform testing during the circuit normal operation without imposing a need to set the circuit offline to perform the test, therefore they can prevent problems appearing in offline BIST techniques. The operation is carried out both in normal mode and test mode .During normal mode the outputs from the CUT and logic block are verified using response verifier RV. During test mode the values are generated and the output is verified based on that values. Based on clock and selection lines the output is executed using the tanner tool 13.0.The inputs can be changed for different combinations using netlist. Using modified SRAM cells the switching activities are reduced which leads to decreased power consumption.

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