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MODELLING AND PERFORMANCE COMPARISON OF GRAPHENE AND CARBON NANOTUBE BASED FETS

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ABSTRACT

The era of nanoelectronics has emerged to overcome the effects of limits of physics due to technology scaling. Hence there is a need to explore the use of advanced nanomaterials namely, graphene and carbon nanotube that can overcome the limitations of short channel effects that arise in conventional silicon based field effect transistors (FET). The high carrier mobility of these materials on a substrate at room temperature and high electron velocity and thermal conductivity, are the motivation to explore the possibility to use FETs based on these materials. The focus in this work is the electronic characterization of such FET models. In this work, SPICE compactible models using closed form equations that are suitable for future circuit level simulations have been developed for single gate graphene FET (GFET), dual gate GFET (DG-GFET) and carbon nanotube field effect transistor (CNT-FET). This paper presents a modified single gate GFET model that is compatible with device length of 100nm and it is found to have better linear and saturation characteristics compared with the existing model. The modified GFET is found to have dirac point stability for lower values of drain to source voltage (V_{ds}<0.4V) which is suitable for voltage scaling. A ballistic, non-linear piece-wise approximation approach in CNT-FET has been applied to achieve the saturation of drain current rather than using the computationally complex self-consistent field approach. This work also presents a detailed study of variation in transconductance and transit frequency for the modified GFET model and it is established to have a higher transit frequency at 100nm than the existing model. The simulation of models and comparison of various parameters are done using MATLAB.

Keywords: graphene field effect transistor (GFET), dual gate graphene field effect transistor (DG-GFET), carbon nanotube field effect transistor (CNT-FET), simulation, modelling, MATLAB, SPICE model, mixed signal modelling.

1. INTRODUCTION

The possibility of achieving electron mobilities, which are orders of magnitude higher than silicon-based technologies, makes graphene-based field-effect transistors (GFETs) excellent candidates for replacing CMOS nanometric scale transistors in analog and digital electronic circuits [1]. This work presents the development of advanced nanomaterials based FET models and a comparative study between graphene FET (GFET), dual gate GFET (DG-GFET) and carbon nanotube FET (CNT-FET) models, to bring out current, transconductance and transit frequency values to enable the electronic characterization of the devices with a future aim of developing circuits for RF application.

The single gate GFET models in [1] and [2] have provided compact models for device length up to 440nm. This work provides modifications to compact model that enables simulation of GFET at 100nm for both large signal and small signal models.

Compact models with closed expressions are essential because only such models can be used in circuit level simulators like SPICE or mixed signal modelling. Such expressions can be easily used for hand calculations while designing circuits. Here simulations have been carried out in MATLAB to simplify the verification on the effectiveness of each model. In future, the model can also be implemented in analog and mixed signal language to compare the results with that obtained from MATLAB.

The developed compact model can in turn be used in analog or digital circuits where in the small signal and large signal parameters can be used to design those circuits. A study has been carried out on transit frequency characteristics which give us crucial information about the GHz ranges in which this device model can be employed.

Fundamentally, the reasons for preferring DG-GFET over single gate GFET are to achieve dirac point stability and better saturation values for drain current. It is noteworthy that the GFET model presented here has already achieved these two criteria. The shortcoming of this model is that the dirac point stability can be achieved only for lower values of drain-source voltage (Vds<0.4). But this in turn is good because as scaling happens the device voltages will also be cut down. But to achieve dirac point stability for higher Vds, we still have to depend on DG-GFET.

In this work, a study has been carried out on the modified GFET model, by varying the range of values of input parameters like length of channel and the supply voltage to find out its effect on the GFET model parameters such as drain current, transconductance and transit frequency. Further, in order to provide better control on the conductivity in channel due to electrons and holes, the DG-GFET has been implemented [3]. This work newly presents a relative study based on the drain current variation with gate voltage of the single and dual gate GFETs. Both models are SPICE compatible.

A CNT-FET model having piece wise non-linear approximation of charge densities in the channel have been modelled. In this model the time consuming numerical integration of density of states and Newton-Raphson iterations have been avoided. This model has been compared to the GFET model.

This paper is organized as follows. Section II presents a brief summary about the previous works carried out about the non-silicon based FETs under our consideration. Characteristic equations that represent the three FET models have been dealt with in Section III. Section III also highlights the modification done in GFET parametric equations that enabled us to carry out the model simulation at 100nm which was earlier carried out at 440nm [2]. Simulation results and comparison between the three FET models have been provided in section IV. Finally section V summarizes the results and observations from this work.

2. LITERATURE SURVEY

A. Graphene field effect transistor

During the last few years, outstanding RF performance has been shown by graphene-based FETs. The drift-diffusion equation based model study has been done as in [5] and [12]. Physical and compact models have been put forward by Meric et al. [6], Thiele et al. [7] and Landauer et al. [15]. The first one takes into account quantum ballistic transport in the graphene channel, while latter works are based on the drift equation.

The analytical models that can predict the electrical characteristics of graphene field effect transistors have been introduced recently. These models are very complex and cannot be handled using circuit simulators like SPICE [1]. In this project, we have built GFET compact model based on the work from [6] and [7] and modified them as in section III.

B. Dual Gate - Graphene field effect transistor

Many physical models exist that calculate the drain current generated by a DG-FET taking into consideration the total electrical charge present in graphene channel based on the energy levels of band structures in the channel. These models are generally too complex, and time consuming when the device is used in circuit level modelling. Reference [9] presents a model of dual gate DG-GFETs that has energy band gaps which can be varied by applying a vertical electric field. Another approach considers zero energy bandgap in graphene channels [7].

The model employed here provides simulation for scaled down back gate voltage when compared with work done in [14]. It considers the difference in electron and hole mobility in the Graphene channel. This results in a change in carrier density as well as mobility in GFET. Also, the effects of top and bottom gate capacitances have been included while forming the equations for channel potential which shows the effect of back gate voltage changes on operation of GFET. This uses equations in closed form.

C. Carbon Nanotube - Field Effect Transistor

In CNTFET model described in [4] and [13], the total current flowing through channel is calculated by approximating the total mobile charge density in the channel by considering ballistic transport. Method like Newton-Raphson is usually utilized to solve non-linear algebraic equation to obtain drain current equation in [8]. Techniques such as non-linear approximation by parts have been devised by which we can eliminate the need for time consuming iterations. A model without any numerical integration has been described as in [16]. To analyze the effect of the Schottky barriers, researchers have used the non-equilibrium Green's function (NEGF) to model the CNTFET [10].

3. IMPLEMENTATION OF FET MODELS

A. Graphene field effect transistor model

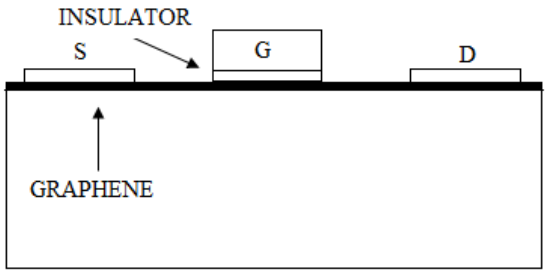

Figure-1. Cross-sectional view of the GFET structure.

1) Large signal model

The drain current equation encloses the physics of the device in a single expression. The drain current derived in [2] is modified to obtain the Eq. 1. Here the total voltage can defined as $V_{tot}=V_{eff}-(0.5V_{dsi})$.

$$Id = \frac{\mu W Ctop Vtot}{\frac{L}{Vdsi} + \frac{\mu}{\omega}\sqrt{\frac{\pi Ctop}{e}} * \sqrt{Vtot}} \quad (1)$$

Where width of transistor is represented by W, μ is the mobility, L is the transistor length, e is the elementary charge (1.6×10^{-19} As), C_{top} is the top gate oxide capacitance and ω is derived from the phonon energy of the substrate ħω. This derivation has been done under the assumption that the $V_{eff} > V_{dsi}/2$. Here effective voltage is given by $V_{eff} = V_{gsi} + V_{th,0}$.

2) Small signal model

The aim of the small signal model is to develop compact equations for the important parameters namely transconductance and transit frequency that are significant in the design of amplifiers. The parameters provided in this model are used to perform quantitative circuit analyses of the behavior of amplifier configurations. The transconductance g_m is the parameter of importance in determining the analog gain and hence imperative in analog and mixed signal designs.

a) Transconductance (g_m)

The transconductance efficiency g_m/I_d gives a measure of the amount of current required to produce

amplification in the output voltage. So it gives an idea about the efficiency in consumption of power of the device under consideration. The expression for the transconductance gain can be directly derived from Equation (1).

$$g_m = \left(\frac{I_d}{V_{tot}}\right) * \left(1 - \frac{I_d}{2W\omega}\sqrt{\frac{\pi}{eC_{top}}} * \frac{1}{\sqrt{V_{tot}}}\right) \quad (2)$$

This model is also efficient when $V_{eff} > V_{dsi}/2$. Therefore, the best g_m performance is actually achieved at low V_{eff} voltages.

b) Transit frequency (f_T)

The focus of our work in the usage of advanced nano material based FETs is to obtain the electronic characterization of the new devices at 100 nm by determining the transit frequency. This parameter provides insight into the high frequency of operation of the devices at nano scale using graphene single gate, multi gate and CNT. f_T is defined as the frequency at which the current gain of the device becomes equal to one, and it is a measure of high-speed and bandwidth that can be achieved by the device. The transit frequency is defined as given below.

$$f_T = \frac{I_d / V_{tot}}{2\pi(1.5C_{top}WL)} * \left(1 - \frac{I_d}{2W\omega}\sqrt{\frac{\pi}{eC_{top}}} * \frac{1}{\sqrt{V_{tot}}}\right) \quad (3)$$

B. Dual Gate - Graphene field effect transistor model

The drain current obtained by taking into consideration the drift velocity and the carrier concentration as summed up in [12] is given below.

$$I_d = q\frac{W}{L}\int_{V(x=0)}^{V(x=L)} \overline{n(x)} V_{drift,eff}(x)dx \quad (4)$$

The average carrier over the channel is given by Eq. 5.

$$\overline{n(x)} = \frac{1}{V_c}\int_{V(x=0)}^{V(x=L)} \sqrt{{n_0}^2 + \left(\frac{C_{top}(V_{tg} - V(x) - V_{tg,0})}{e}\right)^2} \quad (5)$$

Where n_0 is the intrinsic carrier concentration, C_{top} is the top gate capacitance, V_{tg} is the gate bias, V(x) is the voltage in the channel at position x and $V_{tg,0}$ is the charge neutrality voltage. The channel voltage is given by Equation (6).

$$V_c = \frac{C_{top}}{C_{top} + C_{back} + C_q}(V_{tg} - V_{tg,0} - v(x)) + \frac{C_{back}}{C_{top} + C_{back} + C_q}(V_{bg} - V_{bg,0} - v(x)) \quad (6)$$

Where C_q is the quantum capacitance, V_{bg} is the back gate voltage and $V_{tg,0}$ and $V_{bg,0}$ are the top and back gate voltages when there is charge neutrality, C_{top} and C_{back} are the top and back gate capacitances. The effective drift velocity is given by

$$V_{drift,eff} = \sqrt{{V_{drift,e}}^2 + {V_{drift,h}}^2} \quad (7)$$

$V_{drift,e}$ and $V_{drift,h}$ are the drift velocities of electrons and holes respectively.

C. Carbon Nanotube - Field effect transistor model

According to ballistic model in [4], the dynamic charge created in the channel will not be in equilibrium and is given by Equation (8).

$$\Delta Q = q * (N_{si} - N_{di} - N_0) \quad (8)$$

Here N_{si} and N_{di} represents the density of states having positive and negative velocity respectively. N_0 is the density of electrons at equilibrium. The self-consistent voltage illustrates that CNT energy bands are directly related to the terminal charges, electron densities and terminal capacitances as in [4].

$$V_{sci} = -\frac{Q_{si} + q(V_{sci}(N_{si} + N_{di}) + N_0)}{C_m} \quad (9)$$

Where Q_{si} denotes the charge accumulated and is given by Equation (10).

$$Q_{si}(V_{sc}) = (-(0.5N_0) + N_s)q \quad (10)$$

The total capacitance is given by Equation (11).

$$C_m = C_{gi} + C_{di} + C_{si} \quad (11)$$

Where C_{gi}, C_{di}, and C_{si} are the gate, drain and source capacitances respectively. According to [10] the total output current can be obtained using Equation (12).

$$I_d = \frac{2qkT}{\pi\hbar}\left(F_o\left(\frac{U_{s1f}}{kT}\right) - Fo\left(\frac{U_{d1f}}{kT}\right)\right) \quad (12)$$

Here where F_o presents the Fermi-Dirac integral, k is Boltzmann's constant, T is the temperature and $\hbar$ is reduced Planck's constant.

$$F_o(\eta) = \log\left(1 + e^{\eta}\right) \quad (13)$$

As V_{sci} is known, the the output current can be easily be derived from equations (12) and (13) and is given by Equation (14).

$$I_d = \frac{2Tkq}{\pi\hbar}\left(\log\left(1+e^{\frac{E_{fi}-qV_{sci}}{kT}}\right)-\log\left(1+e^{\frac{E_{fi}-q(V_{sci}-V_{dsi})}{kT}}\right)\right) \quad (14)$$

4. SIMULATION RESULTS

All the three models namely GFET, DG-GFET and CNT-FET have been developed using MATLAB. These models have been simulated and characteristic graphs of the device are monitored to study the effect of variation in voltage and device length.

A) Simulation of Graphene FET

1) Output characteristics (I_d versus V_{ds})

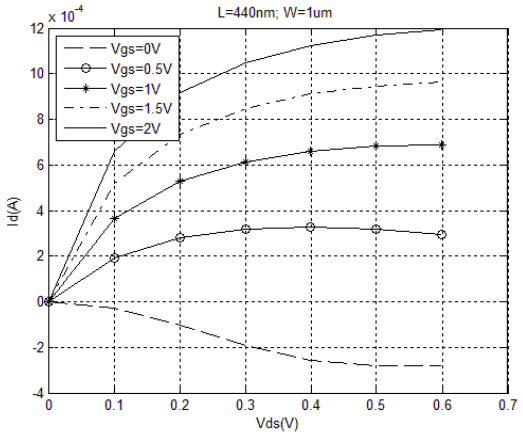

Figure-2. Graphene drain current as obtained using the model in [1] with L=440nm, C_{top} = 3.6 × 10−3 F/m^2, μ = 7000 cm^2 V^{-1} s^{-1}, and ω = 8.5*10^{13} Hz.

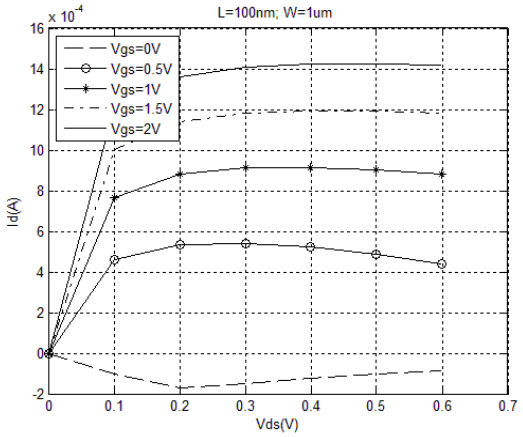

Figure-3. Graphene drain current calculated using the modified model with L=100nm, C_{top} = 3.6 × 10−3 F/m^2, μ = 7000 cm^2 V^{-1} s^{-1}, and ω = 8.5*10^{13} Hz.

In the modified work simulation shown in Figure-3, we have achieved better consistent saturation in drain current even for device length of 100nm whereas [1] had implemented for 440nm only which is shown in Figure-2. Also it can be observed that linearity in the first triode region is improved in our work when compared with the existing one.

The linear region of operation can be used to implement FET as resistors or switches; the saturation region can be used to implement voltage controlled current sources and the negative resistance region can be used to build oscillators. The second linear region is not implemented by Equation (1) because of the assumption $V_{eff} > V_{dsi}/2$ which does not hold true here.

2) Transfer characteristics (I_d versus V_{gs})

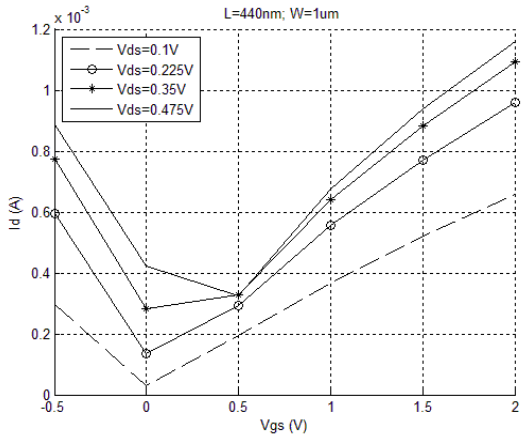

Figure-4. Shows ambipolar conduction and dirac point calculated as obtained using the model in [1] with L=440nm, C_{top} = 3.6 × 10−3 F/m^2, μ = 7000 cm^2 V^{-1} s^{-1}, and ω = 8.5*10^{13} Hz.

The transfer characteristic has been found to hold good in modified model with length of 100nm. For positive values of V_{gs}, the conduction in the device is due to electrons and for negative values of V_{gs} the conduction is due to holes. Since graphene is a zero bandgap semiconductor, it always conducts and the gate voltage at which minimum conduction occurs is called dirac point. From Figure-5 we can see that modified model has dirac point stability for Vds<0.475V, which restricts the usage of voltage ranges for this model.

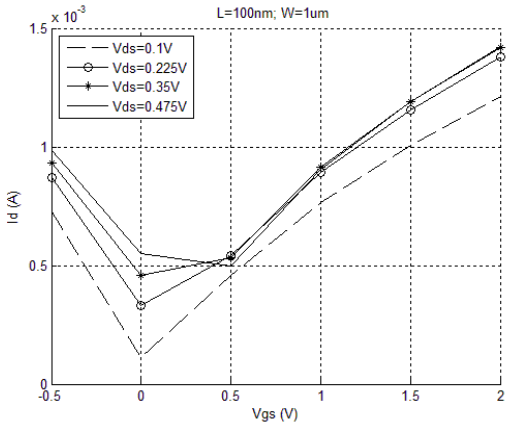

Figure-5. Shows ambipolar conduction and dirac point calculated using modified model with L=100nm, C_{top} = 3.6 × 10−3 F/m^2, μ = 7000 cm^2 V^{-1} s^{-1}, and ω = 8.5*10^{13} Hz.

3) Transconductance characteristics (g_m)

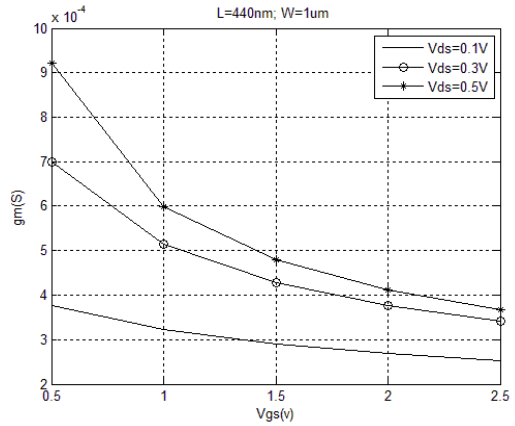

Figure-6. Shows variation of transconductance with Vgs as obtained using model in [1] with L=440nm, C_{top} = 3.6 × 10−3 F/m^2, μ = 7000 cm^2 V^{-1} s^{-1}, and ω = 8.5*10^{13} Hz.

The modified model simulation shown in Figure-7, with reduced length has achieved higher conductance for same voltage as in [1] and better characteristics. It is interesting to notice that g_m drops substantially at large gate biasing voltages, mainly due to the effect of v_{SAT}. Therefore, the best transconductance is actually achieved at low V_{eff} voltages.

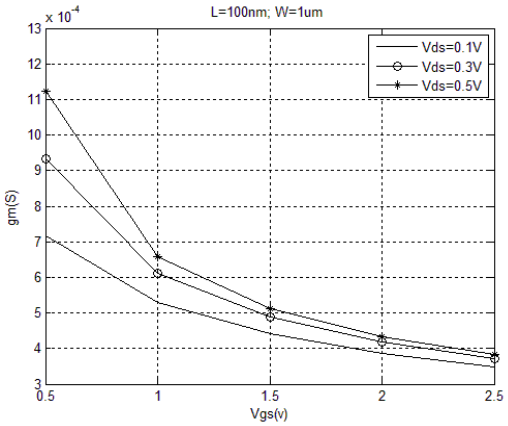

Figure-7. Shows variation of transconductance using modified model with L=100nm, C_{top} = 3.6 × 10−3 F/m^2, μ = 7000 cm^2 V^{-1} s^{-1}, and ω = 8.5*10^{13} Hz.

4) Transit frequency characteristics (f_T)

Comparing with Figure-9 with Figure-8, we can see that we have achieved higher transit frequencies. It can also be noted that higher transit frequencies are achieved for lower gate voltages which will be an advantage when voltages are brought down due to scaling. Hence this model is preferable for low voltage applications requiring high frequencies of operation.

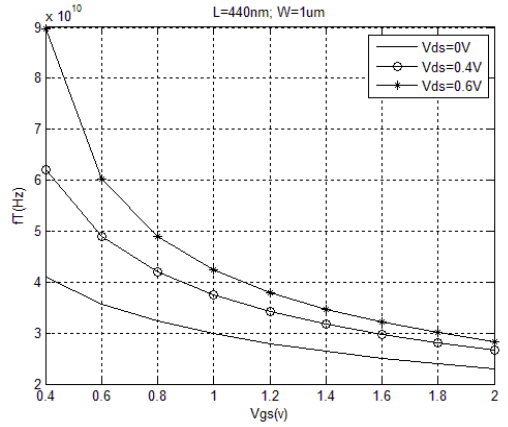

Figure-8. Shows variation of transit frequency with Vgs obtained using model in [1] with L=440nm, C_{top} = 3.6 × 10−3 F/m^2, μ = 7000 cm^2 V^{-1} s^{-1}, and ω = 8.5*10^{13} Hz.

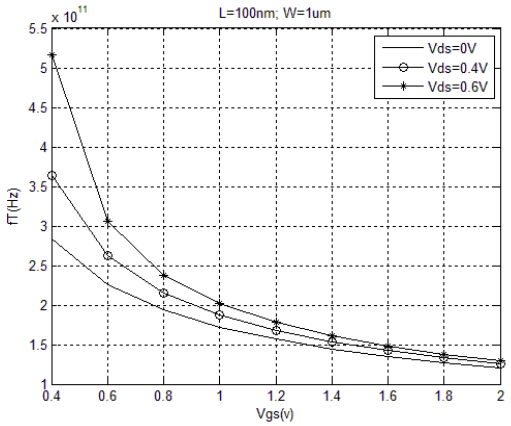

Figure-9. Shows variation of transit frequency with Vgs calculated using modified model with L=100nm, C_{top} = 3.6 × 10−3 F/m^2, μ = 7000 cm^2 V^{-1} s^{-1}, and ω = 8.5*10^{13} Hz.

Table-1. Parameter comparison for different lengths of GFET using modified model.

Parameter \ length	3μm	1μm	440nm	100nm
I_{dmax}(mA)	0.68	10.4	12.1	14.1
g_m(mS)	0.33	0.68	0.92	11.2
$f_T(10^{10})$Hz	41	2.6	9	52

From Table-1 we can observe that both the maximum current conduction through GFET and transconductance has increased when model length is reduced to 100nm. The transit frequency increases as effective length is reduced for lengths below 1μm. But there is an exception when the length of channel is 3μm. This exception can be overlooked as this model is aimed at nanometric applications.

B. Simulation of dual gate Graphene fet

1) Transfer characteristics (I_d versus V_{gs})

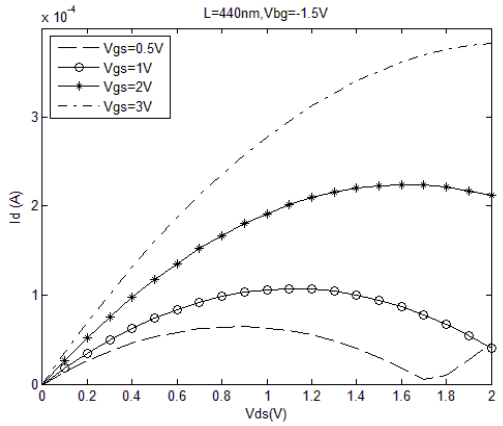

Figure-10. Shows variation of drain current with V_{ds} calculated with L=440nm, C_{top} = 209× 10^{-9} F, C_{back}=11.5x10^{-9} F.

From Figures 10 and 11 we can infer that, for a particular value of V_{ds} the drain current increases when channel length is reduced. The Figures 11 and 12 shows drain current with respect to drain voltage when back gate voltage is -1.5V and -5V respectively. The inference that can be made from the two figures is that, for a particular value of V_{gs} as the back gate voltage is increased in negative direction, drain current also increases.

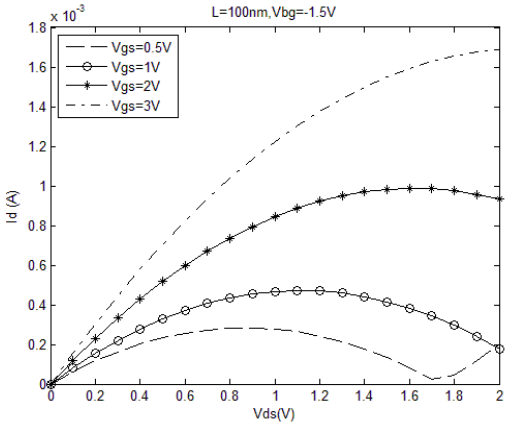

Figure-11. Shows variation of drain current with V_{ds} calculated with L=100nm, C_{top} = 209× 10^{-9} F, C_{back}=11.5x10^{-9} F, V_{bg}=-1.5V.

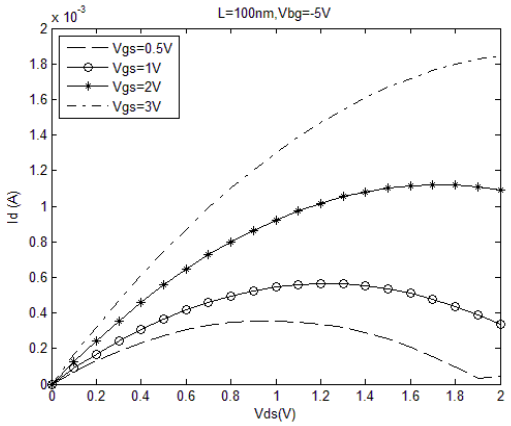

Figure-12. Change in drain current with V_{ds} calculated with L=100nm, C_{top} = 209× 10^{-9} F, C_{back}=11.5x10^{-9} F, V_{bg}=-5V.

Table-2. Parameter comparison between GFET and DG-GFET.

Parameter \ device	**GFET**(100nm)	**DG-GFET**(100nm)
I_{dmax} (mA)	14.1	1.18
g_m (mS)	11.2	0.89

From the Table-2 we could infer that modified GFET model is preferred to DG-GFET model implemented here, when higher I_{dmax} and g_m are required criterion. But we need to depend on DG-GFET to achieve stable dirac point when V_{ds}>0.475V.

C. simulation of Carbon Nanotube FET

1) Transfer characteristics (I_d versus V_{gs})

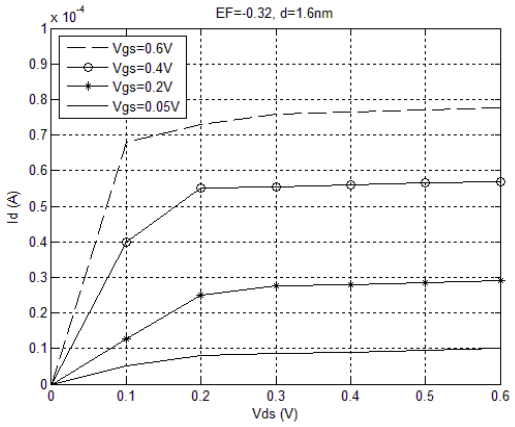

Figure-13. Shows change in drain current with V_{ds} calculated with d=1.6nm and T=300K.

In Figure-13, we can observe the triode and saturation regions of operation of the CNT-FET device model. We have been able to achieve the saturation of drain current by non-linear piece-wise approximation approach, rather than using the computationally complex self-consistent field approach. This is

Comparing with Figure-2, this implemented CNT-FET in Figure-13 has lower drain current for a gate to source voltage of 0.6V. (Approximately 0.08mA for CNT-FET and 0.6mA for GFET). So GFET model is preferred when maximum current is the important criterion. Also the difficulty to fabricate CNT-FET is a disadvantage because of it 3D nature. So GFET can be used when the model has to be cost effective.

CONCLUSIONS

A comparative study between GFET, DG-GFET and CNT-FET models has been done. The modified GFET model was found to possess more stable saturation and triode region characteristics at 100nm than in the previous work at 440nm. The drain current was found to increase with scaling in GFET. Higher transit frequency characteristics were achieved at 100nm than in [1] due to incorporation effective channel voltage using modification of f_T as in section III. The implemented GFET is found to have dirac point stability for lower values of drain to source voltage (V_{ds}<0.4V). This in turn is good because as scaling happens the device voltages will also be cut down. But if dirac point stability is required for higher values of V_{ds}, then DG-GFET will be the suitable FET model.

GFET was found to have higher conductance than DG-FET at same specifications. Hence GFET is preferable over GFET if drain current and transconductance are the parameters of importance. When GFET and CNT-FET models were compared at same gate voltage, GFET was found to have higher conductance. Hence GFET is preferred over CNT-FET because of the difficulty and cost involved in fabrication of CNT-FET.

In future, these device models can be developed as analog mixed signal (AMS) libraries to be used in circuit level simulation to implement an application.

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