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GLITCH FREE NAND BASED DCDL IN PHASE LOCKED LOOP APPLICATION

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ABSTRACT

This paper presents a glitch free NAND based digitally controlled delay lines for the avoidance of glitches by using different driving circuits. In glitch free NAND based DCDL, driving circuits are used to generate the control bits which consumes considerable amount of power and delay time. Driving techniques suggested here are dual edge triggered sense amplifier based flip-flop and NIKOLIC sense amplifier based flip-flop, which comparatively have reduced power consumption and delay time. The proposed NAND based DCDL have been designed in 90nm CMOS technology and various performances of these techniques are compared by the simulation parameters like power, area and delay. In addition, the proposed DCDL is adopted in phase locked loop.

Keywords: digitally controlled delay lines (DCDL), glitches, NIKOLIC sense amplifier based flip-flop, dual edge triggered sense amplifier based flip-flop, phase locked loop (PLL).

1. INTRODUCTION

Glitching is the most common design problem in many digital circuits which may affect the results such as loss of data, increased throughput and power consumption. An electronic glitch is an unwanted pulse or spike which occurs in a digital circuit. In other perception, glitch is an undesired transition or unpredicted output of a digital circuit which occurs before the signal settles to its specified value and hence it results in false output. Glitches occur due to the propagation delay in the digital circuit. The proposed NAND based DCDL avoids the glitches problem and also achieves the low power and delay time.

NAND based DCDL is a digital circuit whose delay is controlled by the digital control word. DCDL plays an important role in many applications such as All-Digital Phase Locked Loop (ADPLL) [3], All Digital Delay Locked Loop (ADDLL) [4], [5], All Digital Spread-Spectrum Clock Generator (SSCG) [2], Clock Generators, microprocessors etc.

2. EXISTING METHODOLOGY

A. Glitches problem of NAND based DCDL

In [1], [4] NAND based digitally controlled delay lines (DCDL) is constructed by a series of delay elements (DE) is shown in the Fig.1. Each delay element is composed of four NAND gates. In Fig.1, each NAND gates marked with 'A' are the fast input and 'D' are the dummy cells which is used for load balancing. The delay of the DCDL circuit is controlled through the control bits (S_i). The control bits are S_0, S_1, S_2, S_3 and complementary of those control bits S'_0, S'_1, S'_2 and S'_3.

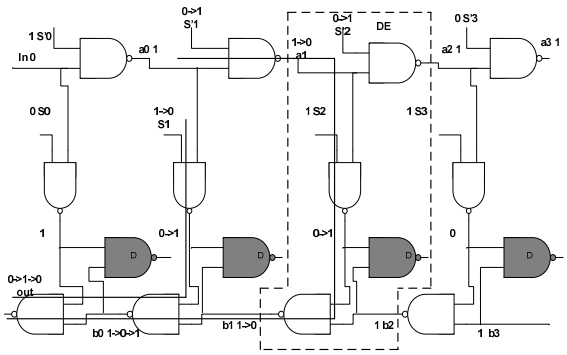

Figure-1. Single glitch when the control code increased by one.

Consider the situation if the control code 'c' is switched from 1(s=0,1,1,1) to 2(s=0,0,1,1) glitches are generated in two different paths as indicated by the solid lines. If it is one bit variation, a single glitch occurs. The control bits Si encode the delay control code c.

If i<c, then Si=0 (pass state); if i≥c, then Si=1 (turn state),where i is the number of stages, c is the control code and Si is the control-bits.

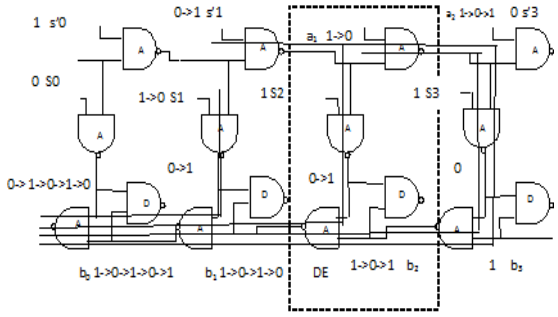

Figure-2. Multiple glitches when the control code increased by two or more.

Figure-2 shows, if the control code 'c' is switched from 1(s=0,1,1,1) to 3(s=0,0,0,1), glitches are generated in four different paths as shown in red lines. If there were more than one bit variation, then there would be the occurrence of multiple glitches.

B. Glitch-free NAND based DCDL

Glitches can be avoided by increasing the control bits which are Si and Ti. So that, each delay element in DCDL requires two sets of control bits Si and Ti which controls the DCDL with the conditions: Consider the state if i<c, then Si=0 and if i ≥c, then Si=1; and also the control code Ti=1 and Tc+1=0 for i≠c+1. The corresponding schematic diagram of glitches free NAND based DCDL is shown in Figure-3.

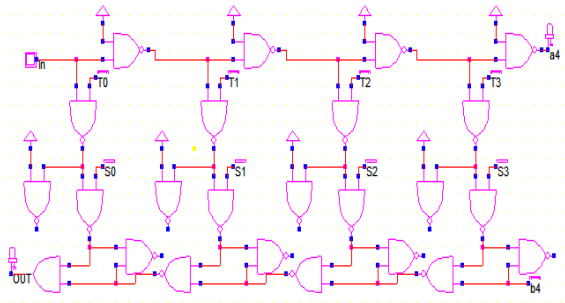

Figure-3. Schematic of glitch-free NAND based DCDL.

The three possible delay elements (DE) states of glitch free DCDL and the corresponding values of Si and Ti are shown in the Table-1.

Table-1. States of de in glitch-free dcdl.

S_i	T_i	DE STATE
0	1	Pass
1	1	Turn
1	0	Post-Turn

C. Conventional NAND based DCDL using a Double clocked sense amplifier based flip-flop

The conventional DCDL uses the double clocked flip-flop as a driving circuit [1], [9]. This is one of the special flip-flops which employs two different clock signals, so that it can provide different delays for LH and HL transitions. One of these clock signals is CLH. I.e., Clock signal rises when low to high transitions. Another one is CHL. I.e., Clock signal falls when high to low transitions. But this too have some of the drawbacks such as consumption of more power and consumes more delay time. This sense amplifier based flip-flop consists of sense amplifier in the first stage and set-reset (SR) latch in the next stage. This conventional flip-flop is shown in the Figure-4. This sensing stage capture the input signal state on the clock rising edges and a latch stage provides the two flip-flop outputs are detailed in Figure-4 and can be realized by using a simple NAND based SR latch or more advanced structures [6], [8]-[10].

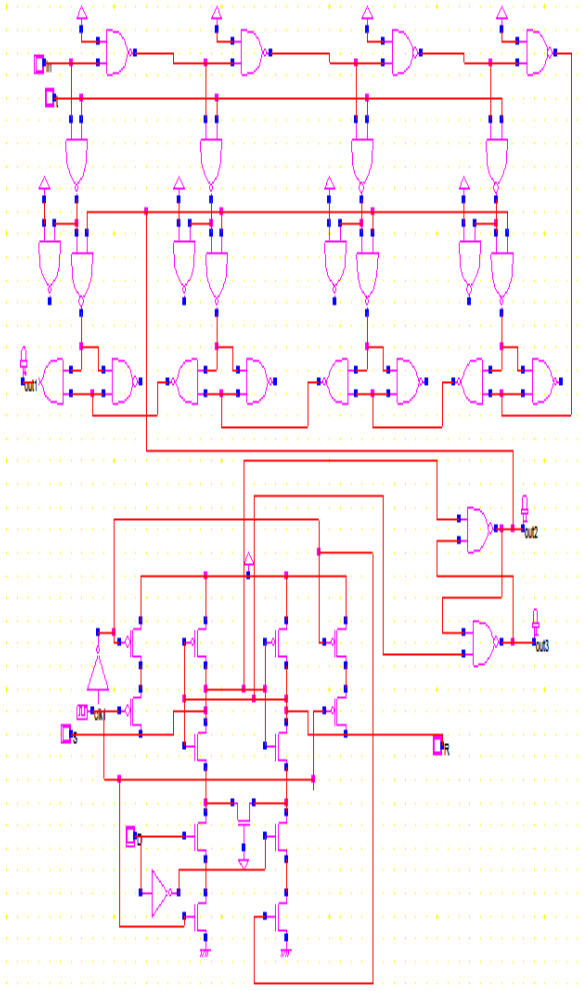

Figure-4. Schematic of existing DCDL with double clocked sense amplifier based flip-flop.

3. PROPOSED NAND BASED DCDL

Proposed NAND based DCDL uses two different driving techniques. That is a sense amplifier based dual edge triggered flip-flop and NIKOLIC sense amplifier based flip-flop. By using these proposed driving techniques, the power and delay time of glitches free NAND based DCDL is reduced.

A. Proposed NAND based DCDL with dual edge triggered sense amplifier based flip-flop

The sense amplifier based dual edge triggered flip-flop is constructed by using three stages. Those are pulse generating stage, the sensing stage and the latch stage. The pulse generating stage is used to generate a exact pulse at both the rising and falling edges of the given clock signal.

For a sense amplifier stage, in the evaluation phase, if the given input as D is low, SB is set to high. And if the input D is high, RB is set to high. The conditional precharge technique is used to avoid redundant transitions at the major internal nodes.

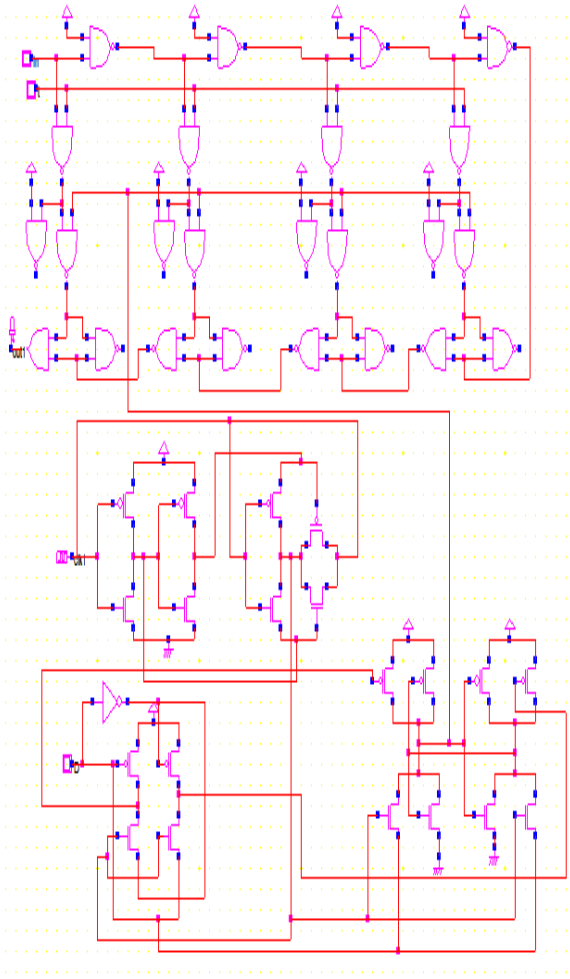

Figure-5. Schematic of proposed DCDL with dual edge triggered sense amplifier based flip-flop.

To improve the operating speed, a fast symmetric latch is developed, which can be shown in the Figure-5. This latch used to SB and RB to pull up the output nodes. When SB is low, the output Q will be high and when RB is low, the output QB will be high. In latching stage, the pull down path is developed as a pulse controlled NMOS pass transistor, through which D and DB are directly fed to output nodes.

B. NIKOLIC sense amplifier based flip-flop

A NIKOLIC-latch sense amplifier based flip-flop employs two inverters to evaluate the signals S and R are used to drive four devices N1, N2, P1 and P2 which in turn are devoted to switching Q and QB nodes. A role of this flip-flop is to reduce the use of clock signal so that NIKOLIC latch had a better power consumption. This technique is shown in the Figure-6.

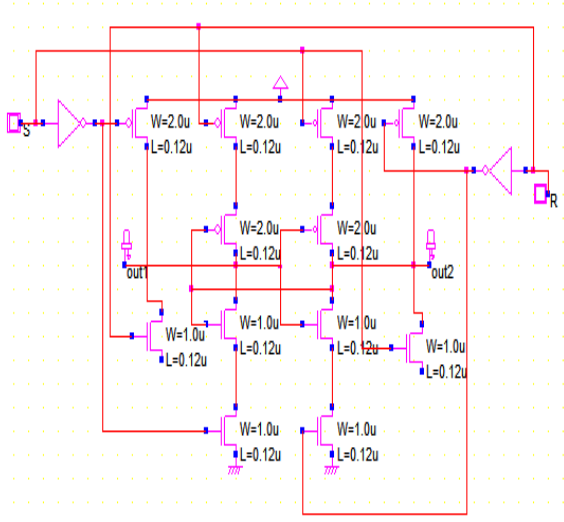

Figure-6. NIKOLIC latch sense amplifier based flip-flop.

C. DCDL in PLL application

The PLL architecture is shown in the Figure-8 and is detailed in [7]. It has four major blocks, namely the phase/frequency detector, loop filter, digitally controlled delay loop and frequency divider. The phase detector detects the phase difference between the input reference signal and output feedback signal which is shown in the Figure-7.

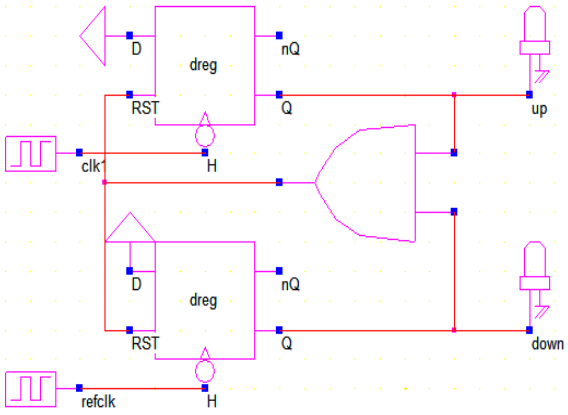

Figure-7. Phase/Frequency detector.

Based upon the error signal the charge pump either increases or decreases the charge to the low pass filter. This loop filter removes high frequency and then applied to the input of DCDL. The proposed DCDL has better performances in delay and power consumption. The output from the DCDL is given to frequency divider. It takes an input signal frequency and generates the output signal frequency.

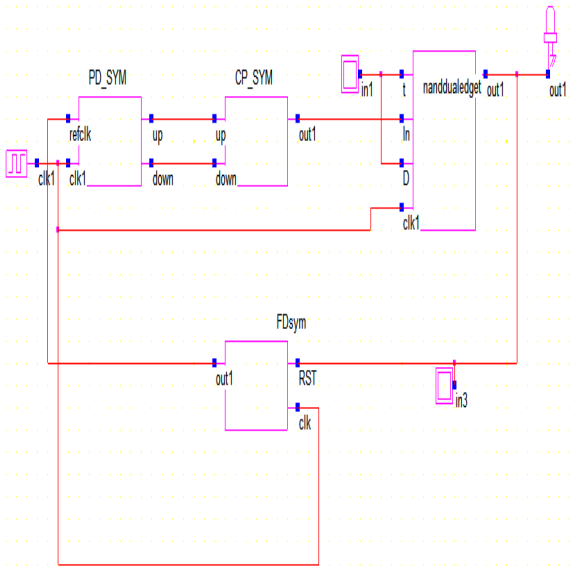

Figure-8. Phase locked loop architecture.

4. SIMULATION ANALYSIS

A. Simulation result of DCDL with double clocked flip-flop

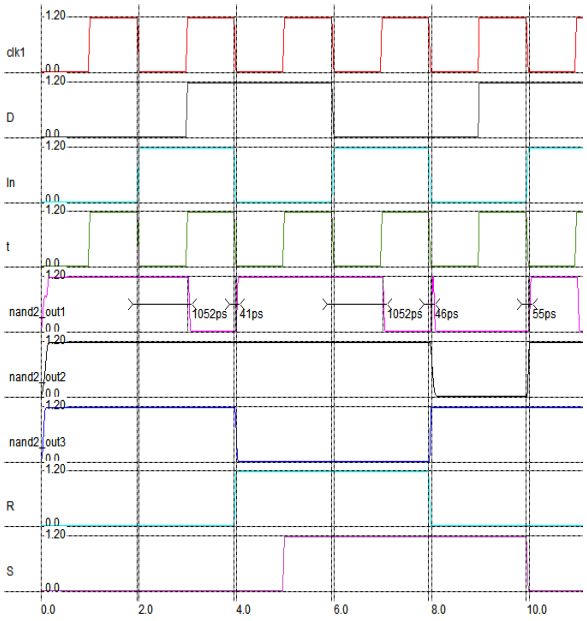

Figure-9. DCDL with double clocked flip-flop.

Simulation result of Existing DCDL with double clock flip-flop as shown in the Figure-9.

B. Simulation result of proposed DCDL with dual edge triggered flip-flop

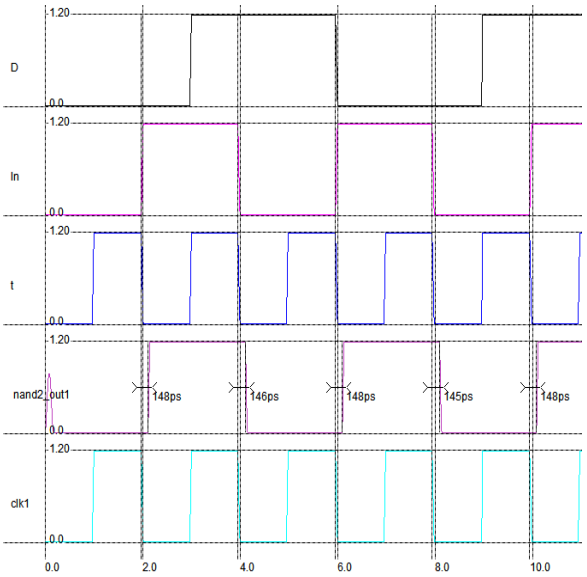

Figure-10. Simulation result of proposed DCDL with dual edge triggered flip-flop.

This is the simulation result of proposed DCDL with dual edge triggered flip-flop. It consumes less power than existing DCDL.

C. Simulation result of proposed NIKOLIC sense amplifier based flip-flop

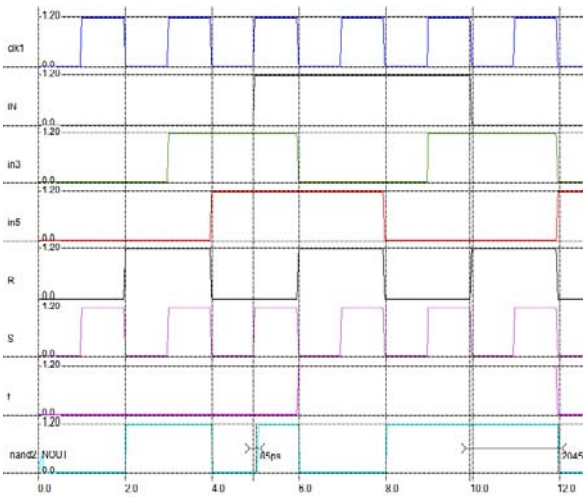

Figure-11. Simulation result of proposed DCDL with NIKOLIC latch sense amplifier based flip-flop.

This is the simulation result of proposed DCDL with NIKOLIC- latch sense amplifier based flip-flop. It reduces delay time and power than existing DCDL.

5. RESULT ANALYSIS

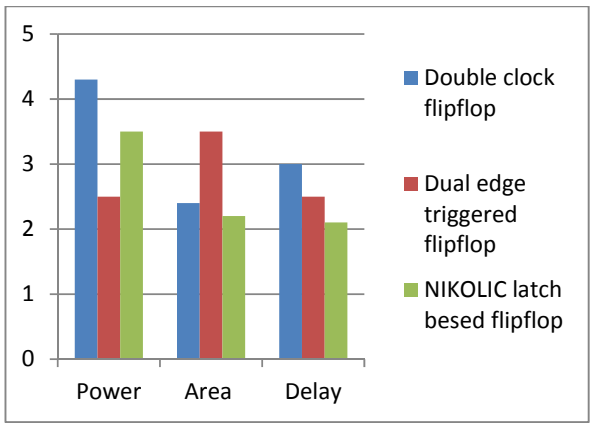

Figure-12. Comparison chart for power, area and delay.

Microwind tool has been used for analyzing the power consumption and delay of both the existing and proposed sense amplifier based flip-flop. The area has been analyzed in terms of total gate count used. The power consumption of existing double clock flip-flop is P=0.546mw. And the proposed NIKOLIC latch based flip-flop and dual edge triggered sense amplifier based flip-flop consumes 0.468mw and 45.252µw power. This is less compared to other and concluded that dual edge triggered flip-flop had better performances in power and delay.

6. CONCLUSIONS

In this paper, a phase locked loop with glitch free NAND based DCDL has been presented. Two driving techniques of driving circuits for the NAND based DCDL have been considered to generate the control bits. By using these proposed techniques, low power consumption and delay are achieved. All the simulation results are carried out using MICROWIND tool, designed at 90nm CMOS technology. For the future more advanced driving techniques would be applicable to achieve better performances in power, area and delay.

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