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A NOVEL HIGH PERFORMANCE DYNAMIC VOLTAGE LEVEL SHIFTER

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ABSTRACT

Level shifters are interfacing circuits, generally for Low voltage to high voltage translation Level shifters are used and high to low translation inverters are sufficient, but it needs an additional circuitry. In this paper we have presented a novel high performance Dynamic Voltage Level Shifter. It is a unique circuit will perform level-up shift, level-down shift, and Blocking. The type of shift, Level up/down is will be performed automatically based on its input voltage (VIN). The proposed dynamic voltage level shifter has designed and simulated in 90nm technology. Simulation results demonstrate that the proposed level shifter translates voltages between 0.4V to 1V and vice versa, at operating frequencies of 100 KHz, 500 KHz, and 1 MHz. It is observed that the proposed design having static power of 4.6 nW while level up, and 2.8 nW while level down operations. Level up and level down average active power is 20.9nW.

Keywords: delay, level down shift, level up shift, low power consumption, multi VDD systems.

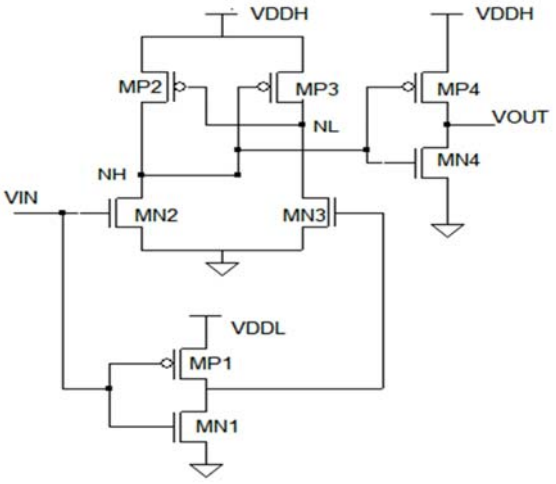
INTRODUCTION

Power and energy optimization are the important and significant issues need to be addressed as the technology moves towards sub-micron and deep sub-micron technologies. In general, high power consumption and energy consumption per transaction not just shortens the battery life span and also cause thermal and reliability problems for handheld devices.Low power appliance such as pacemakers, micro sensors, personnel note books, palmtops and many moveable devices operates under high energy constraints may reduce the long battery life. Hence the designing the digital system, to attain high speed computation with low power is very essential and becoming major design anxiety for VLSI and ULSI system designs.

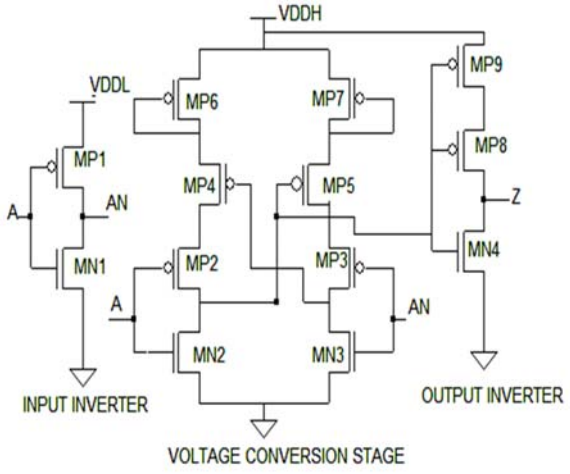
There are number of power reduction techniques adopted to reduce power consumption at circuit level and integrated circuit level such as reducing transistor size, reducing supply voltage, and multi threshold voltages (Multi Vt) [1], [2], [3]. However there are number of drawbacks like increases in leakage power, low driving capabilities, unbalanced noise margins power, and increases in latency [2]. The above drawbacks can be overcome with Clustered Voltage Scaling (CVS)/multi-supply voltage system [4]. To adopt such kind of system, the whole system is partitioned to voltage islands and will be operated with different supply voltages. All the critical path voltage islands are provided with higher supply voltage (VDDH) to increase the speed performance and non-critical path voltage islands are provided with lower supply voltage (VDDL) to reduce the power consumption and will yields reduced power consumption at system level [5]. To interface these voltage islands efficient interfacing modules are needed, these interfacing modules are nothing but voltage Level Shifter (LS).Voltage Level shifters are interfacing modules, used to voltage translate or shift from one voltage level to other voltage level. The LS as broadly viewed as level up shifter and level down shifter. While level up shift the low input voltage (VIN) driven by the VDDL module will be translated to the higher voltage level (VDDH), which is the logic '1' voltage level of VDDH module. While level down shift the high input voltage (VIN) driven by the VDDH module will be translated to the lower voltage level (VDDL), which is the logic '1' voltage level of VDDL module. Generally level up is performed by level shifters and level down shift can be with inverters [6]. In this paper we have introduced a new a novel high performance Dynamic Voltage Level Shifter (DVLS). It is a unique design, which performs up shift, down shift, and blocking just with 13 numbers of MOS transistors with lower power and energy consumption. The remaining part of the paper has arranged in the following order, next section describes about review on existing Level shifters, then another section deals with proposed novel high performance DVLS, after that Section four brief out about simulation results and analysis, and last section concludes the paper.

REVIEW ON EXISTING LEVEL SHIFTERS

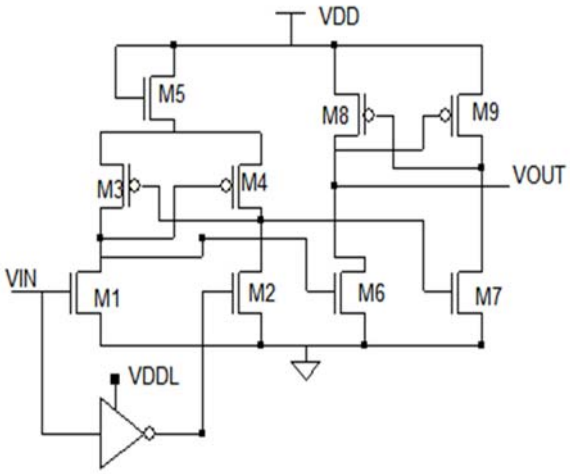
The review on existing level shifters is performed in this section. The very basic form of LS is a Cross-Coupled LS (CCLS), it is a Differential Cascade Voltage Switch Logic (DCVSL) designed for the purpose of level up shift only, shown in Figure-1(a). The DCVSL is a ratioed circuit, it poses a contention problem between pull-up &pull-down transistors, as a consequence pull up and pull down impedances need to be properly designed and it is useful only for level up shift [7]. The LS proposed by Marco Lanuzza*et al*. [7] shown in Figure-1(b) require more area to perform only level up operation. Figure-1(c) The LS proposed by Wooters*et al*. [8] used the two stages,



(a)



(b)



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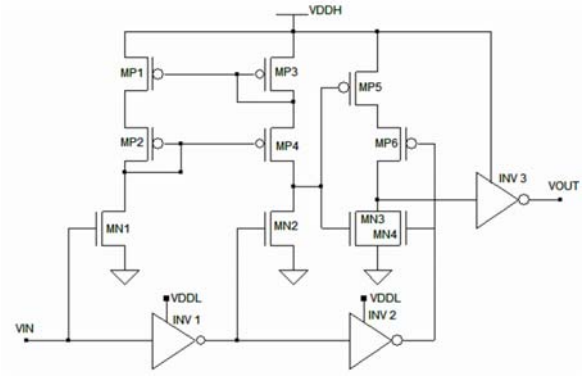


(d)

Figure-1. Existing level shifters.

the first stage deals with DCVSL logic with ON NMOS transistor, and the next stage is another DCVSL circuit to achieve high voltage swing between power rails and it is suitable only for level up shift, at the same time it may be poor speed performance. A wide range LS shown in Figure-1(d), using modified Wilson current mirror is proposed by Shien Chun Luo*et al*. [9], useful for wide range level shifting applications, having provision for bidirectional capability, balancing in rise and fall time delays, and it uses three stages to perform level shifting. Unfortunately it is lagging with auto selection of type of shift and passing/blocking kind of operations.

PROPOSED DYNAMIC VOLTAGE LEVEL SHIFTER

The proposed DVLS design is depicted in Figure-2. This design is quite different from other existing LSs. All existing LSs are capable to perform level up shift and some of the designs having provision to perform level down shift. This proposed novel high performance DVLS circuit performs both level up and level down shift just based on its input voltage (VIN) and having the provision to Block the data. The operation can be split up in to two parts.

Level up/down shifting

The MOS transistors MP3, MN3 and its connection topology resemble as 2X1 Mux, its VIN is a select line, and level shifting voltages VDDH and VDDL are the selectable inputs. Based on input voltage VIN, either VDDH or VDDL will be selected and available at virtual VDD. The remaining 7 MOS transistors MN1, MP1, MN2, MP2, MN4, MP4, and MP5 and its connection topologies will perform level translation operation. As an illustration VDDH is 1V, VDDL is 0.4V and the possible values of VIN is 0.4V, 1V, and 0V are taken and BLOCK enable has negated.

When VIN is 0.4V, the MOS transistor MP3 becomes ON, the VDDH will appears at VDD, the level shifter circuit is getting biased with VDDH, the gate

voltages of MN2, MP2, and MP4 is close to VSS, MP2 becomes ON and MN2 becomes OFF and the VOUT node will charged to strong VDDH, i.e. 1V through MN6-MP7 ON transmission gate, and level up shift is the resultant.

When VIN is 1V, the MOS transistor MN3 becomes ON, the VDDL will appears at VDD, the level shifter circuit is getting biased with VDDL, the gate voltages of MN2, MP2, and MP4 is close to VSS, MP2 becomes ON and MN2 becomes OFF and the VOUT node will charged to strong VDDL, i.e. 0.4V through MN6-MP7 ON transmission gate, and level down shift is the resultant.

When VIN is 0V, the MOS transistor MP3 becomes ON, the VDDH will appears at VDD, the level shifter circuit is getting biased with VDDH, the gate voltages of MN2, MP2, and MP4 is close to VDDH, hence MP2 becomes OFF and MN2 becomes ON and the VOUT node will be discharged to strong VSS, i.e. 0V through MN6-MP7 ON transmission gate.

This novel high performance DVLS circuit performs up-shift/down-shift just based on its input voltage VIN i.e. when VIN closure to VDDL, it acted as Level Up shifter and when VIN is closure to VDDH, it acted as Level Down shifter, hence it has named as dynamic voltage Level Shifter.

Blocking

The blocking circuit comprises with MOS transistors MN5, MP6, MN6, and MP7, with a blocking enable input called BLOCK. When BLOCK enable is asserted completely stopping of signal takes place due to MN6-MP7 OFF transmission gate, and will be in high impedance state. In normal mode the BLOCK enable will be in negation state. The assertion and negation of BLOCK enable depends on driving/driven modules.

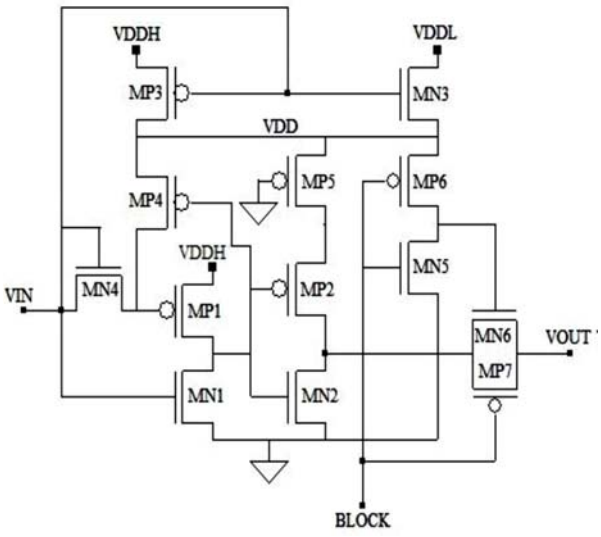


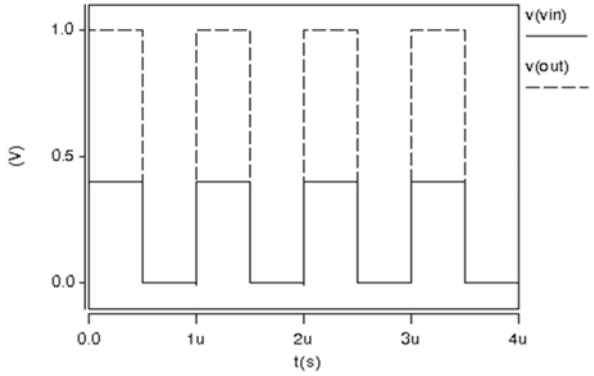
Figure-2. Proposed dynamic voltage level shifter.

SIMULATION RESULTS AND ANALYSIS

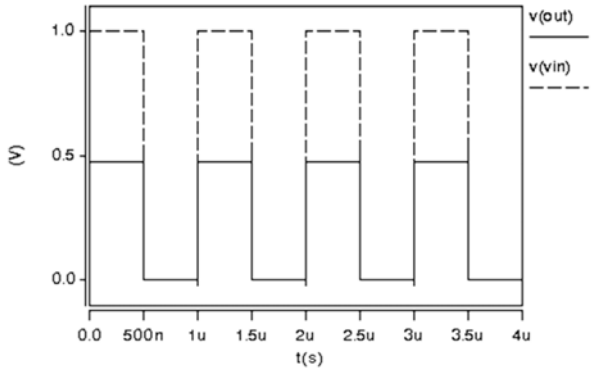
The novel high performance DVLS design is designed and simulated at with L=90nm, NMOS W=180nm, and PMOS W=360nm in Synopsis HSPICE at 90nm technology. The circuit has designed to work with threshold voltages of NMOS is 0.3V and PMOS is –0.3V respectively. The robustness of the design is tested with a load capacitance of 10fF, temperature of 27 ^{0}C, and at the frequencies of 100 KHz, 500 KHz, and 1 MHz.

Waveforms

The logic level simulation has shown in the Figure-3 at a frequency of 1 MHz. The Figure-3 (a) depicts the voltage level up shifting from 0.4 V to 1 V and the Figure-3 (b) depicts the voltage level down shifting from 1V to 0.4 V.



(a)



(b)

Figure-3. Waveforms (a) Level up (b) Level down shifts.

Performance analysis

Figures 4 and 5 shows the average power consumption of the proposed DVLS to perform level up and level down shifts for the varying VDDH from 0.9V to 1.1V and VDDL from 0.4V to 1V respectively, at different frequencies are 100 KHz, 500 KHz, 1 MHz. Figure-4 depicts the average power consumption while level up shift, for varying VDDH from 0.9V to 1.1V with a

constant of VDDL 0.4V. Figure-5 depicts the average power consumption while level down shift, for varying VDDL from 0.3V to 0.5V with a constant of VDDH 1V.

Figures 6 and 7 depicts the energy per transitions of proposed LS while level up and level down with varying VDDH and VDDLs, respectively. The energy per transitions were lower both in level up and level down transitions It can be observed that the energy per transition is low at higher frequencies like 1MHz and 500 KHz and then 100 KHz.

Figure-8 shows the delay of the proposed design as function of varying VDDH from 0.9V to 1V at a constant VDDL 0.4V. The delay of the proposed design is decreases as increases in VDDH and almost uniforms at all the frequencies.

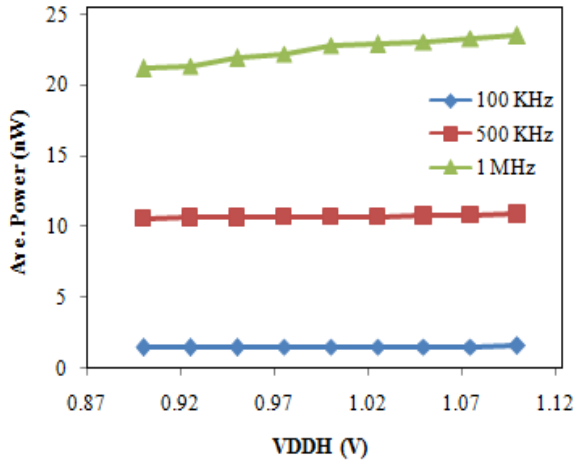


Figure-4. Average power of proposed LS at VDDL = 0.4V.

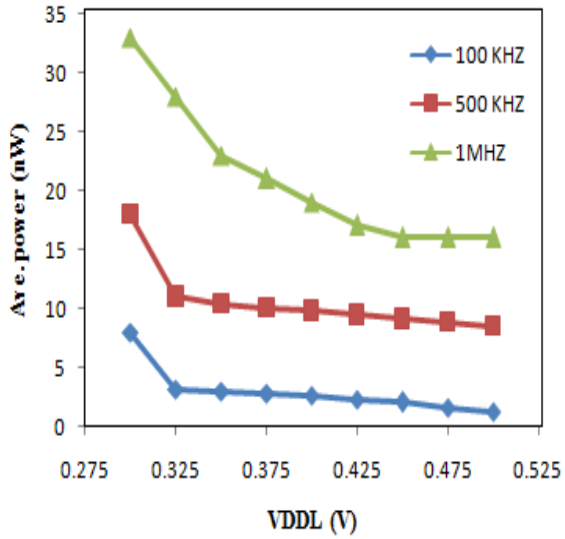


Figure-5. Average power of proposed LS at VDDH = 1V.

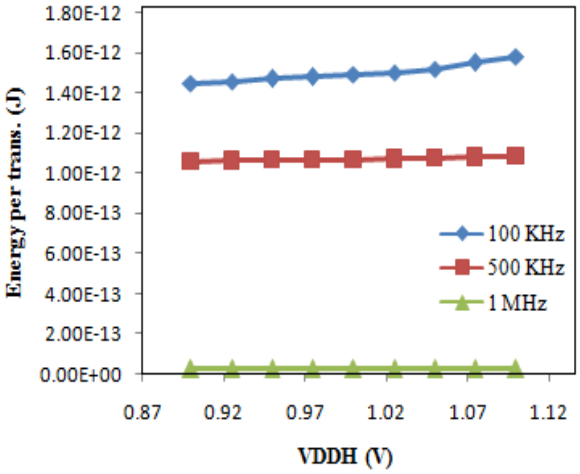


Figure-6. Energy per transition of the proposed LS as a function of VDDH at VDDL=0.4V.

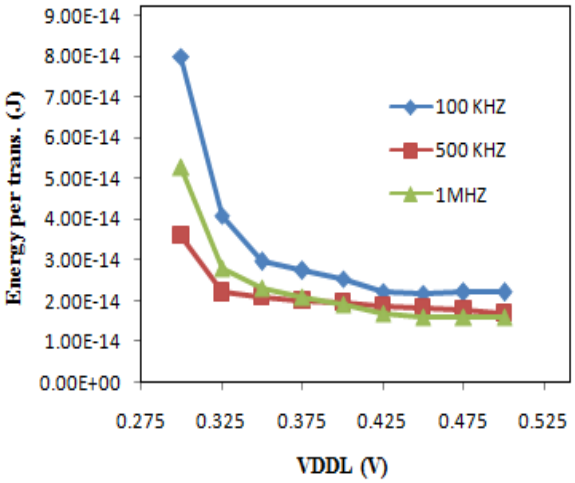


Figure-7. Energy per transition of the proposed LS as a function of VDDL at VDDH= 1V.

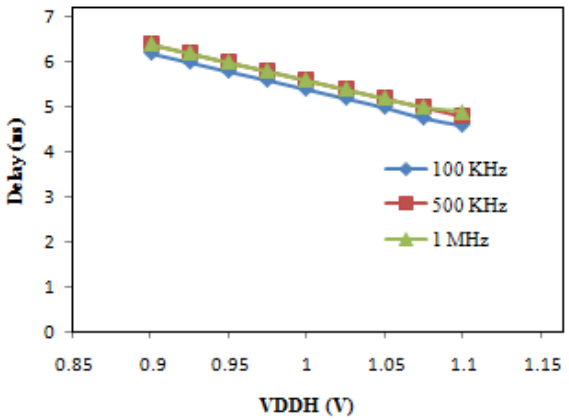


Figure-8. Delay of proposed LS as a function of VDDH at VDDL=0.4V.

Comparative analysis with other designs

Table-1shows the comparison between proposed DVLS with other five benchmark level Shifter (LS) designs. The proposed design having lower average level up and level down static power consumption is 3.7 nW, active power is 20.9 nW at an Energy per transition 2.09E-14J, and delay is 5.6ns, these parameters can be compared with LSs [7], [8], [9], [10], and [11]. The LS design in [7] having static power consumption of 6.4nW and delay 22ns at 90nm technology, and it performs level up only. The LS design in [8] also performs only level up shift with active power consumption of 90nW and delay is 10ns at 130nm technology. The LS in [9] having a provision to performs both level up and level down at average static power consumption 15nW with a delay of 15ns at 65nm technology, with a signal frequency of 20 KHz. The design in [10] having huge active power and performs only level up shift. The LS design in [11] having static power consumption of 6.6nW and delay 18.4 ns at 90nm technology, and it performs level up shift only. From the above LSs, it also can be comparable that, there are some LSs with higher VDDH with higher delays.

CONCLUSIONS

We have designed, and simulated a novel high performance dynamic voltage level shifter with 13 no. of transistors to perform level up, level down and blocking operations. The designed LS having the provision of auto selection of level up or level down just based on its input voltage (VIN). The type of operation, either shifting or blocking will depends on its driving /driven modules or cores. Simulation results show that proposed circuit is able to shift 0.4V to 1.V and vice versa. As an illustration the frequency at 1MHZ, VDDL=0.4V and VDDH=1V are taken to report the power and delay constraints It offers very low static power dissipation compared with other designs. The average level up and level down active power is 20.9 nW, which is approximately 28.2% of other best bench mark design [7]. And the average level up and level down static power consumption is 3.7 nW.

Table-1. Comparative analysis of various level shifters.

Work/Ref.	Type of shift	Technology	Frequency (Hz)	VDDL (V)	VDDH (V)	Power (nW)	Energy per tran. (J)	Delay (ns)
[7]	Level up	90nm	1M	0.18	1	Pa = 74	7.40E-14	22
[8]	Level up	130nm	1M	0.188	1.2	Pa = 90	9.00E-14	10
[9]	Level up and down	65nm	20K	0.4	1.2	Ps = 15	----	15
[10]	Level up	350nm	10K	0.4	3	Pa = 150	1.50E-11	10
[11]	Level up	90nm	1M	0.2	1	Pa = 93.6	9.36E-14	18.4
[12]	Level up	90nm	1M	0.4	1	Pa = 80	8.0E-14	0.8
[13]	Level up and down	90nm	1M	0.4	1	Pa =24	2.40E-14	17.3
Proposed	Level up and down	90nm	1M	0.4	1	Ps= 3.7/ Pa =20.9	2.09E-14	5.6

Pa – Active power, Ps – Static power

The average level up and level down energy per transition is also very low, and it is just 2.09E-14 J. The entire design have maintained uniform Vt transistors, Minimum VDDL to Maximum VDDH conversion ratio is 0.25 have obtained. The some more optimized power, delay and better minimum VDDL and Maximum VDDH ratio can be achieved with multi V_t transistors.

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