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A NOVEL ARITHMETIC AND LOGIC UNIT DESIGN USING UNCONVENTIONAL MATHEMATICS

Nirmal Bhardwaj and V. J. K. Kishor Sonti
Department of Electronics and Communication Engineering, Sathyabama University, Chennai, India
E-Mail: nirmalbhrdwj@gmail.com

ABSTRACT

The ever increasing demand in enhancing the speed of processors to handle the challenging problems has resulted in the need of an efficient ALU. The speed of ALU greatly depends on multiplier and Vedic mathematics helps in the design of an efficient multiplier using Anurupyena and Urdhva Tiryakbhyam. Using Ekadhikena Purvena and Dwandwayoga a squarer circuit is generated. After designing the proposed Vedic multiplier and Squarer Circuit, it is integrated into an eight bit module of arithmetic logic unit along with the conventional adder, subtractor, and basic logic gates. The performance of the Different Multipliers and Squarer circuit is analyzed using Xilinx ISE 9.1i.From the results it is found that Dwandwayoga Squarer is better than Ekadhikena in terms of time delay but on the other hand Ekadhikena Purvena consumes less power than Dwandwayoga. Among multipliers Anurupyena is better in terms of power consumption than Urdhva Tiryakbhyam but it is having much delay. After synthesizing each module of multipliers they are incorporated into the existing ALU Design.

Keywords: arithmetic logic unit, mathematics, anurupyena, urdhva tiryakbhyam, ekadhikena purvena, dwandwayoga.

1. INTRODUCTION

In digital electronics, an ALU is a digital circuit that performs arithmetic and logical operations on integers and binary numbers. The inputs to an ALU are the data to be operated on and it is called as operands and a code indicating the operation to be performed; the ALU's output is the result of the performed operation. Here in the design of ALU ancient Vedic mathematics sutras have been used. In section 2 all the Vedic sutras pertaining to the design of ALU are discussed in brief.Section2.1 illustrates the Anurupyena multiplier.Section2.2 illustrates about Urdhva Tiryakbhyam. Section 2.3 and Section 2.4 illustrates the sutras for squaring of numbers. Section III describes about the simulation output for all the Vedic multipliers. Section IV describes about result summary in terms of power and time delay. Finally the conclusion is given in section V.

2. VEDIC MATHEMATICS

Vedic Mathematics is the name given to the ancient system of Indian Mathematics which was rediscovered between 1911 and 1918 by Sri Bharati Krishna Tirthaji (1884-1960). Vedic Mathematics contains sixteen sutras among them the sutras which are used for the design of ALU are discussed here. Table for Vedic sutras relevant for multiplication is given below.

Table-1. Vedic Sutras relevant to the data conditions.

DATA CONDITIONS	SUITABLE VEDIC SUTRA APPLICABLE
Numbers near to multiple of 10	Anurupyena
Squaring of numbers ending with 5	Ekadhikena Purvena
Squaring of numbers(other cases)	(Dwandwayoga)Duplex method
Multiplication of numbers (all other cases)	Urdhva Triyakbhyam

2.1 Anurupye (Shunyamanyat) sutra

Anurupyena is an up sutra which means proportionality. This Sutra is used to find the product of two numbers when both the numbers are close to the common bases like 50, 60, 200 etc (multiples of powers of 10) [3]. Block Diagram of Anurupyena multiplier is given in Figure-1.

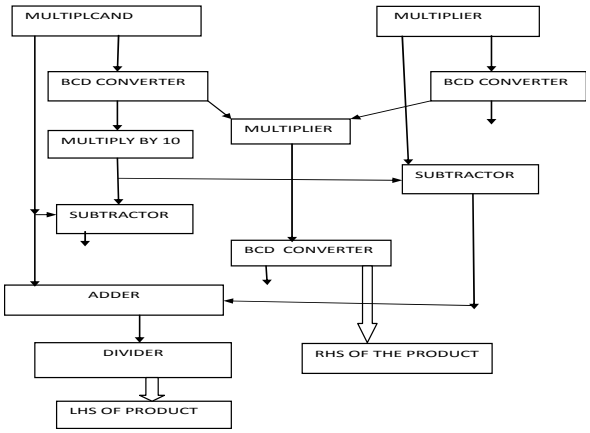

Figure-1. Anurupyena multiplier logical diagram.

2.2 Urdhva Tiryakbhyam

The 'Urdhva Tiryakbhyam' sutra is a common method of multiplication which can be applied to all cases of multiplication. Figure-2 shows the diagrammatic representation of UT process flow.The rule of this multiplication is at first, multiplication starts from MSB, of both multiplicands to get first cross product. Then increasing one bit, further calculation of cross products

takes place between the bits of multiplicands goes till all bits are used. Then further dropping bits from MSB (or LSB) process of cross product is continued till only LSB (or MSB) is used for cross product. Here the notable characteristic of this multiplication is that determination of cross product and the summation involved with each step takes place simultaneously.

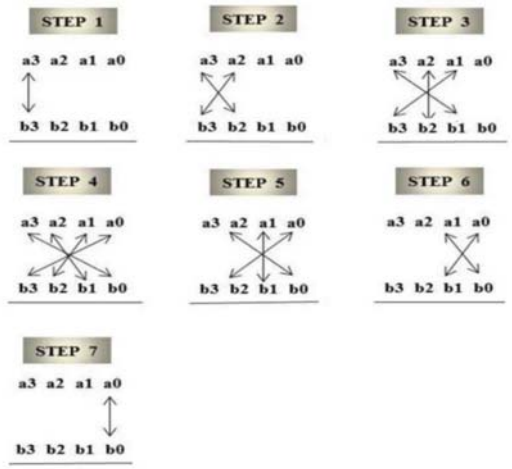

Figure-2. Multiplication steps for multiplying two numbers using Urdhva Tiryakbhyam Sutra.

2.3 Dwandwayoga

Decimal squaring is achieved very quickly for formula Dwandwayoga which means duplex. Duplex of a digit is obtained by multiplication with itself, i.e. duplex of a will be a^2. Duplex of two digit numbers is obtained by doubling their product, duplex of ab is 2×a×b. Duplex of three digit number is obtained by addition of square of middle digit and twice product of first and second. So abc will have duplex (2×a×c + b2).

Illustration: Duplexes of Numbers

Duplex of 4= 16

Duplex of 43 =2*4*3 = 24

Duplex of 182 =2*1*2 + 8^2 = 68

Duplex of 3824= 2*3*4 + 2*8*2 = 56

Duplex of 10934= 2*1*4 + 2*0*3 + 9^2= 8 + 0 + 81 = 89

Duplex of 23456789= 2*2*9 + 2*3*8 + 2*4*7 + 2*5*6 = 36 + 48 + 56 + 60 = 190

Duplex of 33 =2*3*3 = 18.

It can be observed that calculating duplex is based on Urdhva-Tiryakbhyam. To obtain the square of a number, duplexes are calculated starting from a digit on right or left then 20 proceeding leftwards or rightwards to add digits while determining duplex and adding the duplexes similar to the addition of cross-products described. Figure-3 shows complete Illustration of Squaring of a number using Duplex method.

32451^2 = 1053067401

Duplexes No	Duplex
3	9
32	12
324	24+4 = 28
3245	30 +16 = 46
32451	6+20+16 = 42
2451	4+40 = 44
451	8+25 = 33
51	10
1	1

9/12/28/46/42/44/33/10/1 = 9 2 8 6 2 4 3 0 1
1 2 4 4 4 3 1
1 0 5 3 0 6 7 4 0 1

Figure-3. Complete example of squaring.

2.4 Ekadhikena Purvena

Ekadhikena Purvena literally means by one more than the previous. It is generally best used for squaring of numbers which ends with 5. [4]

Figure-4 explains the logical diagram of Ekadhikena Purvena explains this sutra in detail for decimal number ending with 5. Let us take a number 35.Square of 35 is 1225.

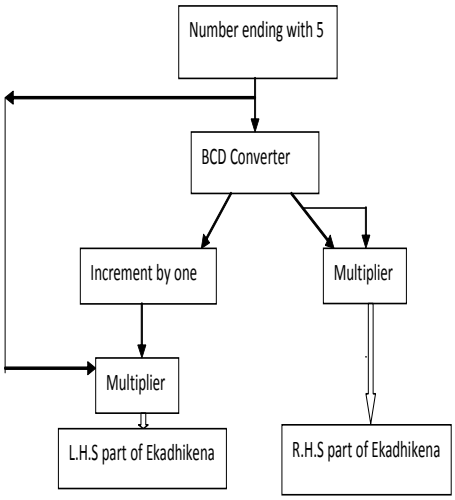

Figure-4. Ekadhikena Purvena squarer logical diagram.

3. SIMULATION RESULTS

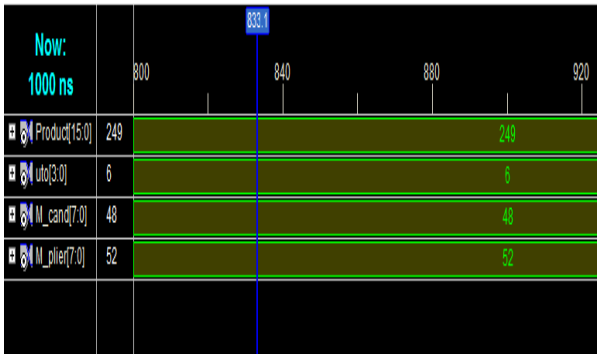

Figure-5. Simulation result of Anurupyena multiplier.

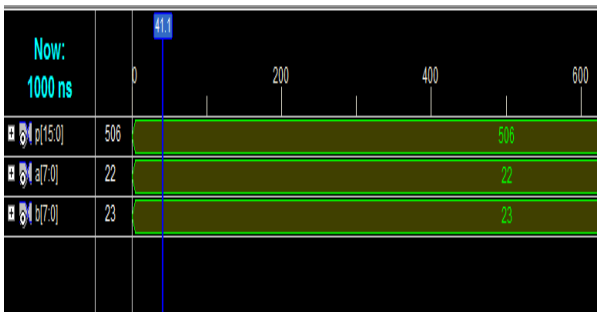

Figure-6. Simulation result of Urdhva Tiryakbhyam.

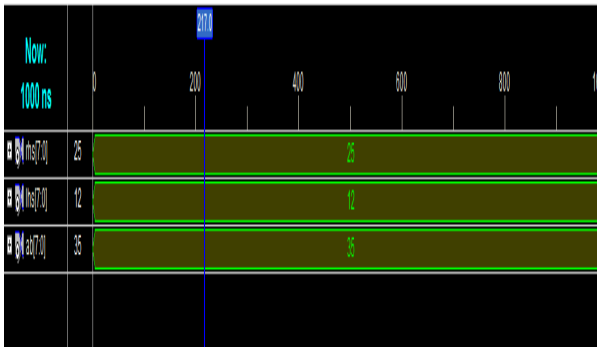

Figure-7. Simulation result of Ekadhikena Purvena Squarer.

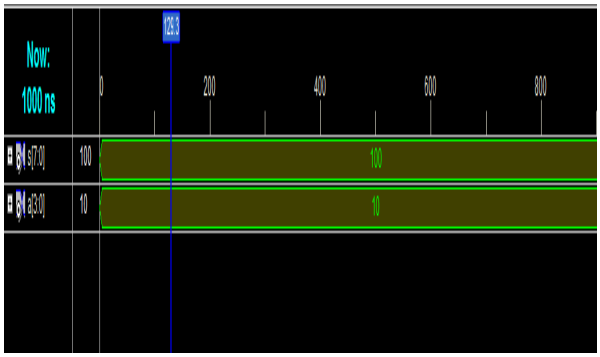

Figure-8. Simulation result of Dwandwayoga multiplier.

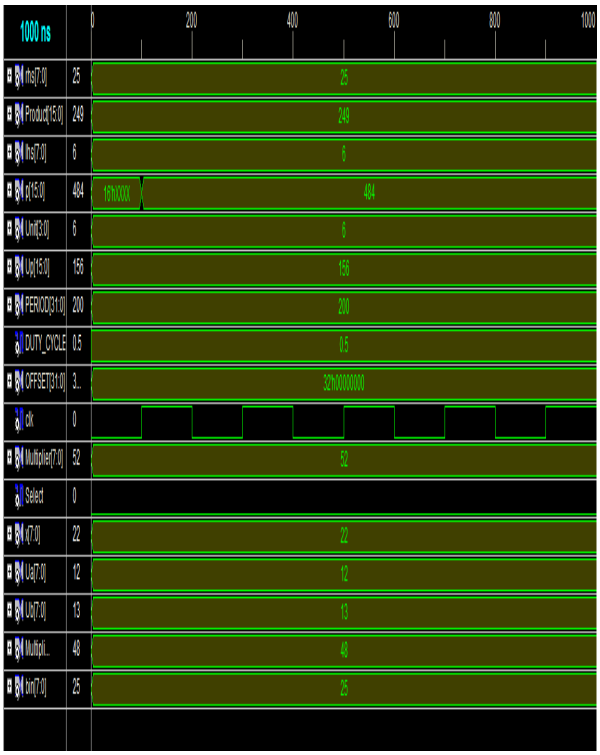

Figure-9. Simulation result of novel design of ALU.

4. COMPARISON TABLE AND RESULTS

TEST1 Partition Summary
No partition information was found.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	522	1,536	33%	
Logic Distribution				
Number of occupied Slices	278	768	36%	
Number of Slices containing only related logic	278	278	100%	
Number of Slices containing unrelated logic	0	278	0%	
Total Number of 4 input LUTs	522	1,536	33%	
Number of bonded IOBs	108	124	87%	
Total equivalent gate count for design	3,183			
Additional JTAG gate count for IOBs	5,184			

Performance Summary			
Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints		

Figure-10. Device utilization summary of the proposed ALU.

Table-2. Comparision table of multipliers and squarer.

Vedic multiplier	**Power consumption** (mw)	**Time delay** (ns)
Ekadhikena Purvena	24	24.95
Urdhva tiryakbhyam	34	22.96
Anurupyena	24	35
Dwandwayoga	37	9.07

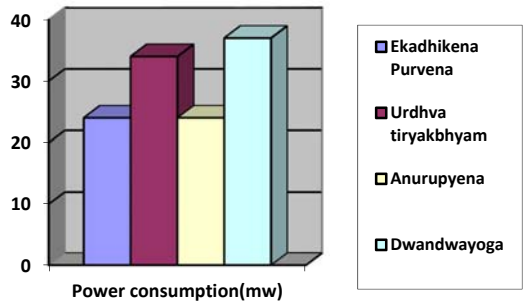

Figure-11. Power consumption comparison chart for multipliers and squarer.

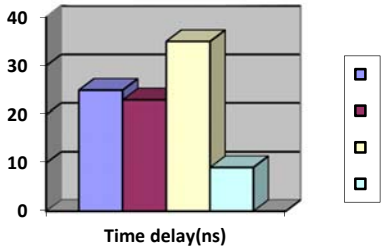

Figure-12. Time delay comparison chart for multipliers and squarer.

5. CONCLUSIONS

The performance of the Different Multipliers and Squarer circuit is analyzed using Xilinx ISE 9.1i. From the results it is found that Dwandwayoga Squarer is better than Ekadhikena in terms of time delay but on the other hand Ekadhikena Purvena consumes less power than Dwandwayoga. Ekadhikena Purvena sutra is applied where the input number ends with 5. Where as Dwandwayoga is applied in general case of squaring of number. Among multipliers Anurupyena is better in terms of power consumption than Urdhva Tiryakbhyam but it is having much delay. After synthesizing each module of multipliers it is incorporated into the existing ALU Design.

The total Power consumption of the proposed ALU design is 24mw. The total time delay of the ALU is 49.95ns. Thus an efficient ALU is designed using the Vedic mathematics is developed.

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